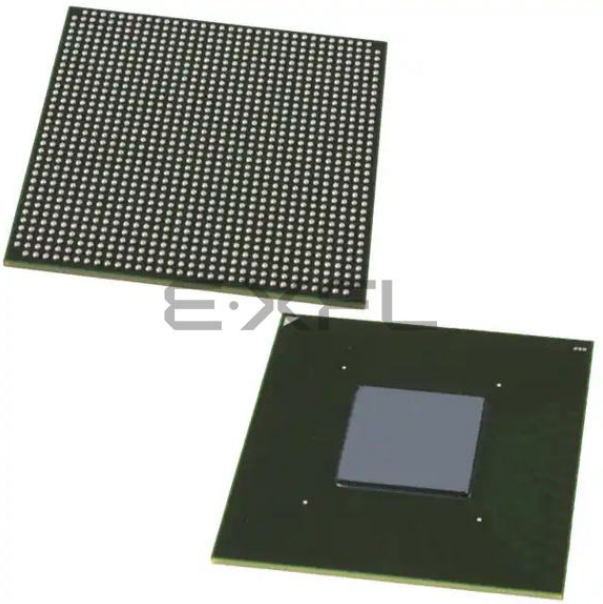

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 19811 |
| Number of Logic Elements/Cells | 420000 |
| Total RAM Bits | 23625728 |
| Number of I/O | 544 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA Exposed Pad |
| Supplier Device Package | 1152-FBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxmb5g4f35c5n |

**Figure 1-1: Equation for OCT Variation Without Recalibration**

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The $R_{OCT}$ value calculated shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
- $R_{SCAL}$ is the OCT resistance value at power-up.
- $\Delta T$ is the variation of temperature with respect to the temperature at power up.
- $\Delta V$ is the variation of voltage with respect to the $V_{CCIO}$ at power up.
- dR/dT is the percentage change of $R_{SCAL}$ with temperature.
- dR/dV is the percentage change of $R_{SCAL}$ with voltage.

## OCT Variation after Power-Up Calibration

**Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices**

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0°C to 85°C.

| Symbol | Description | $V_{CCIO}$ (V) | Value | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.100 | %/mV |
| | | 2.5 | 0.100 | |
| | | 1.8 | 0.100 | |
| | | 1.5 | 0.100 | |
| | | 1.35 | 0.150 | |
| | | 1.25 | 0.150 | |
| | | 1.2 | 0.150 | |

## I/O Standard Specifications

Tables in this section list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Arria V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

### Single-Ended I/O Standards

**Table 1-14: Single-Ended I/O Standards for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$[13] (mA) | $I_{OH}$[13] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3-V LVCMOS | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 2 | –2 |
| 3.0-V LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| 3.0-V LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | 0.3 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

(13) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

## Transceiver Specifications for Arria V GT and ST Devices

### Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300(42)/2000 | mV |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | — | 1.2 | — | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | mV |

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | –3 speed grade | 5 | — | 800[61] | MHz |
| | | –4 speed grade | 5 | — | 800[61] | MHz |
| | | –5 speed grade | 5 | — | 750[61] | MHz |
| | | –6 speed grade | 5 | — | 625[61] | MHz |
| $f_{INPFD}$ | Integer input clock frequency to the phase frequency detector (PFD) | — | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional input clock frequency to the PFD | — | 50 | — | 160 | MHz |
| $f_{VCO}$[62] | PLL voltage-controlled oscillator (VCO) operating range | –3 speed grade | 600 | — | 1600 | MHz |
| | | –4 speed grade | 600 | — | 1600 | MHz |
| | | –5 speed grade | 600 | — | 1600 | MHz |
| | | –6 speed grade | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | — | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock | –3 speed grade | — | — | 500[63] | MHz |
| | | –4 speed grade | — | — | 500[63] | MHz |
| | | –5 speed grade | — | — | 500[63] | MHz |
| | | –6 speed grade | — | — | 400[63] | MHz |

(61) This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(62) The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(63) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $F_{OUT}$ of the PLL.

| Symbol | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | SERDES factor J ≥ 8[76][78], LVDS TX with RX DPA | [77] | — | 1600 | [77] | — | 1500 | [77] | — | 1250 | Mbps |
| | SERDES factor J = 1 to 2, Uses DDR Registers | [77] | — | [79] | [77] | — | [79] | [77] | — | [79] | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Network - $f_{HSDR}$ (data rate)[80] | SERDES factor J = 4 to 10[81] | [77] | — | 945 | [77] | — | 945 | [77] | — | 945 | Mbps |
| Emulated Differential I/O Standards with One External Output Resistor Network - $f_{HSDR}$ (data rate)[80] | SERDES factor J = 4 to 10[81] | [77] | — | 200 | [77] | — | 200 | [77] | — | 200 | Mbps |
| $t_{x\ Jitter}$ -True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |

(78) The $V_{CC}$ and $V_{CCP}$ must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency ($f_{OUT}$), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

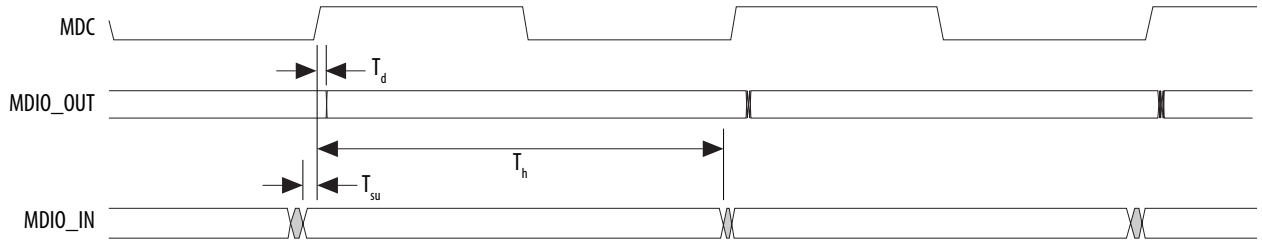
| Symbol | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 260 | — | — | 300 | — | — | 350 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.16 | — | — | 0.18 | — | — | 0.21 | UI |
| $t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network | — | — | — | 0.15 | — | — | 0.15 | — | — | 0.15 | UI |
| $t_{DUTY}$ | TX output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ and $t_{FALL}$ | True Differential I/O Standards[82] | — | — | 160 | — | — | 180 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with Three External Output Resistor Network | — | — | 250 | — | — | 250 | — | — | 300 | ps |
| | Emulated Differential I/O Standards with One External Output Resistor Network | — | — | 500 | — | — | 500 | — | — | 500 | ps |

(82) This applies to default pre-emphasis and $V_{OD}$ settings only.

| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| Receiver | True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J =3 to 10(76) | 150 | — | 1250 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | | SERDES factor J ≥ 8 with DPA(76)(78) | 150 | — | 1600 | 150 | — | 1500 | 150 | — | 1250 | Mbps |
| | $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (77) | — | (83) | (77) | — | (83) | (77) | — | (83) | Mbps |
| | | SERDES factor J = 1 to 2, uses DDR registers | (77) | — | (79) | (77) | — | (79) | (77) | — | (79) | Mbps |
| DPA Mode | DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| Soft-CDR Mode | Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | ±ppm |
| Non-DPA Mode | Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |

(83) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

**Figure 1-15: MDIO Timing Diagram**




## I²C Timing Characteristics

**Table 1-59: I²C Timing Requirements for Arria V Devices**

| Symbol | Description | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{clk}$ | Serial clock (SCL) clock period | 10 | — | 2.5 | — | µs |
| $T_{clkhigh}$ | SCL high time | 4.7 | — | 0.6 | — | µs |
| $T_{clklow}$ | SCL low time | 4 | — | 1.3 | — | µs |
| $T_s$ | Setup time for serial data line (SDA) data to SCL | 0.25 | — | 0.1 | — | µs |
| $T_h$ | Hold time for SCL to SDA data | 0 | 3.45 | 0 | 0.9 | µs |
| $T_d$ | SCL to SDA output data delay | — | 0.2 | — | 0.2 | µs |
| $T_{su\_start}$ | Setup time for a repeated start condition | 4.7 | — | 0.6 | — | µs |
| $T_{hd\_start}$ | Hold time for a repeated start condition | 4 | — | 0.6 | — | µs |
| $T_{su\_stop}$ | Setup time for a stop condition | 4 | — | 0.6 | — | µs |

**Figure 1-18: NAND Address Latch Timing Diagram**

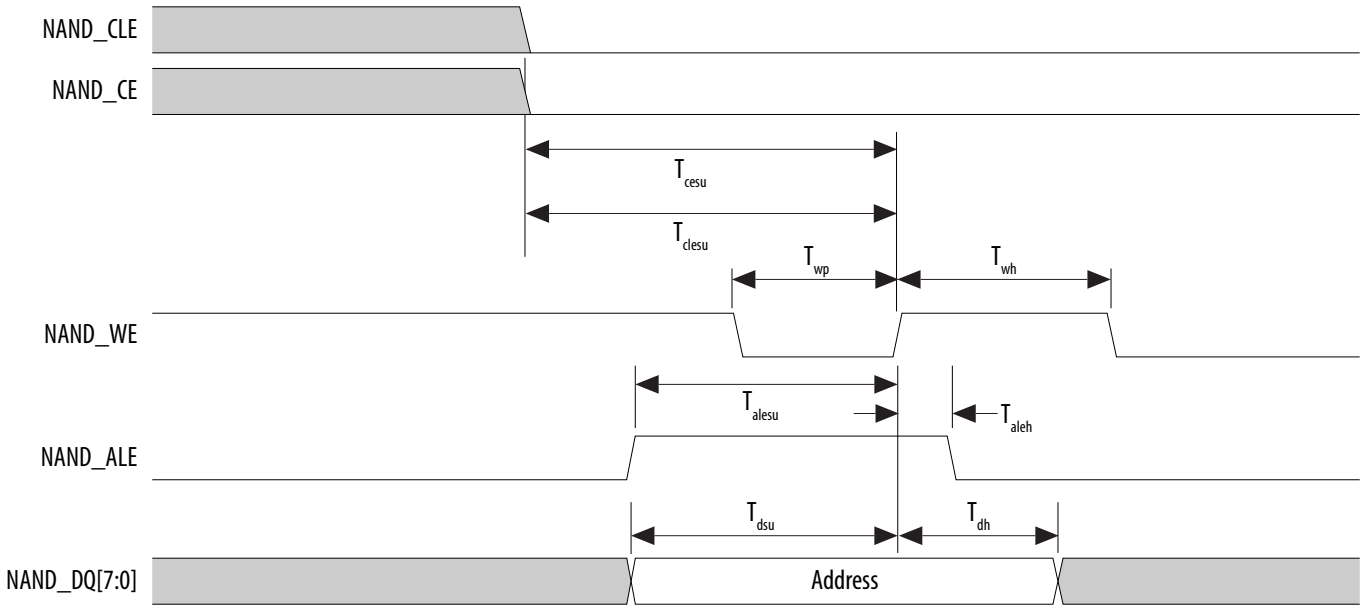
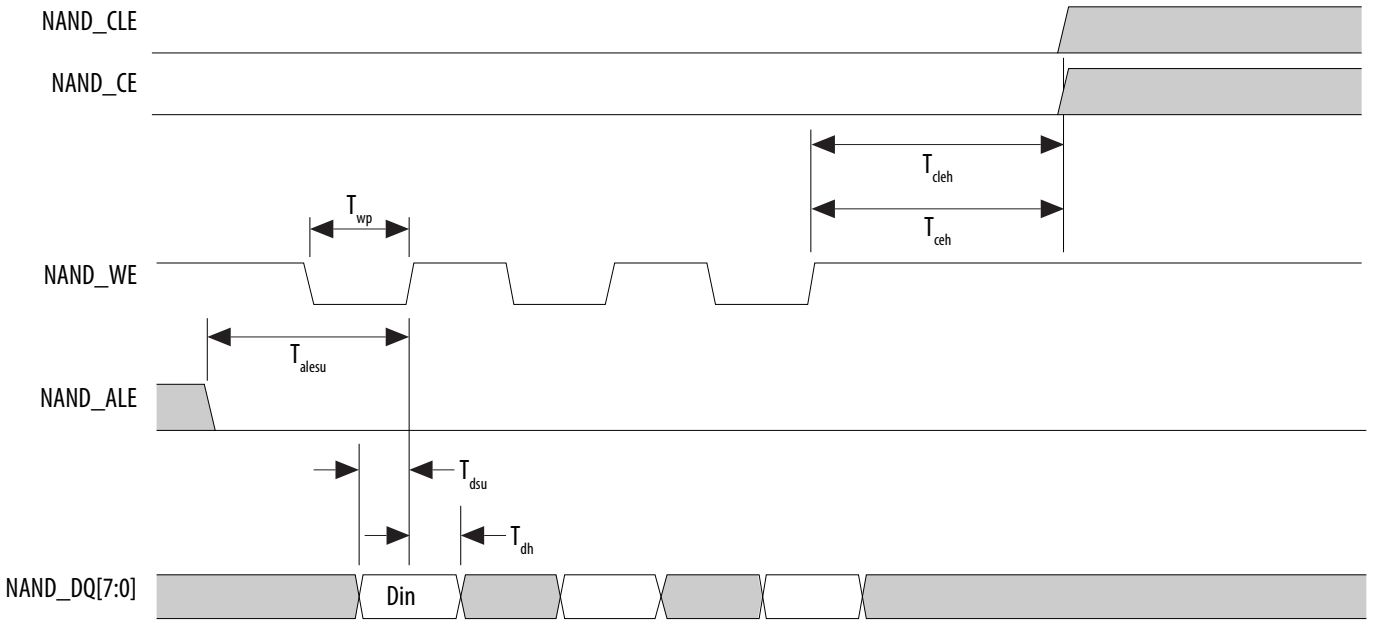


**Figure 1-19: NAND Data Write Timing Diagram**



**Related Information**

- **PS Configuration Timing** on page 1-81
- **AS Configuration Timing**
  Provides the AS configuration timing waveform.

## DCLK Frequency Specification in the AS Configuration Scheme

### Table 1-69: DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| DCLK frequency in AS configuration scheme | 5.3 | 7.9 | 12.5 | MHz |
| | 10.6 | 15.7 | 25.0 | MHz |
| | 21.3 | 31.4 | 50.0 | MHz |
| | 42.6 | 62.9 | 100.0 | MHz |

## PS Configuration Timing

### Table 1-70: PS Timing Parameters for Arria V Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1506(103) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1506(104) | µs |

(103) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(104) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CK}$[105] | nCONFIG high to first rising edge on DCLK | 1506 | — | µs |
| $t_{ST2CK}$[105] | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode[106] | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (T_{init} \times$ CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | 8,576 | — | Cycles |

**Related Information**

**PS Configuration Timing**

Provides the PS configuration timing waveform.

(105) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(106) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

| Symbol | Description | Condition | Minimum[114] | Typical | Maximum [114] | Unit |
|---|---|---|---|---|---|---|
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

## Recommended Transceiver Power Supply Operating Conditions

**Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices**

| Symbol | Description | Minimum [118] | Typical | Maximum[118] | Unit |
|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ [119], [120] | Transceiver channel PLL power supply (left side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GXBR}$ [119], [120] | Transceiver channel PLL power supply (right side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side) | 0.82 | 0.85 | 0.88 | V |

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(118) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(119) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(120) When using ATX PLLs, the supply must be 3.0 V.

## Bus Hold Specifications

### Table 2-9: Bus Hold Parameters for Arria V GZ Devices

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

### Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.

## I/O Standard Specifications

The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

**Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

**Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |

**Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (127) | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | (127) | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | (127) | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF}$ –0.15 | $V_{CCIO}/2$ | $V_{REF}$ + 0.15 | –0.30 | 0.30 |

**Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

(127) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

| Mode [164] | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| Register | 2 | C3, I3L core speed grade | 9.9 | 9 | 7.92 | 7.2 | 4.9 | 4.,5 | 3.92 | 3.6 |
| | 3 | C4, I4 core speed grade | 8.8 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

**Related Information**

**Operating Conditions** on page 2-1

## 10G PCS Data Rate

**Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices**

| Mode [165] | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |
| Register | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |

(164) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(165) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

**Related Information**

**Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

## Initialization

**Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|---|---|---|---|
| Internal Oscillator | AS, PS, FPP | 12.5 | 8576 |
| CLKUSR (222) | PS, FPP | 125 | |
| | AS | 100 | |
| DCLK | PS, FPP | 125 | |

## Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

(221) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(222) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

**Related Information**

- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

## User Watchdog Internal Oscillator Frequency Specification

**Table 2-65: User Watchdog Internal Oscillator Frequency Specifications**

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

**Arria V Devices Documentation page**
For the Excel-based I/O Timing spreadsheet

(226) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(227) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

| Date | Version | Changes |
|---|---|---|
| June 2016 | 2016.06.20 | • Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table.<br>• Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table.<br>• Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table:<br>  • True RSDS output standard: data rates of up to 230 Mbps<br>  • True mini-LVDS output standard: data rates of up to 340 Mbps |
| December 2015 | 2015.12.16 | • Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table.<br>• Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table.<br>• Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table.<br>• Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table. |
| June 2015 | 2015.06.16 | • Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table.<br>• Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table. |
| January 2015 | 2015.01.30 | • Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table.<br>• Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table.<br>• Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table. |