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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	19811
Number of Logic Elements/Cells	420000
Total RAM Bits	23625728
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb5g6f40c6n

Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	–0.50	3.25	V
I _{OUT}	DC output current per pin	–25	40	mA
T _J	Operating junction temperature	–55	125	°C
T _{STG}	Storage temperature (no bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω Table 1-32: Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting ⁽⁵⁸⁾	V_{OD} Value (mV)	V_{OD} Setting ⁽⁵⁸⁾	V_{OD} Value (mV)
V_{OD} differential peak-to-peak typical	6 ⁽⁵⁹⁾	120	34	680
	7 ⁽⁵⁹⁾	140	35	700
	8 ⁽⁵⁹⁾	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.⁽⁵⁹⁾ Only valid for data rates ≤ 5 Gbps.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{OUTPJ_DC}}^{(67)}$	Period jitter for dedicated clock output in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
$t_{\text{FOUTPJ_DC}}^{(67)}$	Period jitter for dedicated clock output in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	250 ⁽⁶⁸⁾ , 175 ⁽⁶⁹⁾	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	25 ⁽⁶⁸⁾ , 17.5 ⁽⁶⁹⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}^{(67)}$	Cycle-to-cycle jitter for dedicated clock output in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}^{(67)}$	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	250 ⁽⁶⁸⁾ , 175 ⁽⁶⁹⁾	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	25 ⁽⁶⁸⁾ , 17.5 ⁽⁶⁹⁾	mUI (p-p)
$t_{\text{OUTPJ_IO}}^{(67)(70)}$	Period jitter for clock output on a regular I/O in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}^{(67)(68)(70)}$	Period jitter for clock output on a regular I/O in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}^{(67)(70)}$	Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}^{(67)(68)(70)}$	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)

⁽⁶⁷⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

⁽⁶⁸⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be $\geq 1000 \text{ MHz}$.

⁽⁶⁹⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be $\geq 1200 \text{ MHz}$.

⁽⁷⁰⁾ External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

DSP Block Performance Specifications

Table 1-37: DSP Block Performance Specifications for Arria V Devices

Mode		Performance			Unit
		-I3, -C4	-I5, -C5	-C6	
Modes using One DSP Block	Independent 9×9 multiplication	370	310	220	MHz
	Independent 18×19 multiplication	370	310	220	MHz
	Independent 18×25 multiplication	370	310	220	MHz
	Independent 20×24 multiplication	370	310	220	MHz
	Independent 27×27 multiplication	310	250	200	MHz
	Two 18×19 multiplier adder mode	370	310	220	MHz
	18×18 multiplier added summed with 36-bit input	370	310	220	MHz
Modes using Two DSP Blocks	Complex 18×19 multiplication	370	310	220	MHz

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX} .

Symbol	Condition	-I3, -C4			-I5, -C5			-C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor $J \geq 8^{(76)(78)}$, LVDS TX with RX DPA	⁽⁷⁷⁾	—	1600	⁽⁷⁷⁾	—	1500	⁽⁷⁷⁾	—	1250	Mbps
	SERDES factor $J = 1$ to 2, Uses DDR Registers	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate) ⁽⁸⁰⁾	SERDES factor $J = 4$ to $10^{(81)}$	⁽⁷⁷⁾	—	945	⁽⁷⁷⁾	—	945	⁽⁷⁷⁾	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate) ⁽⁸⁰⁾	SERDES factor $J = 4$ to $10^{(81)}$	⁽⁷⁷⁾	—	200	⁽⁷⁷⁾	—	200	⁽⁷⁷⁾	—	200	Mbps
$t_{\text{x jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

⁽⁷⁸⁾ The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

⁽⁷⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.

⁽⁸⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

⁽⁸¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Symbol		Condition	-I3, -C4			-I5, -C5			-C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - f_{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 ⁽⁷⁶⁾	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J \geq 8 with DPA ⁽⁷⁶⁾⁽⁷⁸⁾	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	\pm ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

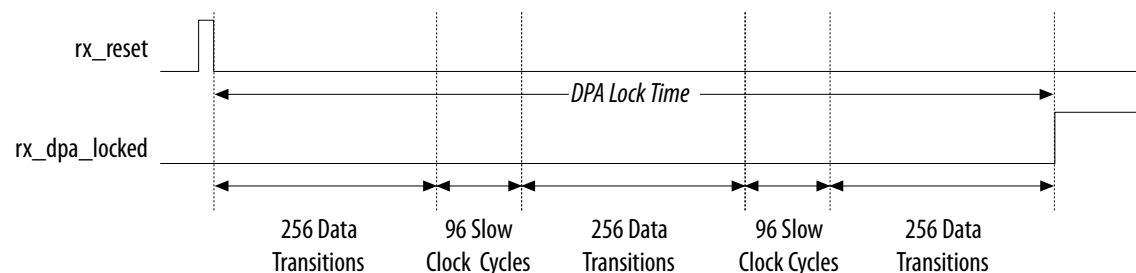


Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

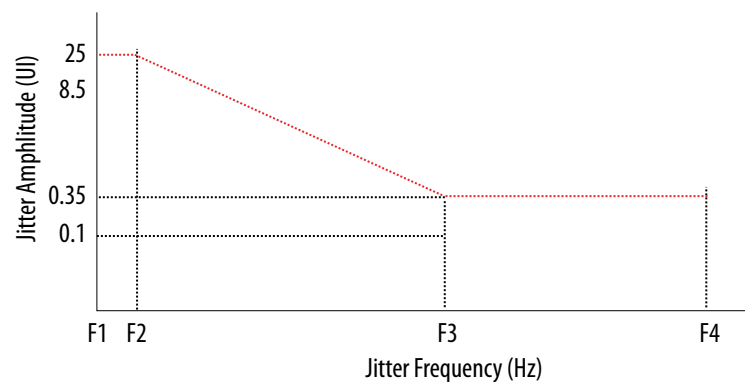


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 1-9: SPI Master Timing Diagram

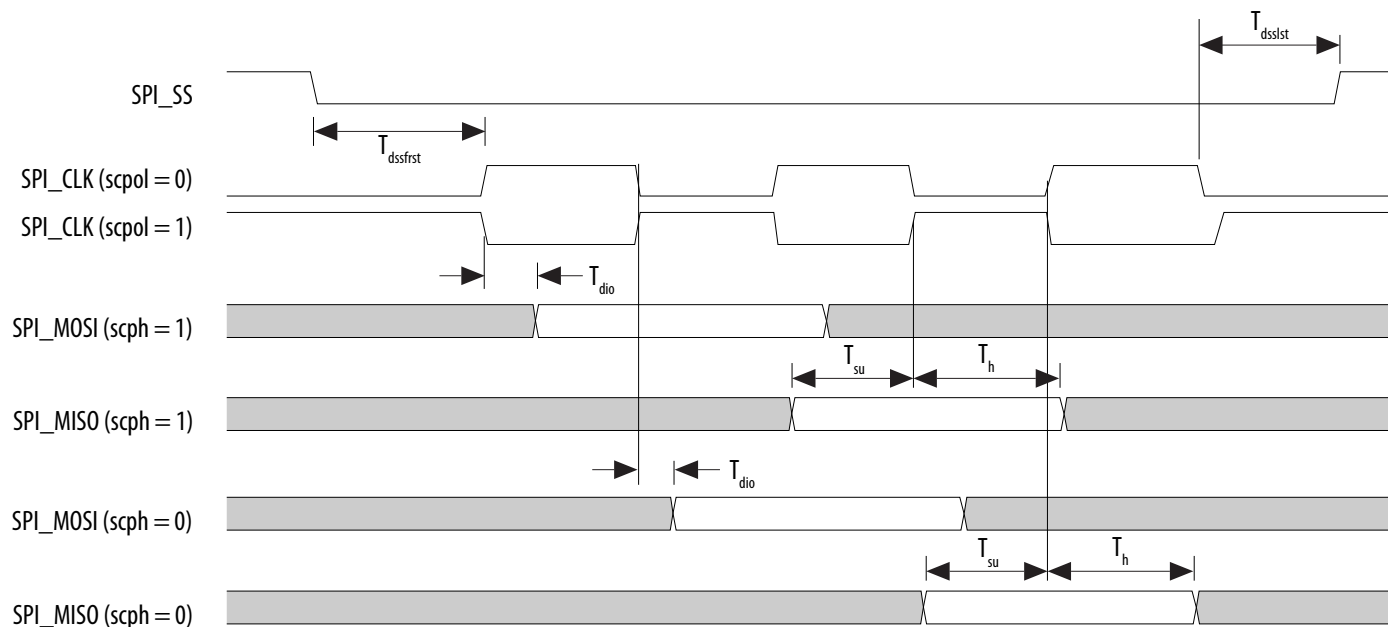


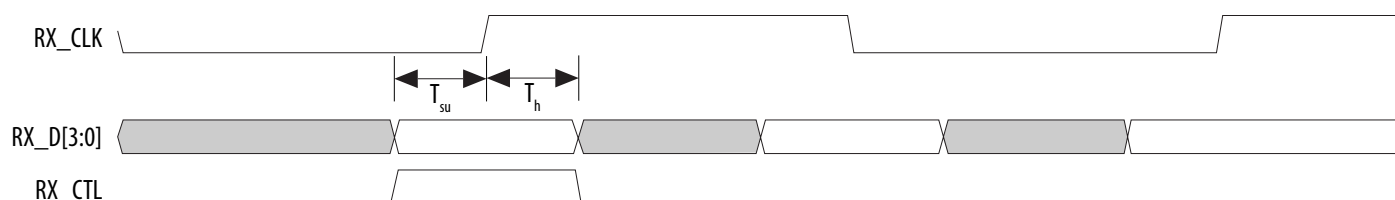
Table 1-53: SPI Slave Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	MISO output delay	—	6	ns

Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_{h}	RX_D/RX_CTL hold time	1	—	ns

Figure 1-14: RGMII RX Timing Diagram**Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_{d}	MDC to MDIO output data delay	10	—	20	ns
T_{s}	Setup time for MDIO data	10	—	—	ns
T_{h}	Hold time for MDIO data	0	—	—	ns

Variant	Member Code	Active Serial ⁽¹⁰⁸⁾			Fast Passive Parallel ⁽¹⁰⁹⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

Related Information**Configuration Files** on page 1-83⁽¹⁰⁸⁾ DCLK frequency of 100 MHz using external CLKUSR.⁽¹⁰⁹⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
June 2012	2.0	<ul style="list-style-type: none">• Updated for the Quartus II software v12.0 release:• Restructured document.• Updated “Supply Current and Power Consumption” section.• Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52.• Added Table 22, Table 23, and Table 33.• Added Figure 1–1 and Figure 1–2.• Added “Initialization” and “Configuration Files” sections.
February 2012	1.3	<ul style="list-style-type: none">• Updated Table 2–1.• Updated Transceiver-FPGA Fabric Interface rows in Table 2–20.• Updated V_{CCP} description.
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	<ul style="list-style-type: none">• Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36.• Added Table 2–5.• Added Figure 2–4.
August 2011	1.0	Initial release.

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
$V_{CCR_GXBL}^{(121)}$	Receiver analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCR_GXBR}^{(121)}$	Receiver analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCT_GXBL}^{(121)}$	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCT_GXBR}^{(121)}$	Transmitter analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{OUTPJ_IO}}^{(173), (175)}$	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}^{(173), (175), (176)}$	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}^{(173), (175)}$	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}^{(173), (175), (176)}$	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}^{(173), (177)}$	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

⁽¹⁷⁵⁾ The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

⁽¹⁷⁶⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

⁽¹⁷⁷⁾ The cascaded PLL specification is only applicable with the following condition:

- Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
- Downstream PLL: $\text{Downstream PLL BW} > 2$ MHz

Description	Min	Typ	Max	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x \text{ Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x \text{ Jitter}}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
$t_{\text{RISE}} \& t_{\text{FALL}}$	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

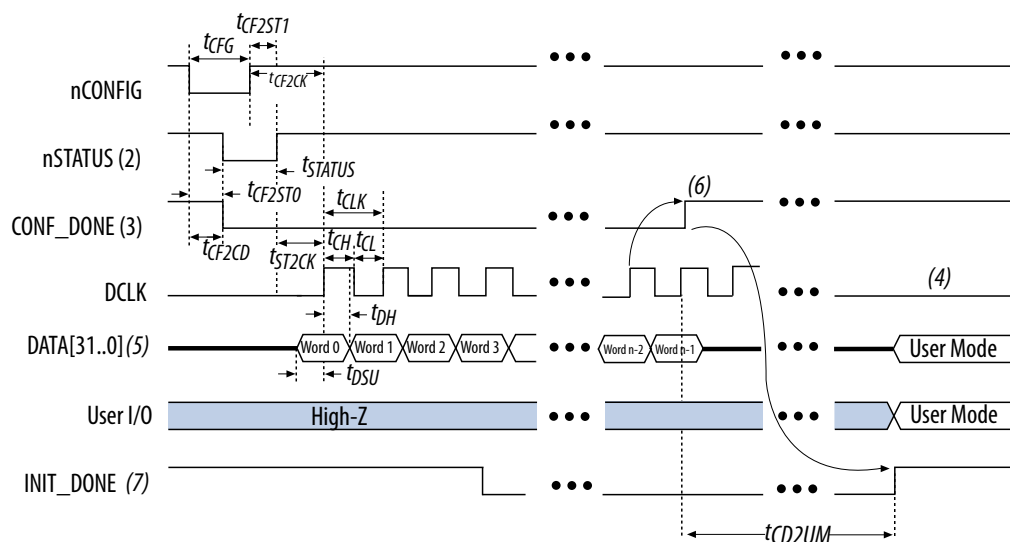
When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX[®] II or MAX V device as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP $\times 16$, use DATA[15..0]. For FPP $\times 8$, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μs
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²¹⁰⁾	μs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²¹¹⁾	μs
t_{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t_{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$ ⁽²¹³⁾	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μs

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹²⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²¹³⁾ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	<ul style="list-style-type: none"> Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table. Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.