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Details

Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb7g4f40c5n

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AV-51002



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This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

Related Information

[Arria V Device Overview](#)

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			-I3, -C4	-I5, -C5	-C6	
60- Ω and 120- Ω R _T	Internal parallel termination with calibration (60- Ω and 120- Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	-10 to +40	%
25- Ω R _{S_left_shift}	Internal left shift series termination with calibration (25- Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

OCT Without Calibration Resistance Tolerance Specifications

Table 1-9: OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

This table lists the Arria V OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	ResistanceTolerance			Unit
			-I3, -C4	-I5, -C5	-C6	
25- Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
25- Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
25- Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
50- Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
50- Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
50- Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
100- Ω R _D	Internal differential termination (100- Ω setting)	V _{CCIO} = 2.5	±25	±40	±40	%

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	—	—	—

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	$I_{OL}^{(14)}$ (mA)	$I_{OH}^{(14)}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽¹⁵⁾	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	⁽¹⁵⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

⁽¹⁵⁾ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Interface speed (PMA direct mode)	50	153.6 ⁽⁵⁶⁾ , 161 ⁽⁵⁷⁾	MHz
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

Related Information

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36

⁽⁵⁶⁾ The maximum frequency when core transceiver local routing is selected.

⁽⁵⁷⁾ The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

Table 1-34: Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
	SRIO_6250_SR	6,250
	SRIO_6250_MR	6,250
	SRIO_6250_LR	6,250

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–3 speed grade	5	—	800 ⁽⁶¹⁾	MHz
		–4 speed grade	5	—	800 ⁽⁶¹⁾	MHz
		–5 speed grade	5	—	750 ⁽⁶¹⁾	MHz
		–6 speed grade	5	—	625 ⁽⁶¹⁾	MHz
f_{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	—	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	—	50	—	160	MHz
$f_{VCO}^{(62)}$	PLL voltage-controlled oscillator (VCO) operating range	–3 speed grade	600	—	1600	MHz
		–4 speed grade	600	—	1600	MHz
		–5 speed grade	600	—	1600	MHz
		–6 speed grade	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	–3 speed grade	—	—	500 ⁽⁶³⁾	MHz
		–4 speed grade	—	—	500 ⁽⁶³⁾	MHz
		–5 speed grade	—	—	500 ⁽⁶³⁾	MHz
		–6 speed grade	—	—	400 ⁽⁶³⁾	MHz

⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter κ value. Therefore, if the counter κ has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{CASC_OUTPJ_DC}}^{(67)(71)}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	—	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	$f_{\text{INPFD}} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

- Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
- Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C5, –I5, –C6	320	1,600	MHz
	–C4	320	1,850	MHz
	–I3	320	2,100	MHz

HPS PLL Input Clock Range

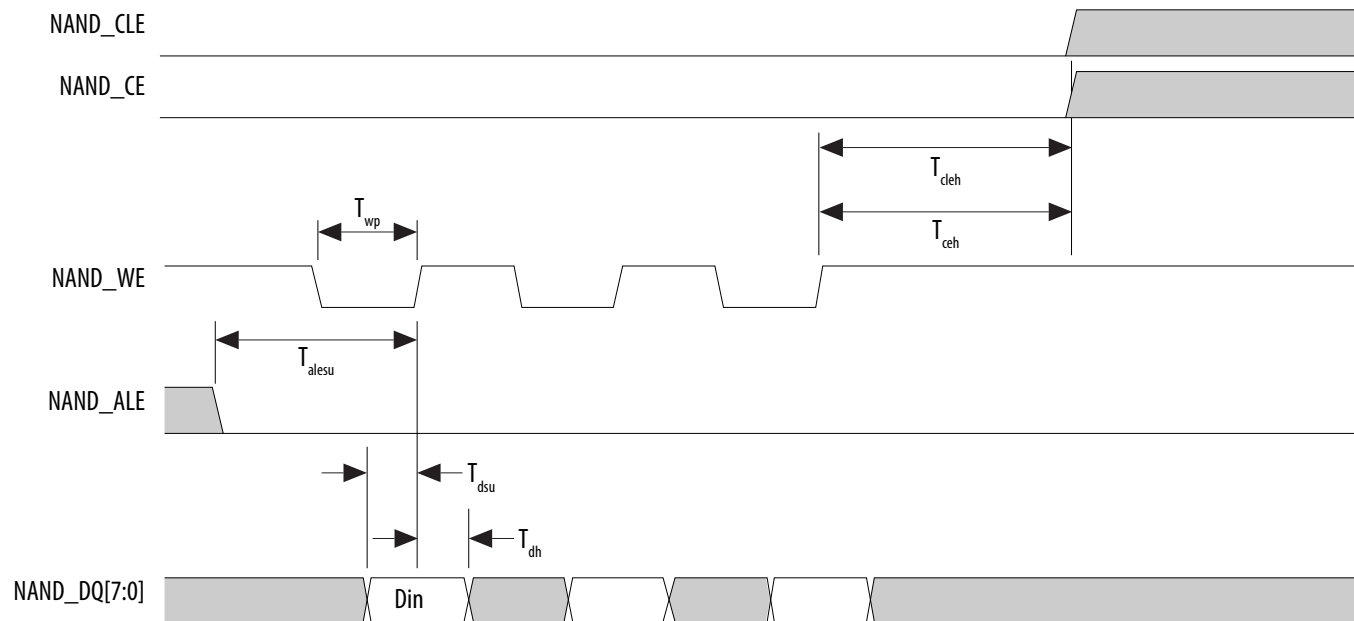
The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

[Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

Figure 1-19: NAND Data Write Timing Diagram



Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS $\times 1$ and $\times 4$ Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding $nSTATUS$ low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
Arria V GT	C3	71,015,712	439,960
	C7	101,740,800	446,360
	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SX	B3	185,903,680	450,968
	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.

Term	Definition
JTAG timing specifications	<p>JTAG Timing Specifications</p> <p>The diagram illustrates the timing requirements for JTAG signals. It shows four signals: TMS, TDI, TCK, and TDO. TMS and TDI are high during the first two clock cycles and low during the next two. TCK is a periodic clock signal. TDO is high during the first two clock cycles and low during the next two. Various timing parameters are indicated: t_{JCP} (TCK high pulse width), t_{JCH} (TCK high setup time), t_{JCL} (TCK high hold time), t_{JPSU} (TCK high setup time for TDO), t_{JPH} (TCK high hold time for TDO), t_{JPZX} (TDO setup time), t_{JPCO} (TDO hold time), and t_{JPXZ} (TDO output delay).</p>

Date	Version	Changes
June 2015	2015.06.16	<ul style="list-style-type: none"> Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table: <ul style="list-style-type: none"> True RSDS output standard: data rates of up to 360 Mbps True mini-LVDS output standard: data rates of up to 400 Mbps Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported. Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash. Updated T_h location in I²C Timing Diagram. Updated T_{wp} location in NAND Address Latch Timing Diagram. Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table. Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS $\times 1$ and $\times 4$ Configurations in Arria V Devices table. Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter. <ul style="list-style-type: none"> FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1 FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1 AS Configuration Timing Waveform PS Configuration Timing Waveform

Date	Version	Changes
August 2013	3.5	<ul style="list-style-type: none">Removed “Pending silicon characterization” note in Table 29.Updated Table 25.
August 2013	3.4	<ul style="list-style-type: none">Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64.Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29.
June 2013	3.3	Updated Table 20, Table 21, Table 25, and Table 38.
May 2013	3.2	<ul style="list-style-type: none">Added Table 37.Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23.Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64.Updated industrial junction temperature range for –I3 speed grade in “PLL Specifications” section.
March 2013	3.1	<ul style="list-style-type: none">Added HPS reset information in the “HPS Specifications” section.Added Table 60.Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59.Updated Figure 21.

Date	Version	Changes
November 2012	3.0	<ul style="list-style-type: none"> Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: <ul style="list-style-type: none"> Added “HPS Specifications” section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5.
October 2012	2.4	<ul style="list-style-type: none"> Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	<ul style="list-style-type: none"> Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4.

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.2 V	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.2 V	±50	±50	%
100-Ω R _D	Internal differential termination (100-Ω setting)	V _{CCIO} = 2.5 V	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{\text{OCT}} = R_{\text{SCAL}} \left(1 + \left(\frac{dR}{dT} \times \Delta T \right) \pm \left(\frac{dR}{dV} \times \Delta V \right) \right)$$

Notes:

1. The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
2. R_{SCAL} is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
5. dR/dT is the percentage change of R_{SCAL} with temperature.
6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Typical VOD Settings

Table 2-32: Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical	0 ⁽¹⁶⁶⁾	0	32	640
	1 ⁽¹⁶⁶⁾	20	33	660
	2 ⁽¹⁶⁶⁾	40	34	680
	3 ⁽¹⁶⁶⁾	60	35	700
	4 ⁽¹⁶⁶⁾	80	36	720
	5 ⁽¹⁶⁶⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920

⁽¹⁶⁶⁾ If TX termination resistance = 100 Ω , this VOD setting is illegal.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - f_{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197)	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(198)	—	(200)	(198)	—	(200)	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

(192) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

(195) Requires package skew compensation with PCB trace length.

(196) Do not mix single-ended I/O buffer within LVDS I/O bank.

(197) Chip-to-chip communication only with a maximum load of 5 pF.

(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁰⁵⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁰⁶⁾	μs
t _{CF2CK} (207)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} ⁽²⁰⁷⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CL}	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CLK}	DCLK period	$1/f_{\text{MAX}}$	—	s
f _{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²⁰⁸⁾	175	437	μs

⁽²⁰⁵⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²⁰⁶⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²⁰⁷⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.