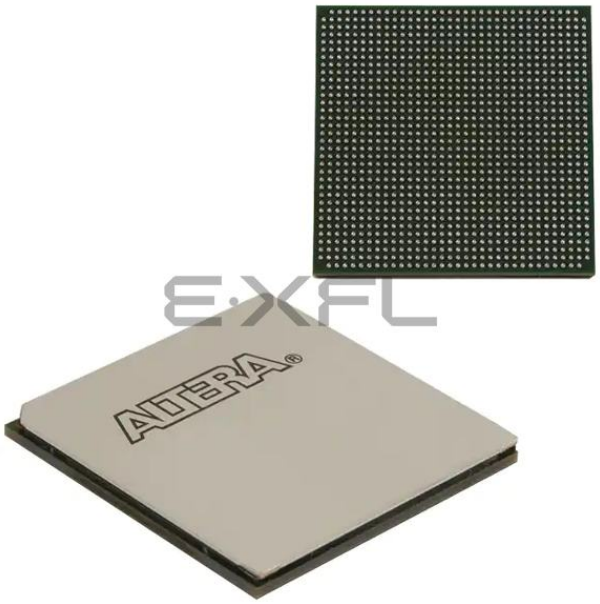

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	16980
Number of Logic Elements/Cells	360000
Total RAM Bits	23946240
Number of I/O	414
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme3h2f35c3n

I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[14] (mA)	I_{OH}[14] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO}+ 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[15]	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	[15]	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

(14) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

(15) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[16]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[17]			V_{OCM} (V)[17][18]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.														
2.5 V LVDS[19]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 1.25 Gbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} >$ 1.25 Gbps	1.55						
RSDS (HIO)[20]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)[21]	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL[22]	—	—	—	300	—	—	0.60	$D_{MAX} \leq$ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	$D_{MAX} >$ 700 Mbps	1.60						

Related Information

- **Transceiver Specifications for Arria V GX and SX Devices** on page 1-23
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

(16) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
(17) R_L range: $90 \leq R_L \leq 110\ \Omega$.
(18) This applies to default pre-emphasis setting only.
(19) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.
(20) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.
(21) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.
(22) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	75	—	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS							
Data rate[28]	—	611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin[29]	—	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	V

(28) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
(29) The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew[55]	×*N* PMA bonded mode	—	—	500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

[55] This specification is only applicable to channels on one side of the device across two transceiver banks.

Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Interface speed (PMA direct mode)	50	153.6[56], 161[57]	MHz
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

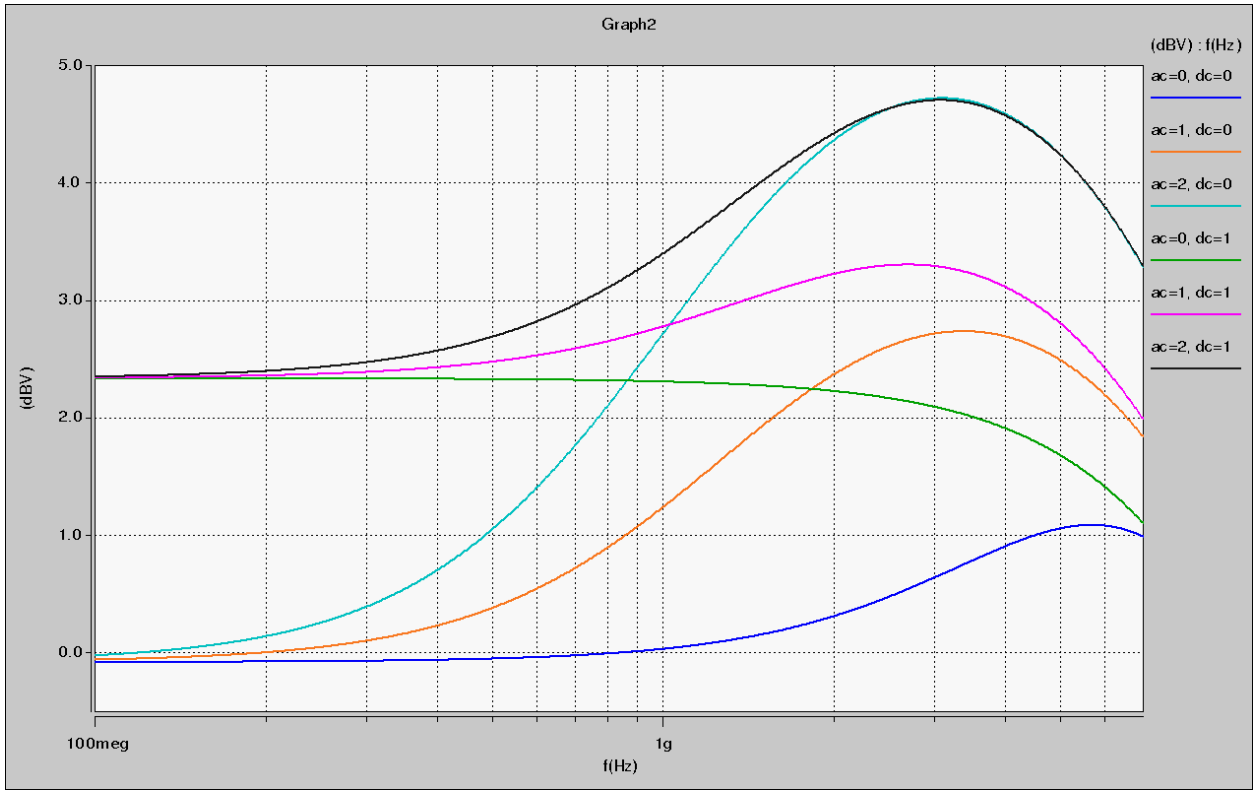
Related Information

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-35
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-36

[56] The maximum frequency when core transceiver local routing is selected.
[57] The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

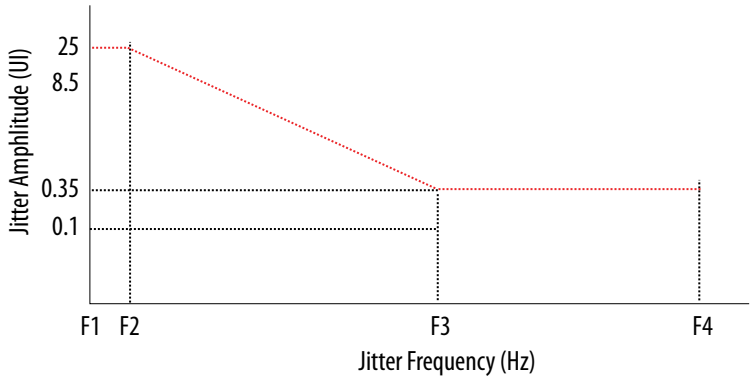
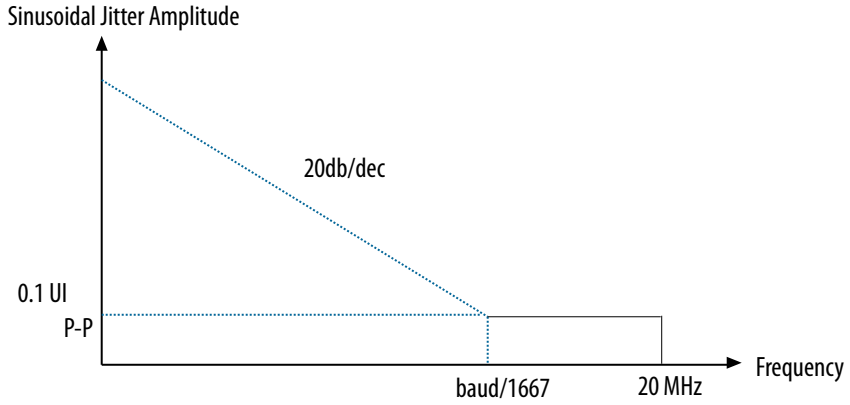


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	–I3, –C4	–I5, –C5	–C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	–C6	Unit
2	40	80	80	ps

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

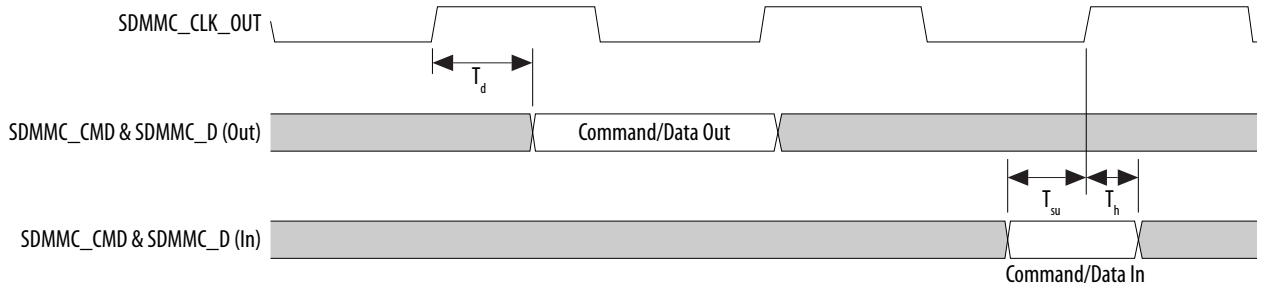
Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (85)	ns

Figure 1-11: SD/MMC Timing Diagram



Related Information

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual
Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

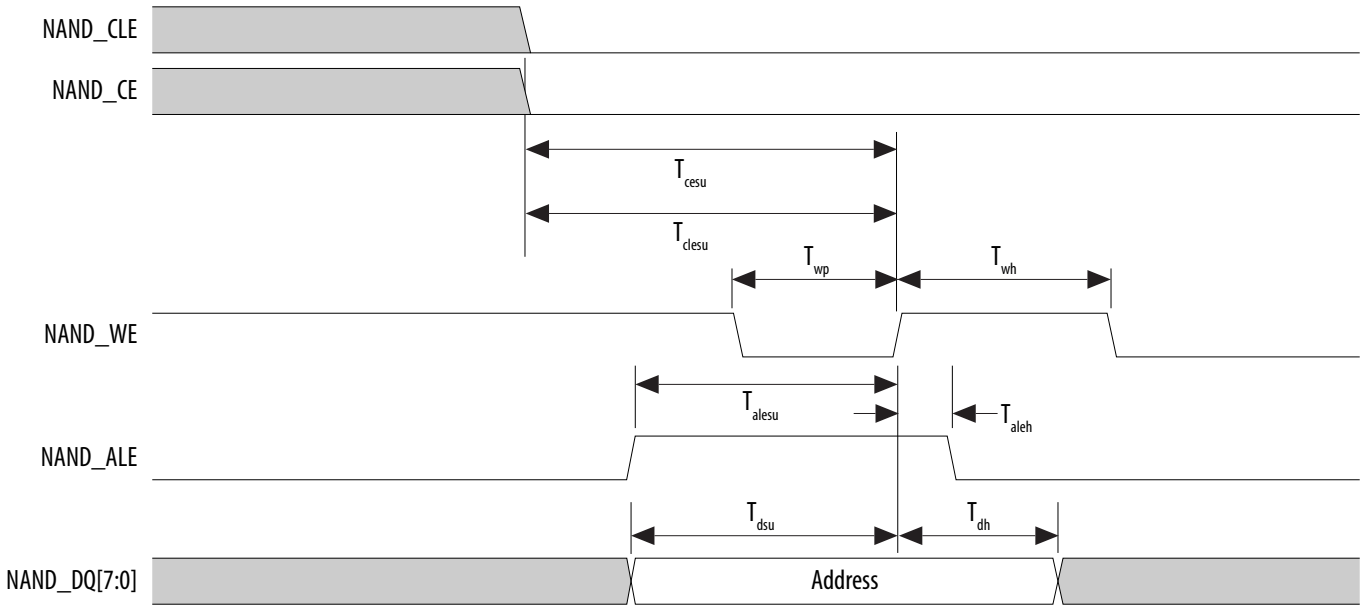
USB Timing Characteristics

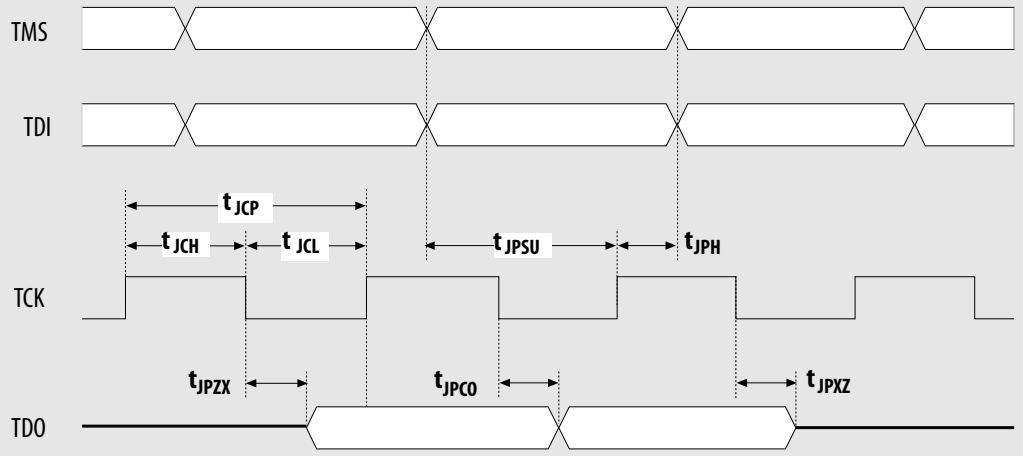
PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 1-18: NAND Address Latch Timing Diagram



Term	Definition
JTAG timing specifications	JTAG Timing Specifications 

Symbol	Description	Condition	Minimum[114]	Typical	Maximum [114]	Unit
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} [116]	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V_{CCBAT} [117]	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(116) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(117) If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-125 Class I, II	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-12 Class I, II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data rate range	VCO post-divider L = 2	8000	—	12500	8000	—	10312.5	Mbps
	L = 4	4000	—	6600	4000	—	6600	Mbps
	L = 8 (155)	2000	—	3300	2000	—	3300	Mbps
$t_{pll\_powerdown}$ (156)	—	1	—	—	1	—	—	µs
t_{pll_lock} (157)	—	—	—	10	—	—	10	µs

Related Information

- **Arria V Device Overview**
  For more information about device ordering codes.
- **Transceiver Clocking in Arria V Devices**
  For more information about clocking ATX PLLs.
- **Dynamic Reconfiguration in Arria V Devices**
  For more information about reconfiguring ATX PLLs.

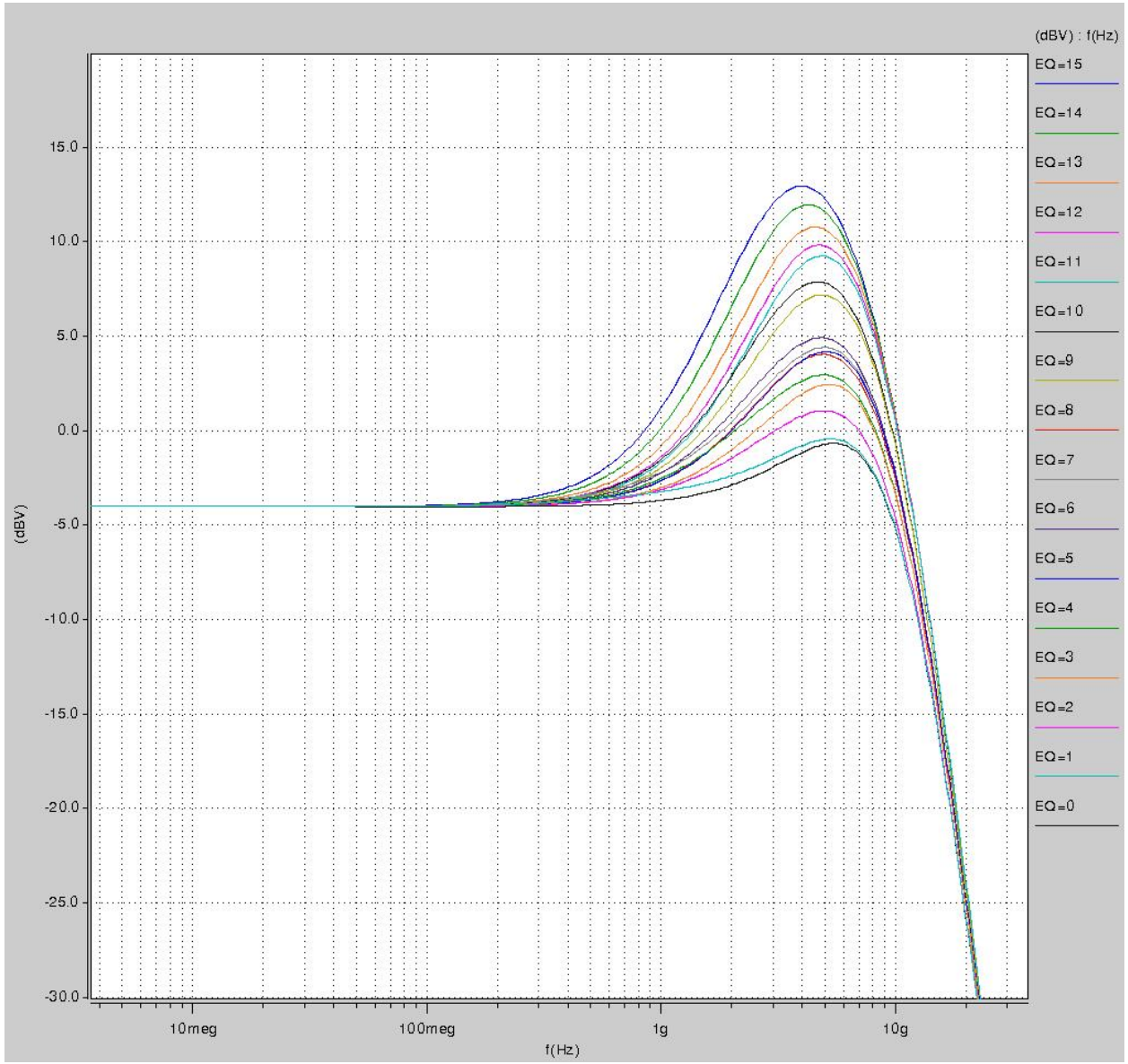
Fractional PLL

Table 2-28: Fractional PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(155) This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the Transceiver Clocking in Arria V Devices chapter and the Dynamic Reconfiguration in Arria V Devices chapter.
(156) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.
(157) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Figure 2-2: AC Gain Curves for Arria V GZ Channels (full bandwidth)



Symbol	Parameter	Min	Typ	Max	Unit
k_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency (f_{INPFD} = 100 MHz)	390625	5.96	0.023	Hz

Related Information

- **Duty Cycle Distortion (DCD) Specifications** on page 2-56
- **DLL Range Specifications** on page 2-53

DSP Block Specifications

Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mode	Performance			Unit
	C3, I3L	C4	I4	
Modes using One DSP Block				
Three 9 × 9	480	420		MHz
One 18 × 18	480	420	400	MHz
Two partial 18 × 18 (or 16 × 16)	480	420	400	MHz
One 27 × 27	400	350		MHz
One 36 × 18	400	350		MHz
One sum of two 18 × 18 (One sum of two 16 × 16)	400	350		MHz
One sum of square	400	350		MHz
One 18 × 18 plus 36 (a × b) + c	400	350		MHz
Modes using Two DSP Blocks				
Three 18 × 18	400	350		MHz
One sum of four 18 × 18	380	300		MHz

Related Information

- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V Devices Documentation page
For the Excel-based I/O Timing spreadsheet

(226) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(227) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Date	Version	Changes

June 2016	2016.06.20	• Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table.
		• Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table.
		• Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table:
		  • True RSDS output standard: data rates of up to 230 Mbps
		  • True mini-LVDS output standard: data rates of up to 340 Mbps

December 2015	2015.12.16	• Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table. • Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table. • Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table. • Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table.
June 2015	2015.06.16	• Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table. • Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table.
January 2015	2015.01.30	• Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table. • Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table. • Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table.