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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	18870
Number of Logic Elements/Cells	400000
Total RAM Bits	34322432
Number of I/O	534
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme5h2f35c3n

Caution: Conditions outside the range listed in the following table may cause permanent damage tothe device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	–0.50	1.43	V
V_{CCP}	Periphery circuitry, PCIe® hardIP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.50	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.50	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO}	I/O power supply	–0.50	3.90	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V_{CCA_FPLL}	PLL analog power supply	–0.50	3.25	V
V_{CCA_GXB}	Transceiver high voltage power	–0.50	3.25	V
V_{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V_{CCR_GXB}	Receiver power	–0.50	1.50	V
V_{CCT_GXB}	Transmitter power	–0.50	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.50	1.50	V
V_I	DC input voltage	–0.50	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.50	3.90	V

Symbol	Description	Maximum	Unit
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Condition (V)[11]	Value[12]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

(10) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

(11) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(12) Valid with ±10% tolerances to cover changes over PVT.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew[55]	×*N* PMA bonded mode	—	—	500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

[55] This specification is only applicable to channels on one side of the device across two transceiver banks.

Protocol	Sub-protocol	Data Rate (Mbps)
SONET	SONET 155	155.52
	SONET 622	622.08
	SONET 2488	2,488.32
Gigabit-capable passive optical network (GPON)	GPON 155	155.52
	GPON 622	622.08
	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

Parameter	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

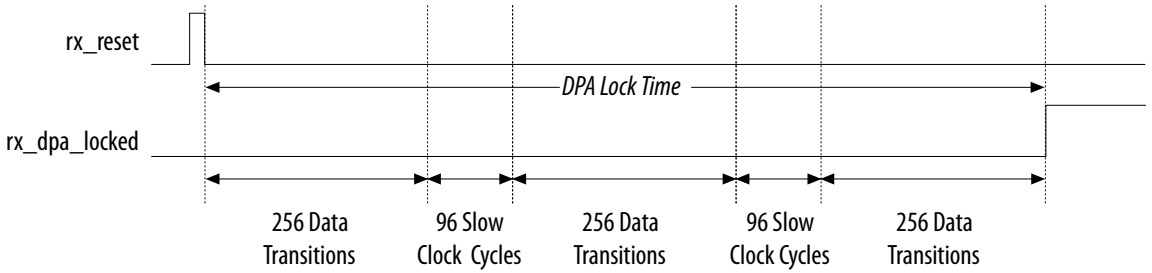


Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(84)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

(84) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

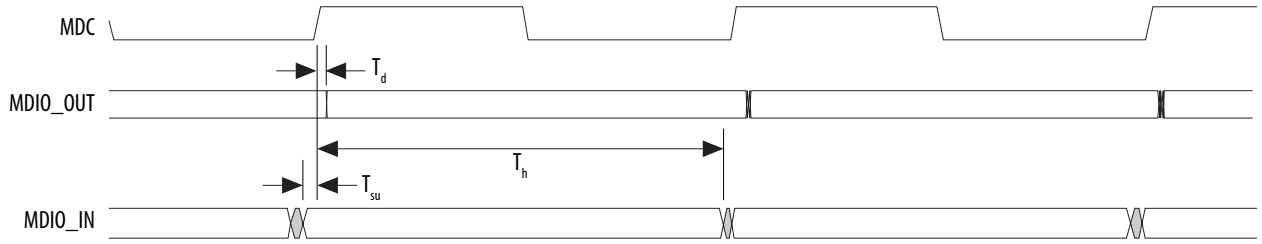
Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (85)	ns

Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Related Information

- **PS Configuration Timing** on page 1-81
- **AS Configuration Timing**
  Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 1-69: DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

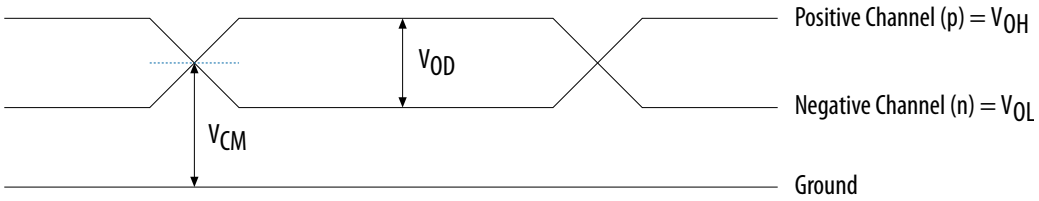
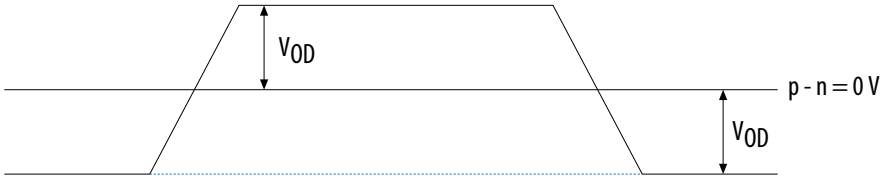
Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

PS Configuration Timing

Table 1-70: PS Timing Parameters for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(103)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(104)	µs

(103) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(104) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

Term	Definition
	Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ =1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

Term	Definition
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/ (Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
$V_{CM(DC)}$	DC common mode input voltage.
V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage

Date	Version	Changes
June 2012	2.0	• Updated for the Quartus II software v12.0 release: • Restructured document. • Updated "Supply Current and Power Consumption" section. • Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. • Added Table 22, Table 23, and Table 33. • Added Figure 1–1 and Figure 1–2. • Added "Initialization" and "Configuration Files" sections.
February 2012	1.3	• Updated Table 2–1. • Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. • Updated V_{CCP} description.
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	• Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. • Added Table 2–5. • Added Figure 2–4.
August 2011	1.0	Initial release.

Symbol	Description	Minimum [118]	Typical	Maximum [118]	Unit
V_{CCR_GXBL} [121]	Receiver analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCR_GXBR} [121]	Receiver analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCT_GXBL} [121]	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCT_GXBR} [121]	Transmitter analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V

(118) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(121) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-125 Class I, II	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-12 Class I, II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (146)	V_{CCR_GXB} = 1.0 V (V_{ICM} = 0.75 V)	—	—	1.8	—	—	1.8	V
	V_{CCR_GXB} = 0.85 V (V_{ICM} = 0.6 V)	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins (147)(148)	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85–Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100–Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120–Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150–Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	Ω

(146) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(147) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(148) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{pll\_powerdown}$ (153)	—	1	—	—	1	—	—	µs
t_{pll_lock} (154)	—		—	10	—	—	10	µs

Related Information

Arria V Device Overview

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(153) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(154) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	3250/ 3125(158)	600	—	3250/ 3125 (158)	Mbps
$t_{pll\_powerdown}$ (159)	—	1	—	—	1	—	—	µs
t_{pll_lock} (160)	—	—	—	10		—	10	µs

Related Information

Arria V Device Overview
For more information about device ordering codes.

Clock Network Data Rate

Table 2-29: Clock Network Maximum Data Rate Transmitter Specifications

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

Clock Network	ATX PLL			CMU PLL (161)			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 (162)	12.5	—	6	12.5	—	6	3.125	—	3
x6 (162)	—	12.5	6	—	12.5	6	—	3.125	6
x6 PLL Feedback (163)	—	12.5	Side-wide	—	12.5	Side-wide	—	—	—

(158) When you use fPLL as a TXPLL of the transceiver.
(159) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.
(160) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
(161) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
(162) Channel span is within a transceiver bank.
(163) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Mode	Performance			Unit
	C3, I3L	C4	I4	
One sum of two 27 × 27	380	300	290	MHz
One sum of two 36 × 18	380	300		MHz
One complex 18 × 18	400	350		MHz
One 36 × 36	380	300		MHz
Modes using Three DSP Blocks				
One complex 18 × 25	340	275	265	MHz
Modes using Four DSP Blocks				
One complex 27 × 27	350	310		MHz

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Memory	C3	C4	I3L	I4	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

(178) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
DPA run length	—	—	—	10000	—	—	10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled

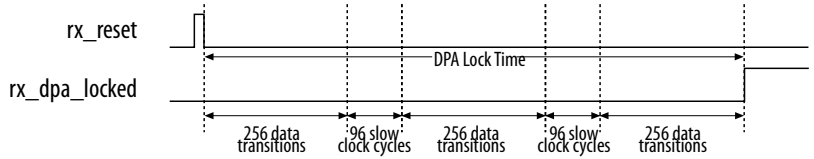


Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

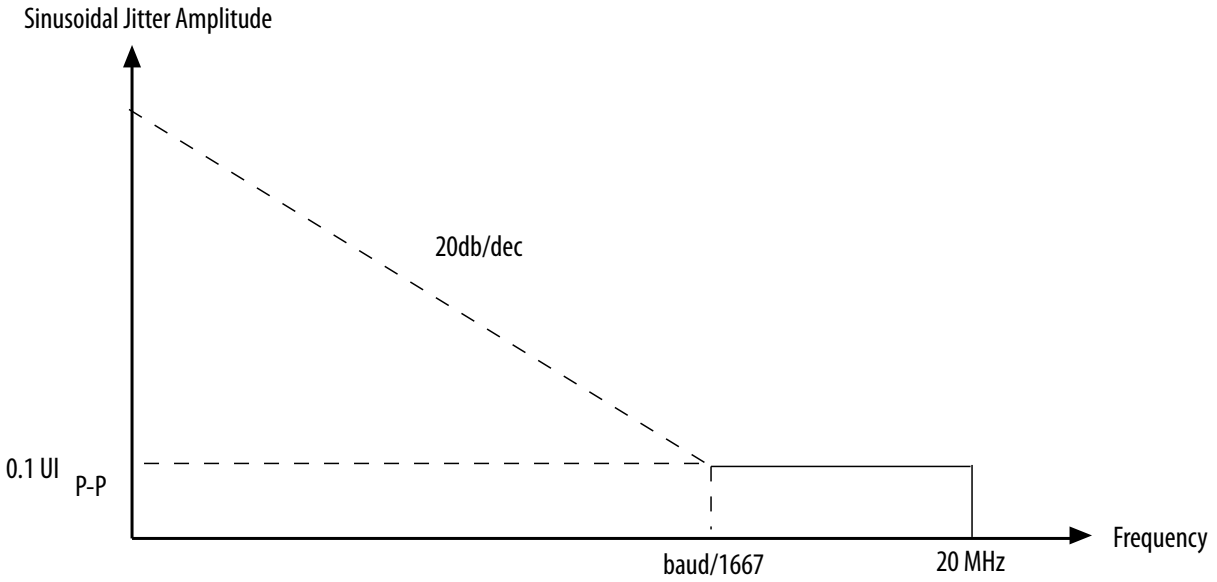
One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (201)	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions

(201) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



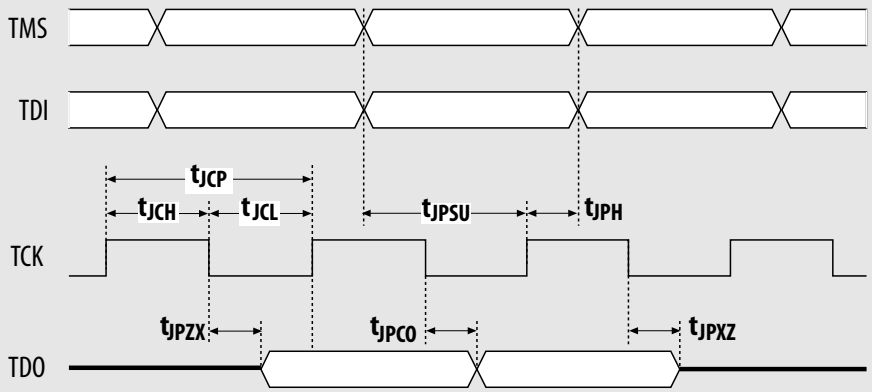
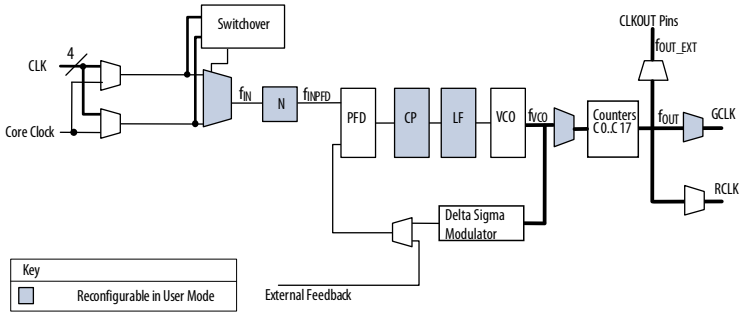
Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sampling Window	—	—	—	300	—	—	300	ps

Term	Definition
JTAG Timing Specifications	JTAG Timing Specifications: 
PLL Specifications	Diagram of PLL Specifications  Note: 1. Core Clock can only be fed by dedicated clock input pins or PLL outputs.