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Intel - 5AGZME5H3F35I4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	18870
Number of Logic Elements/Cells	400000
Total RAM Bits	34322432
Number of I/O	534
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme5h3f35i4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1-4 Recommended Operating Conditions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
Vi (AC)	AC input voltage	4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.



Transceiver Power Supply Operating Conditions

Table '	1-4:	Transceiver	Power S	upply	Operating	Conditions	for Arria V Devices	j
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Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2 275	2 500	2 625	V
V _{CCA_GXBR}	Transceiver high voltage power (right side)	2.575	2.300	2.025	v
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)	1.00/1.12	1.1/1.13	1.14/1.10	v
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1 17	1 20	1 23	V
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)	1.17	1.20	1.23	v
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)	1.00/1.12	1.1/1.15	1.14/1.10	v
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1 17	1 20	1 23	V
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)	1.17	1.20	1.23	v
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1 /25	1 500	1 575	V
V _{CCH_GXBR}	Transmitter output buffer power (right side)	1.423	1.300	1.375	v

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate <=3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.



I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Тур	Max	Unit
II	Input pin	$V_{I} = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I _{OZ}	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30		30	μΑ

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

								V _{CCI}	₀ (V)						
Parameter	Symbol	Condition	1.	.2	1	.5	1	.8	2	.5	3.	.0	3	.3	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max)	8	_	12		30	_	50		70		70		μΑ
Bus-hold, high, sustaining current	I _{SUSH}	V _{IN} < V _{IH} (min)	-8	_	-12		-30	_	-50		-70	_	-70		μΑ
Bus-hold, low, overdrive current	I _{ODL}	$\begin{array}{c} 0 \ \mathrm{V} < \mathrm{V_{IN}} \\ < \mathrm{V_{CCIO}} \end{array}$		125	_	175	_	200		300		500	_	500	μΑ
Bus-hold, high, overdrive current	I _{ODH}	0 V <v<sub>IN <v<sub>CCIO</v<sub></v<sub>	_	-125	_	-175	_	-200		-300	_	-500	_	-500	μΑ

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



								V _{CCI}	₀ (V)						
Parameter	Symbol	Condition	1	.2	1	.5	1	.8	2	.5	3	.0	3	.3	Unit
			Min	Мах	Min	Max	Min	Max	Min	Мах	Min	Max	Min	Max	
Bus-hold trip point	V _{TRIP}	_	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (\/)	Ca	alibration Accura	су	Unit
Symbol	Description		–I3, –C4	–I5, –C5	-C6	Ont
25-Ω R _S	Internal series termination with calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80- Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , and 80- Ω setting)	$V_{CCIO} = 1.2$	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50- Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2	-10 to +40	-10 to +40	-10 to +40	%
20- Ω , 30- Ω , 40- Ω ,60- Ω , and 120- Ω R _T	Internal parallel termination with calibration (20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25	-10 to +40	-10 to +40	-10 to +40	%



Symbol	Description	Maximum	Unit
I _{XCVR-RX (DC)}	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Condition (V) ⁽¹¹⁾	Value ⁽¹²⁾	Unit
		$V_{CCIO} = 3.3 \pm 5\%$	25	kΩ
		$V_{CCIO} = 3.0 \pm 5\%$	25	kΩ
		$V_{CCIO} = 2.5 \pm 5\%$	25	kΩ
D	Value of the I/O pin pull-up resistor before and during	$V_{CCIO} = 1.8 \pm 5\%$	25	kΩ
кру	programmable pull-up resistor option.	$V_{CCIO} = 1.5 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.35 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.25 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.2 \pm 5\%$	25	kΩ

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.



⁽¹⁰⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

 $^{^{(11)}}$ Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

⁽¹²⁾ Valid with $\pm 10\%$ tolerances to cover changes over PVT.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

I/O Standard		V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)	
i/O Stanuaru	Min	Тур	Max	Min	Тур	Мах	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	V _{REF} - 0.04	V _{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95		V _{CCIO} /2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9		V _{CCIO} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$		V _{CCIO} /2	_
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	_		

Tuble 1 15, Single Ended SSTE, 15TE, and 15OE / O hererence voltage Specifications for Anna v Devices



Symbol/Description	Condition ·	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Тур	Max	Min	Тур	Max	Onit
Inter-transceiver block transmitter channel-to- channel skew ⁽³⁹⁾	×N PMA bonded mode			500		_	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver S	peed Grade 6	Unit	
	Min	Мах	Min	Мах	Ont	
Supported data range	611	6553.6	611	3125	Mbps	
fPLL supported data range	611	3125	611	3125	Mbps	

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Spee	ed Grade 4 and 6	Unit	
Symbol Description	Min	Max		
Interface speed (single-width mode)	25	187.5	MHz	
Interface speed (double-width mode)	25	163.84	MHz	

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 1-35
- CTLE Response at Data Rates \leq 3.25 Gbps across Supported AC Gain and DC Gain on page 1-36
- Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines Provides more information about the power supply connection for different data rates.



⁽³⁹⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.

Symbol/Description	Condition	Tran	Unit		
Symbol Description	Condition	Min	Тур	Max	Onic
	10 Hz	_	_	-50	dBc/Hz
	100 Hz			-80	dBc/Hz
	1 KHz			-110	dBc/Hz
Hansmitter REPCLK phase hoise	10 KHz			-120	dBc/Hz
	100 KHz			-120	dBc/Hz
	≥1 MHz			-130	dBc/Hz
R _{REF}	_		2000 ±1%		Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Tran	Unit			
Symbol/Description	Condition	Min	Тур	Max	onit	
fixedclk clock frequency	PCIe Receiver Detect	_	125		MHz	
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz	

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	T	Unit				
Symbol/Description	Condition	Min	Тур	Мах	Onit		
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS						
Data rate (6-Gbps transceiver) ⁽⁴⁴⁾	_	611		6553.6	Mbps		

⁽⁴³⁾ The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10⁻¹², equivalent to 14 sigma.



⁽⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Protocol	Sub-protocol	Data Rate (Mbps)
	SONET 155	155.52
SONET	SONET 622	622.08
	SONET 2488	2,488.32
	GPON 155	155.52
Gigabit-canable passive optical network (GPON)	GPON 622	622.08
Gigable-capable passive optical network (GI OIV)	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

Paramotor		Unit		
Farameter	-I3, -C4	–I5, –C5	-C6	omt
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.



Figure 1-10: SPI Slave Timing Diagram



Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses drvsel = 3 and smplsel = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock SDMMC_CLK_OUT changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock SDMMC_CLK and the CSEL setting. The value of SDMMC_CLK is based on the external oscillator frequency and has a maximum value of 50 MHz.



Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Unit
T _{clk} (1000Base-T)	RX_CLK clock period		8	ns
T _{clk} (100Base-T)	RX_CLK clock period		40	ns
T _{clk} (10Base-T)	RX_CLK clock period		400	ns
T _{su}	RX_D/RX_CTL setup time	1		ns
T _h	RX_D/RX_CTL hold time	1		ns

Figure 1-14: RGMII RX Timing Diagram



Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk}	MDC clock period	—	400	_	ns
T _d	MDC to MDIO output data delay	10		20	ns
T _s	Setup time for MDIO data	10	_		ns
T _h	Hold time for MDIO data	0			ns



		Active Serial ⁽¹⁰⁸⁾			Fast Passive Parallel ⁽¹⁰⁹⁾		
Variant	Member Code	Width	DCLK (MHz)	Minimum Configura- tion Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
Arria V CV	A7	4	100	255	16	125	51
Arna v GA	B1	4	100	344	16	125	69
	В3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
	C3	4	100	178	16	125	36
Amia V CT	C7	4	100	255	16	125	51
Allia v GI	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SV	В3	4	100	465	16	125	93
AIIIa V SA	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
Arria V ST	D5	4	100	465	16	125	93

Related Information Configuration Files on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.
 (109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



2-2 Absolute Maximum Ratings

Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade					
Transceiver speed Grade	C3	C4	I3L	14		
2	Yes	_	Yes	_		
3		Yes		Yes		

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V



Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit	
	Receiver analog power supply (left side)	0.82	0.85	0.88		
V _{CCR_GXBL} ⁽¹²¹⁾		0.97	1.0	1.03	V	
		1.03	1.05	1.07		
		0.82	0.85	0.88		
V _{CCR_GXBR} ⁽¹²¹⁾	Receiver analog power supply (right side)	0.97	1.0	1.03	V	
		1.03	1.05	1.07		
V _{CCT_GXBL} ⁽¹²¹⁾	Transmitter analog power supply (left side)	0.82	0.85	0.88		
		0.97	1.0	1.03	V	
		1.03	1.05	1.07		
		0.82	0.85	0.88		
V _{CCT_GXBR} ⁽¹²¹⁾	Transmitter analog power supply (right side)	0.97	1.0	1.03	V	
		1.03	1.05	1.07		
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V	
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V	



⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Symbol	Description	V _{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	
		2.5	0.0344	
		1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	
		2.5	0.208	
		1.8	0.266	%/°C
		1.5	0.273	
		1.2	0.317	

Pin Capacitance

Table 2-13: Pin Capacitance for Arria V GZ Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF



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Sumbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description		Min	Тур	Max	Min	Тур	Max	Onic
	100 Hz	—	_	-70		—	-70	dBc/Hz
	1 kHz		—	-90		—	-90	dBc/Hz
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁴¹⁾	10 kHz		—	-100		—	-100	dBc/Hz
,	100 kHz		—	-110		—	-110	dBc/Hz
	≥1 MHz		—	-120	_	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁴²⁾	10 kHz to 1.5 MHz (PCIe)	_	_	3		_	3	ps (rms)
R _{REF}	_		1800 ±1%			1800 ±1%		Ω

Related Information

Arria V Device Overview

For more information about device ordering codes.

Transceiver Clocks

Table 2-23: Transceiver Clocks Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Arria V GZ Device Datasheet

Altera Corporation



 $^{^{(141)}}$ To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20 *log(f/622).

⁽¹⁴²⁾ To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.

Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to istatus low		600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (205)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high		1,506 (206)	μs
t _{CF2CK} (207)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} ⁽²	hstatus high to first rising edge of DCLK	2	_	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45 imes 1/f_{ m MAX}$	_	s
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	_	s
t _{CLK}	DCLK period	1/f _{MAX}	_	s
f	DCLK frequency (FPP ×8/×16)	_	125	MHz
¹ MAX	DCLK frequency (FPP ×32)		100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²⁰⁸⁾	175	437	μs

⁽²⁰⁵⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽²⁰⁶⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²⁰⁷⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing



Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Notes:

1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and ERCQ sends in 4-bits of data for each DCLKcycle.

2. The initialization clock can be from internal oscillator or CLKUSR pin

3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE ges low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.



Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

- 1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
- 3. After power-up, before and during configuration, CONF_DONE is low.
- 4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
- 6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.



Related Information

- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reset_timer input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete placeand-route.

Related Information

Arria V Devices Documentation page

For the Excel-based I/O Timing spreadsheet

Arria V GZ Device Datasheet

Altera Corporation



⁽²²⁶⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²⁷⁾ This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.