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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	18870
Number of Logic Elements/Cells	400000
Total RAM Bits	34322432
Number of I/O	674
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme5k2f40c3n

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AV-51002



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This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

Related Information

[Arria V Device Overview](#)

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V _{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C
t _{RAMP} ⁽⁴⁾	Power supply ramp time	Standard POR	200 μs	—	100 ms	—
		Fast POR	200 μs	—	4 ms	—

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽⁴⁰⁾ , HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽⁴¹⁾	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽⁴¹⁾	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300 ⁽⁴²⁾ /2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	—	1.2	—	V
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

⁽⁴⁰⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.⁽⁴¹⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.⁽⁴²⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{OUT_EXT}}$	Output frequency for external clock output	–3 speed grade	—	—	670 ⁽⁶³⁾	MHz
		–4 speed grade	—	—	670 ⁽⁶³⁾	MHz
		–5 speed grade	—	—	622 ⁽⁶³⁾	MHz
		–6 speed grade	—	—	500 ⁽⁶³⁾	MHz
t_{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{\text{DYCONFIGCLK}}$	Dynamic configuration clock for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of <code>areset</code>	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High ⁽⁶⁴⁾	—	4	—	MHz
$t_{\text{PLL_PSERR}}$	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the <code>areset</code> signal	—	10	—	—	ns
$t_{\text{INCCJ}}^{(65)(66)}$	Input clock cycle-to-cycle jitter	$F_{\text{REF}} \geq 100 \text{ MHz}$	—	—	0.15	UI (p-p)
		$F_{\text{REF}} < 100 \text{ MHz}$	—	—	±750	ps (p-p)

⁽⁶⁴⁾ High bandwidth PLL settings are not supported in external feedback mode.⁽⁶⁵⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.⁽⁶⁶⁾ F_{REF} is f_{IN}/N , specification applies when $N = 1$.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{CASC_OUTPJ_DC}}^{(67)(71)}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	—	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	$f_{\text{INPFD}} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

[Memory Output Clock Jitter Specifications](#) on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

- Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
- Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When $J = 3$ to 10 , use the serializer/deserializer (SERDES) block. When $J = 1$ or 2 , bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	-I3, -C4			-I5, -C5			-C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards		Clock boost factor $W = 1$ to $40^{(72)}$	5	—	800	5	—	750	5	—	625	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single-Ended I/O Standards ⁽⁷³⁾		Clock boost factor $W = 1$ to $40^{(72)}$	5	—	625	5	—	625	5	—	500	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single-Ended I/O Standards ⁽⁷⁴⁾		Clock boost factor $W = 1$ to $40^{(72)}$	5	—	420	5	—	420	5	—	420	MHz
$f_{\text{HCLK_OUT}}$ (output clock frequency)		—	5	—	$625^{(75)}$	5	—	$625^{(75)}$	5	—	$500^{(75)}$	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor $J = 3$ to $10^{(76)}$	⁽⁷⁷⁾	—	1250	⁽⁷⁷⁾	—	1250	⁽⁷⁷⁾	—	1050	Mbps

⁽⁷²⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁷³⁾ This applies to DPA and soft-CDR modes only.

⁽⁷⁴⁾ This applies to non-DPA mode only.

⁽⁷⁵⁾ This is achieved by using the LVDS clock network.

⁽⁷⁶⁾ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁷⁷⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol	Condition	-I3, -C4			-I5, -C5			-C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor $J \geq 8^{(76)(78)}$, LVDS TX with RX DPA	⁽⁷⁷⁾	—	1600	⁽⁷⁷⁾	—	1500	⁽⁷⁷⁾	—	1250	Mbps
	SERDES factor $J = 1$ to 2, Uses DDR Registers	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate) ⁽⁸⁰⁾	SERDES factor $J = 4$ to $10^{(81)}$	⁽⁷⁷⁾	—	945	⁽⁷⁷⁾	—	945	⁽⁷⁷⁾	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate) ⁽⁸⁰⁾	SERDES factor $J = 4$ to $10^{(81)}$	⁽⁷⁷⁾	—	200	⁽⁷⁷⁾	—	200	⁽⁷⁷⁾	—	200	Mbps
$t_{\text{x jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

⁽⁷⁸⁾ The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

⁽⁷⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.

⁽⁸⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

⁽⁸¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smp1sel` via the system manager. `drvsel` can be set from 1 to 7 and `smp1sel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Max	Unit
$T_{\text{sdmmc_clk}}$ (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{\text{sdmmc_clk_out}}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{\text{duty cycle}}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	$(T_{\text{sdmmc_clk}} \times \text{drvsel})/2 - 1.23^{(87)}$	$(T_{\text{sdmmc_clk}} \times \text{drvsel})/2 + 1.69^{(87)}$	ns
T_{su}	Input setup time	$1.05 - (T_{\text{sdmmc_clk}} \times \text{smp1sel})/2^{(88)}$	—	ns
T_h	Input hold time	$(T_{\text{sdmmc_clk}} \times \text{smp1sel})/2^{(88)}$	—	ns

⁽⁸⁷⁾ `drvsel` is the drive clock phase shift select value.

⁽⁸⁸⁾ `smp1sel` is the sample clock phase shift select value.

Date	Version	Changes
November 2012	3.0	<ul style="list-style-type: none"> Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: <ul style="list-style-type: none"> Added “HPS Specifications” section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5.
October 2012	2.4	<ul style="list-style-type: none"> Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	<ul style="list-style-type: none"> Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V _{CCPD} ⁽¹¹⁶⁾	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V _{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V _{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V _{CCBAT} ⁽¹¹⁷⁾	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁶⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

⁽¹¹⁷⁾ If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
$V_{CCR_GXBL}^{(121)}$	Receiver analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCR_GXBR}^{(121)}$	Receiver analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCT_GXBL}^{(121)}$	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCT_GXBR}^{(121)}$	Transmitter analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{ICM} (AC and DC coupled)	$V_{CCR_GXB} = 0.85\text{ V}$ full bandwidth	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 0.85\text{ V}$ half bandwidth	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}$ full bandwidth	—	700	—	—	700	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}$ half bandwidth	—	700	—	—	700	—	mV
$t_{LTR}^{(149)}$	—	—	—	10	—	—	10	μs
$t_{LTD}^{(150)}$	—	4	—	—	4	—	—	μs
$t_{LTD_manual}^{(151)}$	—	4	—	—	4	—	—	μs
$t_{LTR_LTD_manual}^{(152)}$	—	15	—	—	15	—	—	μs
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	dB

⁽¹⁴⁹⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽¹⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.

⁽¹⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.

⁽¹⁵²⁾ $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto ref` signal goes high when the CDR is functioning in the manual mode.

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵³⁾	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}$ ⁽¹⁵⁴⁾	—		—	10	—	—	10	μs

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

⁽¹⁵³⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁴⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Clock Network	ATX PLL			CMU PLL ⁽¹⁶¹⁾			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

Standard PCS Data Rate

Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices

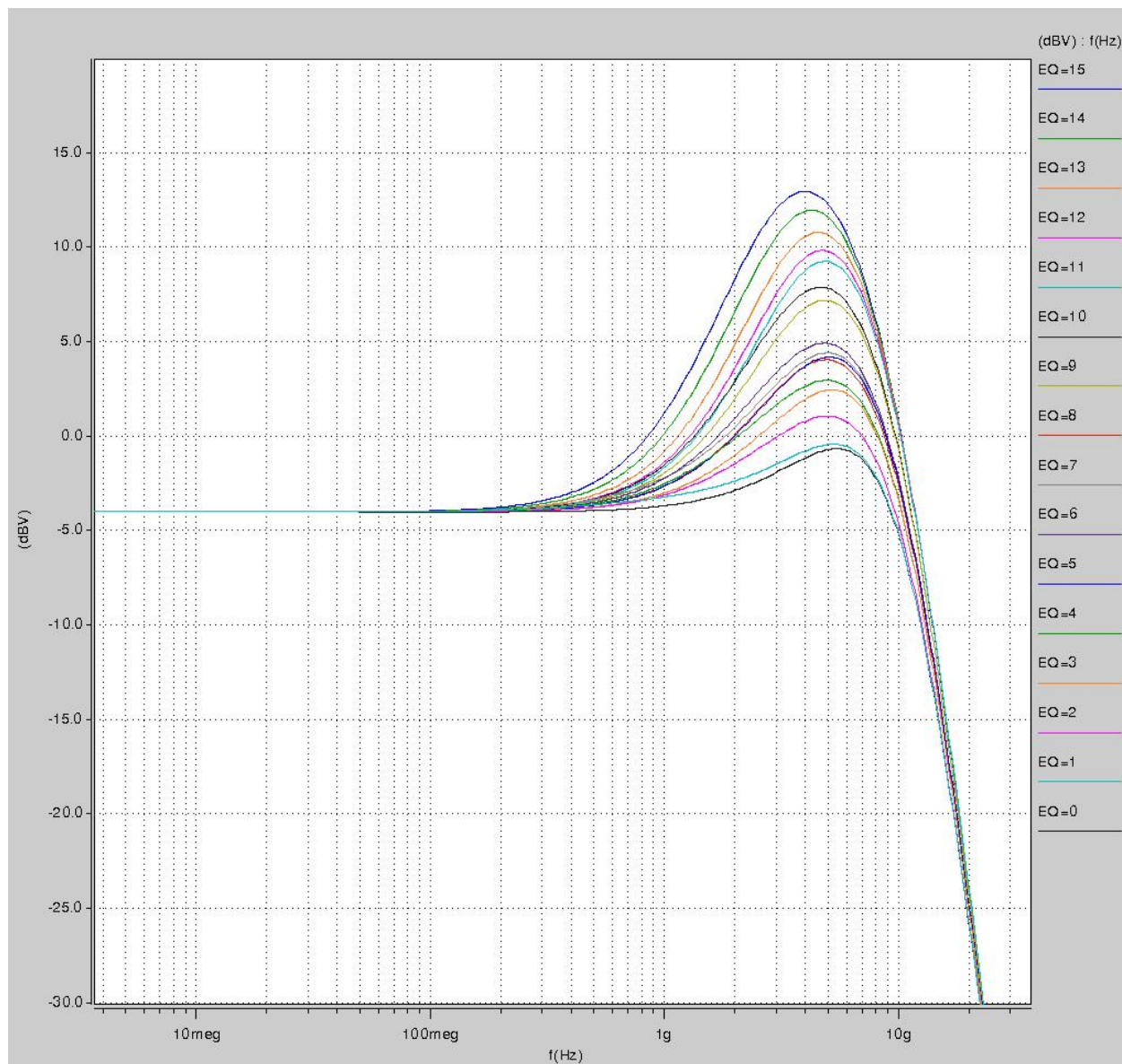
The maximum data rate is also constrained by the transceiver speed grade. Refer to the “Commercial and Industrial Speed Grade Offering for Arria V GZ Devices” table for the transceiver speed grade.

Mode ⁽¹⁶⁴⁾	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

⁽¹⁶¹⁾ ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

⁽¹⁶⁴⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Figure 2-2: AC Gain Curves for Arria V GZ Channels (full bandwidth)



Description	Min	Typ	Max	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor $J = 3$ to 10 (182), (183)	(184)	—	1250	(184)	—	1050	Mbps
	SERDES factor $J \geq 4$ LVDS TX with DPA (185), (186), (187), (188)	(184)	—	1600	(184)	—	1250	Mbps
	SERDES factor $J = 2$, uses DDR Registers	(184)	—	(189)	(184)	—	(189)	Mbps
	SERDES factor $J = 1$, uses SDR Register	(184)	—	(189)	(184)	—	(189)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (190)	SERDES factor $J = 4$ to 10 (191)	(184)	—	840	(184)	—	840	Mbps

(182) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(183) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(184) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(185) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(186) Requires package skew compensation with PCB trace length.

(187) Do not mix single-ended I/O buffer within LVDS I/O bank.

(188) Chip-to-chip communication only with a maximum load of 5 pF.

(189) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

(190) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(191) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

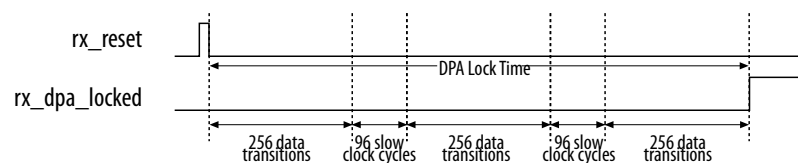
DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
DPA run length	—	—	—	10000	—	—	10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled**Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices**

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions

⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	4	ns
t_{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t_H	Data hold time after falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$	—	—

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

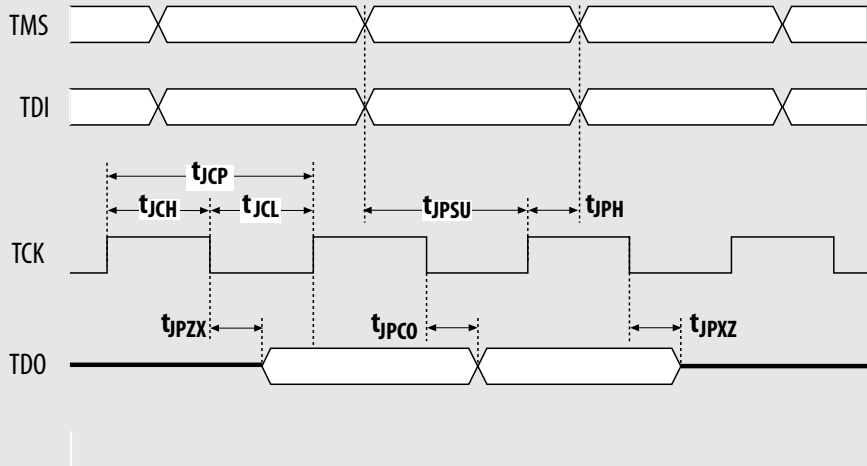
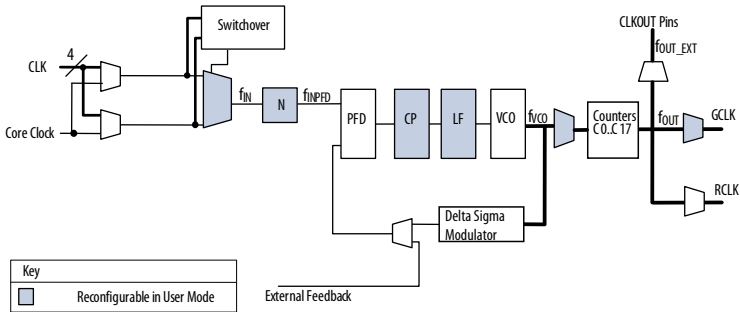
The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- [Passive Serial Configuration Timing](#) on page 2-67
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Term	Definition
JTAG Timing Specifications	<p>JTAG Timing Specifications:</p>  <p>The diagram illustrates the timing relationships between JTAG signals. TMS and TDI are shown as high-impedance signals during certain phases. TCK is the clock signal. TDO is the data output signal. The timing parameters are defined as follows:</p> <ul style="list-style-type: none">t_{JCP}: JTAG Capture Periodt_{JCH}: JTAG Clock Hight_{JCL}: JTAG Clock Lowt_{JPSU}: JTAG Setupt_{JPH}: JTAG Pulse Hight_{JPZX}: JTAG Pulse Zt_{JPCO}: JTAG Pulse COt_{JPXZ}: JTAG Pulse XZ
PLL Specifications	<p>Diagram of PLL Specifications</p>  <p>The diagram shows the internal structure of a PLL. The Core Clock is input to a Switchover block, which then feeds into a PFD (Phase-Frequency Detector). The PFD output goes through a CP (Charge Pump) and an LF (Loop Filter) to the VCO (Voltage-Controlled Oscillator). The VCO output is fed back to the PFD and also passes through a Delta Sigma Modulator. The output of the Delta Sigma Modulator is fed into a Counters block (CO, C 17). The Counters output is then split into CLKOUT Pins (fOUT_EXT), fOUT, and RCLK. A Key indicates that components in blue (PFD, CP, LF, VCO, Counters) are reconfigurable in User Mode.</p> <p>Note: 1. Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>