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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	18870
Number of Logic Elements/Cells	400000
Total RAM Bits	34322432
Number of I/O	674
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme5k2f40i3ln

Contents

Caution: Conditions outside the range listed in the following table may cause permanent damage tothe device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	–0.50	1.43	V
V_{CCP}	Periphery circuitry, PCIe® hardIP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.50	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.50	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO}	I/O power supply	–0.50	3.90	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V_{CCA_FPLL}	PLL analog power supply	–0.50	3.25	V
V_{CCA_GXB}	Transceiver high voltage power	–0.50	3.25	V
V_{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V_{CCR_GXB}	Receiver power	–0.50	1.50	V
V_{CCT_GXB}	Transmitter power	–0.50	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.50	1.50	V
V_I	DC input voltage	–0.50	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.50	3.90	V

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(15)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

DSP Block Performance Specifications

Table 1-37: DSP Block Performance Specifications for Arria V Devices

Mode		Performance			Unit
		–I3, –C4	–I5, –C5	–C6	
Modes using One DSP Block	Independent 9 × 9 multiplication	370	310	220	MHz
	Independent 18 × 19 multiplication	370	310	220	MHz
	Independent 18 × 25 multiplication	370	310	220	MHz
	Independent 20 × 24 multiplication	370	310	220	MHz
	Independent 27 × 27 multiplication	310	250	200	MHz
	Two 18 × 19 multiplier adder mode	370	310	220	MHz
	18 × 18 multiplier added summed with 36-bit input	370	310	220	MHz
Modes using Two DSP Blocks	Complex 18 × 19 multiplication	370	310	220	MHz

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–I3, –C4			–I5, –C5			–C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40[72]	5	—	800	5	—	750	5	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards[73]		Clock boost factor W = 1 to 40[72]	5	—	625	5	—	625	5	—	500	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards[74]		Clock boost factor W = 1 to 40[72]	5	—	420	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	625[75]	5	—	625[75]	5	—	500[75]	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =3 to 10[76]	[77]	—	1250	[77]	—	1250	[77]	—	1050	Mbps

[72] Clock boost factor (W) is the ratio between the input data rate and the input clock rate.
[73] This applies to DPA and soft-CDR modes only.
[74] This applies to non-DPA mode only.
[75] This is achieved by using the LVDS clock network.
[76] The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
[77] The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

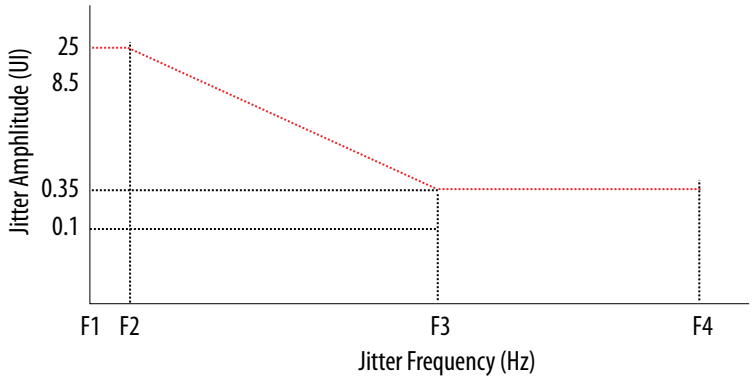


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

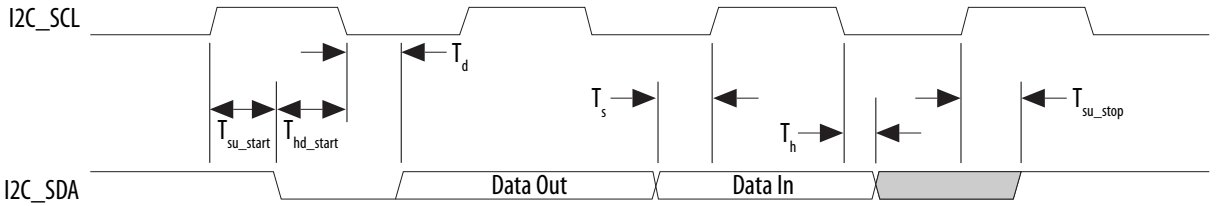
Parameter	Clock Network	Symbol	–I3, –C4		–I5, –C5		–C6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	–41	41	–50	50	–55	55	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	63		90		94		ps

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 1-16: I²C Timing Diagram



NAND Timing Characteristics

Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

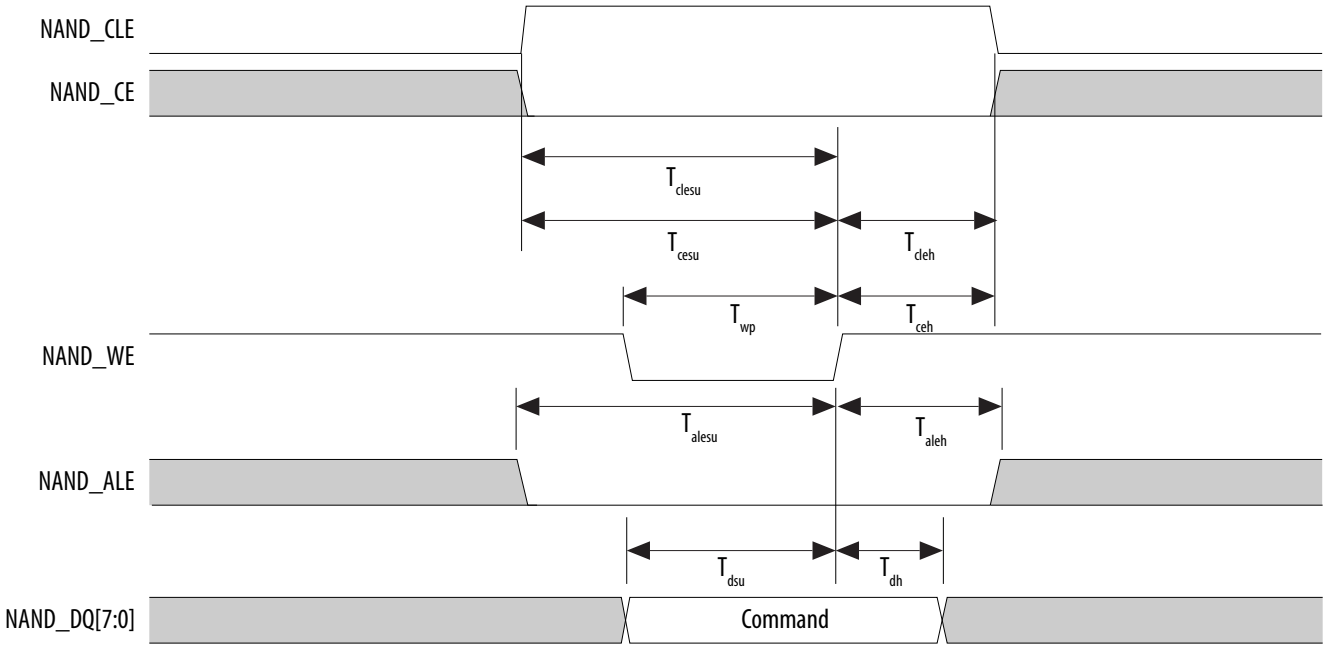
The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T_{wp} (89)	Write enable pulse width	10	—	ns
T_{wh} (89)	Write enable hold time	7	—	ns
T_{rp} (89)	Read enable pulse width	10	—	ns
T_{reh} (89)	Read enable hold time	7	—	ns
T_{clesu} (89)	Command latch enable to write enable setup time	10	—	ns
T_{cleh} (89)	Command latch enable to write enable hold time	5	—	ns
T_{cesu} (89)	Chip enable to write enable setup time	15	—	ns
T_{ceh} (89)	Chip enable to write enable hold time	5	—	ns
T_{alesu} (89)	Address latch enable to write enable setup time	10	—	ns
T_{aleh} (89)	Address latch enable to write enable hold time	5	—	ns
T_{dsu} (89)	Data to write enable setup time	10	—	ns

(89) Timing of the NAND interface is controlled through the NAND configuration registers.

Symbol	Description	Min	Max	Unit
T_{dh} (89)	Data to write enable hold time	5	—	ns
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 1-17: NAND Command Latch Timing Diagram



FPP Configuration Timing when DCLK-to-DATA[] >1

Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(98)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(99)	µs
t_{CF2CK}(100)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(100)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$(101)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode(102)	175	437	µs

(98) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(99) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
(100) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(101) N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.
(102) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V I/O Timing Spreadsheet
Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

Parameter[112]	Available Settings	Minimum Offset[113]	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C4	–C5	–C6	–I3	–I5	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

(112) You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.
(113) Minimum offset does not include the intrinsic delay.

Date	Version	Changes

December 2015	2015.12.16	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.
		  • Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications.
		  • Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.
		• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.
		  • Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol.
		  • Updated $T_{sdmmc\_clk\_out}$ and T_{d} specifications.
		  • Added T_{sdmmc_clk}, T_{su}, and T_{h} specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the following diagrams:
		  • Quad SPI Flash Timing Diagram
		  • SD/MMC Timing Diagram
		• Updated configuration .rbf sizes for Arria V devices.
		• Changed instances of *Quartus II* to *Quartus Prime*.

Date	Version	Changes
July 2014	3.8	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Updated V_{CC_HPS} specification in Table 5. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 39. • Updated T_d and T_h specifications in Table 45. • Added T_h specification in Table 47 and Figure 13. • Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 58. • Added DCLK device initialization clock source specification in Table 60. • Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 63.
February 2014	3.7	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.6	• Added "HPS PLL Specifications". • Added Table 24, Table 39, and Table 40. • Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. • Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. • Removed table: GPIO Pulse Width for Arria V Devices.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum(114)	Typical	Maximum (114)	Unit
V_{CC}	Core voltage and periphery circuitry power supply (115)	—	0.82	0.85	0.88	V

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(115) The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Rise time	Measure at ±60 mV of differential signal (138)	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal (138)	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express ®(PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1000/900/850 (139)			1000/900/850 (139)			mV
	RX reference clock pin	1.0/0.9/0.85 (140)			1.0/0.9/0.85(140)			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

(138) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(139) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
(140) This supply follows VCCR_GXB

Mode [164]	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
Register	2	C3, I3L core speed grade	9.9	9	7.92	7.2	4.9	4.,5	3.92	3.6
	3	C4, I4 core speed grade	8.8	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Related Information

Operating Conditions on page 2-1

10G PCS Data Rate

Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices

Mode [165]	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92
Register	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92

(164) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(165) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (182), (183)	(184)	—	1250	(184)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA (185), (186), (187), (188)	(184)	—	1600	(184)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(184)	—	(189)	(184)	—	(189)	Mbps
	SERDES factor J = 1, uses SDR Register	(184)	—	(189)	(184)	—	(189)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (190)	SERDES factor J = 4 to 10 (191)	(184)	—	840	(184)	—	840	Mbps

(182) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
(183) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(184) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(185) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(186) Requires package skew compensation with PCB trace length.
(187) Do not mix single-ended I/O buffer within LVDS I/O bank.
(188) Chip-to-chip communication only with a maximum load of 5 pF.
(189) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(190) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
(191) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	4	ns
t_{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t_{H}	Data hold time after falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode (216)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period)	—	—

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

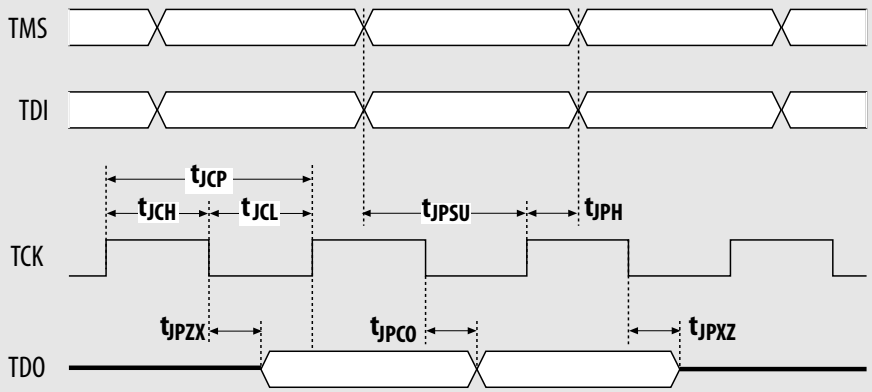
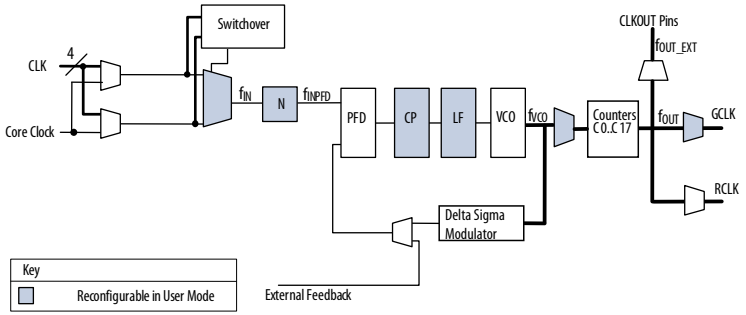
The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- **Passive Serial Configuration Timing** on page 2-67
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

(216) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Term	Definition
JTAG Timing Specifications	JTAG Timing Specifications: 
PLL Specifications	Diagram of PLL Specifications  Note: 1. Core Clock can only be fed by dedicated clock input pins or PLL outputs.

Date	Version	Changes

June 2016	2016.06.20	• Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table.
		• Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table.
		• Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table:
		  • True RSDS output standard: data rates of up to 230 Mbps
		  • True mini-LVDS output standard: data rates of up to 340 Mbps

December 2015	2015.12.16	• Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table. • Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table. • Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table. • Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table.
June 2015	2015.06.16	• Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table. • Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table.
January 2015	2015.01.30	• Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table. • Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table. • Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table.