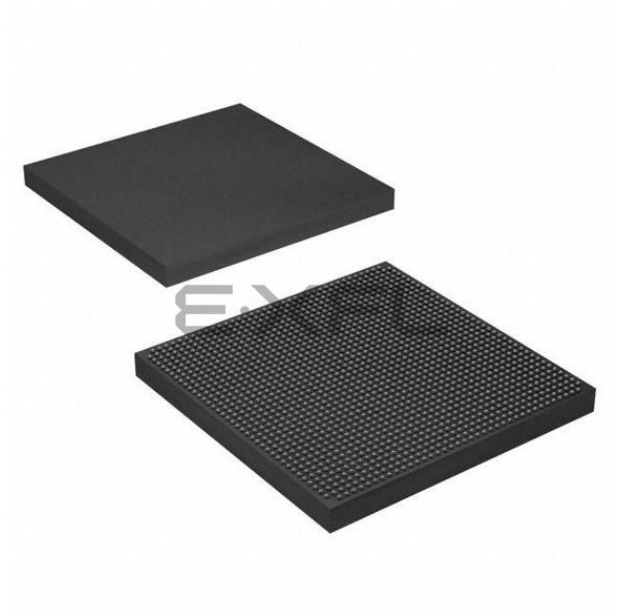

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	18870
Number of Logic Elements/Cells	400000
Total RAM Bits	34322432
Number of I/O	674
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme5k3f40i4n

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in}(input clock frequency) TrueDi•erential I/O Standards(179)	Clock boost factor W = 1 to 40(180)	5	…	625	5	…	525	MHz
f_{HSCLK_in}(input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40(180)	5	…	625	5	…	525	MHz
f_{HSCLK_in}(input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40(180)	5	…	420	5	…	420	MHz
f_{HSCLK_OUT}(output clock frequency)	…	5	…	625(181)	5	…	525(181)	MHz

Transmitter High-Speed I/OSpeci€cations

Table 2-40: Transmitter High-Speed I/OSpeci€cationsfor Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

(179) ,is only applies to DPA and sb‡-CDRmodes.
(180) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.
(181) ,is is achieved by using the LVDS clock network.

Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP •8, FPP •16, and FPP •32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	…	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	…	600	ns
t_{CFG}	nCONFIG low pulse width	2	…	Œs
t_{STATUS}	nSTATUS low pulse width	268	1,506(205)	Œs
t_{CF2ST1}	nCONFIG high to nSTATUS high	…	1,506(206)	Œs
t_{CF2CK} (207)	nCONFIG high to €rst rising edge on DCLK	1,506	…	Œs
t_{ST2CK} (207)	nSTATUS high to €rst rising edge of DCLK	2	…	Œs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	…	ns
t_{DH}	DATA[] hold time a‡er rising edge on DCLK	0	…	ns
t_{CH}	DCLK high time	0.45 • $1/f_{MAX}$	…	s
t_{CL}	DCLK low time	0.45 • $1/f_{MAX}$	…	s
t_{CLK}	DCLK period	$1/f_{MAX}$	…	s
f_{MAX}	DCLK frequency (FPP •8/•16)	…	125	MHz
	DCLK frequency (FPP •32)	…	100	MHz
t_{CD2UM}	CONF_DONE high to user mode(208)	175	437	Œs

(205) ,is value is applicable if you do not delay €guration by extending the nCONFIG or nSTATUS low pulse width.
(206) ,is value is applicable if you do not delay €guration by externally holding the nSTATUS low.
(207) If nSTATUS is monitored, follow the t_{ST2CK} speci€cation. If nSTATUS is not monitored, follow the t_{CF2CK} speci€cation.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 • maximum DCLK period	…	…
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 • CLKUSR period) (209)	…	…

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

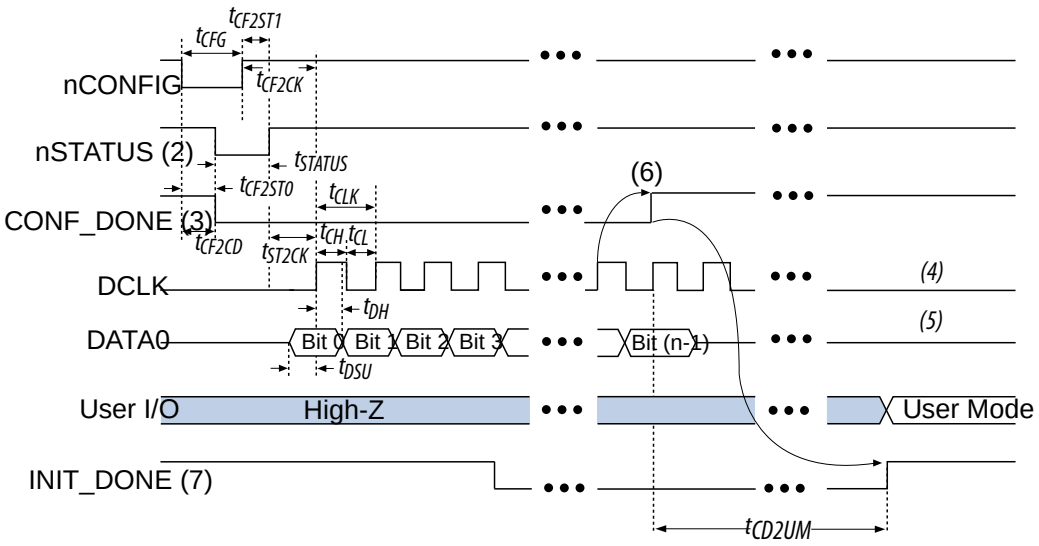
(208) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(209) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.