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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	21225
Number of Logic Elements/Cells	450000
Total RAM Bits	40249344
Number of I/O	674
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme7k2f40c3n

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
V _{CC_AUX_SHARED}	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 1-4

Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics**Supply Current and Power Consumption**

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- **PowerPlay Early Power Estimator User Guide**
Provides more information about power estimation tools.
- **PowerPlay Power Analysis chapter, Quartus Prime Handbook**
Provides more information about power estimation tools.

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIOMAX}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIOMAX}$	-30	—	30	μA

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V _{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold, high, sustaining current	I _{SUSH}	V _{IN} < V _{IH} (min)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus-hold, low, overdrive current	I _{ODL}	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold, high, overdrive current	I _{ODH}	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA

I/O Standard	V _{CCIO} (V)			V _{ID} (mV) ⁽¹⁶⁾			V _{ICM(DC)} (V)			V _{OD} (V) ⁽¹⁷⁾			V _{OCM} (V) ⁽¹⁷⁾⁽¹⁸⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.														
2.5 V LVDS ⁽¹⁹⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	D _{MAX} ≤ 1.25 Gbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D _{MAX} > 1.25 Gbps	1.55						
RSDS (HIO) ⁽²⁰⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽²¹⁾	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL ⁽²²⁾	—	—	—	300	—	—	0.60	D _{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D _{MAX} > 700 Mbps	1.60						

Related Information

- [Transceiver Specifications for Arria V GX and SX Devices](#) on page 1-23
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

⁽¹⁶⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

⁽¹⁷⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽¹⁸⁾ This applies to default pre-emphasis setting only.

⁽¹⁹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.

⁽²⁰⁾ For optimized RSBS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

⁽²¹⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

⁽²²⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

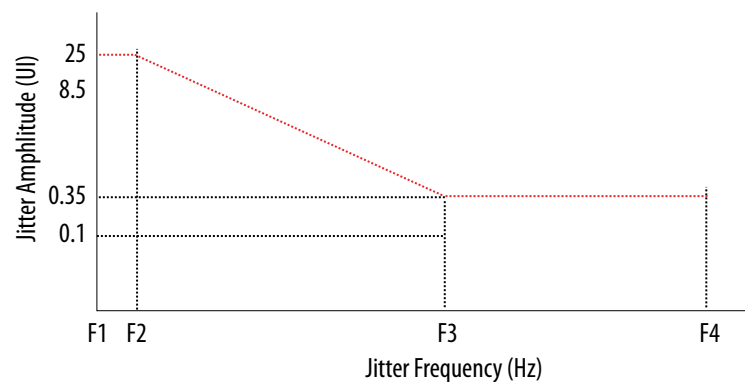
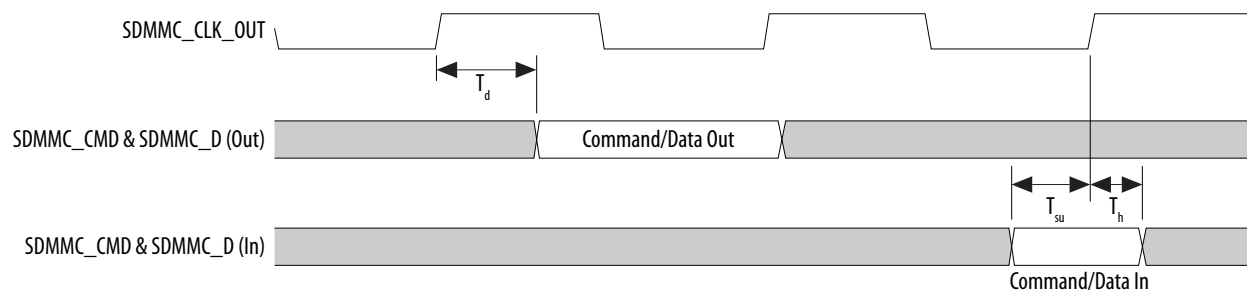


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 1-11: SD/MMC Timing Diagram

**Related Information**

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual

Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

HPS JTAG Timing Specifications

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	2	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12 ⁽⁹⁰⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁹⁰⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁹⁰⁾	ns

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 ⁽⁹¹⁾	ms

⁽⁹⁰⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

⁽⁹¹⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Symbol	Parameter	Minimum	Maximum	Unit
t_{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁹⁴⁾	μs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁹⁵⁾	μs
$t_{\text{CF2CK}}^{(96)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
$t_{\text{ST2CK}}^{(96)}$	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t_{CLK}	DCLK period	$1/f_{\text{MAX}}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/ \times 16$)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽⁹⁷⁾	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{\text{CD2CU}} + (T_{\text{init}} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

⁽⁹⁴⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁹⁵⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁹⁶⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽⁹⁷⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
Arria V GT	C3	71,015,712	439,960
	C7	101,740,800	446,360
	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SX	B3	185,903,680	450,968
	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.

Remote System Upgrades

Table 1-74: Remote System Upgrade Circuitry Timing Specifications for Arria V Devices

Parameter	Minimum	Unit
$t_{RU_nCONFIG}^{(110)}$	250	ns
$t_{RU_nRSTIMER}^{(111)}$	250	ns

Related Information

- [Remote System Upgrade State Machine](#)
Provides more information about configuration reset (RU_CONFIG) signal.
- [User Watchdog Timer](#)
Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 1-75: User Watchdog Internal Oscillator Frequency Specifications for Arria V Devices

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O timing and the Quartus Prime Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

⁽¹¹⁰⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

⁽¹¹¹⁾ This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

Date	Version	Changes
August 2013	3.5	- Removed “Pending silicon characterization” note in Table 29. - Updated Table 25.
August 2013	3.4	- Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64. - Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29.
June 2013	3.3	Updated Table 20, Table 21, Table 25, and Table 38.
May 2013	3.2	- Added Table 37. - Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23. - Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64. - Updated industrial junction temperature range for –I3 speed grade in “PLL Specifications” section.
March 2013	3.1	- Added HPS reset information in the “HPS Specifications” section. - Added Table 60. - Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59. - Updated Figure 21.

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVC MOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$

I/O Standard	V_{CCIO} (V) ⁽¹²⁸⁾			V_{ID} (mV) ⁽¹²⁹⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽¹³⁰⁾			V_{OCM} (V) ⁽¹³⁰⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
RSDS (HIO) ⁽¹³³⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽¹³⁴⁾	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL ^{(135), (136)}	—	—	—	300	—	—	0.6	$D_{MAX} \leq 700$ Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} > 700$ Mbps	1.6	—	—	—	—	—	—

Related Information[Glossary](#) on page 2-73⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.⁽¹³⁰⁾ RL range: $90 \leq RL \leq 110 \Omega$.⁽¹³³⁾ For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.⁽¹³⁴⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.⁽¹³⁵⁾ LVPECL is only supported on dedicated clock input pins.⁽¹³⁶⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	—	100	—	710	100	—	710	MHz

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Rise time	Measure at ± 60 mV of differential signal ⁽¹³⁸⁾	—	—	400	—	—	400	ps
Fall time	Measure at ± 60 mV of differential signal ⁽¹³⁸⁾	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	—	0 to -0.5	—	%
On-chip termination resistors	—	—	100	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1000/900/850 ⁽¹³⁹⁾			1000/900/850 ⁽¹³⁹⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽¹⁴⁰⁾			1.0/0.9/0.85 ⁽¹⁴⁰⁾			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

⁽¹³⁸⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.⁽¹³⁹⁾ The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.⁽¹⁴⁰⁾ This supply follows V_{CCR_GXB}

Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}^{(168)}$	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

⁽¹⁶⁷⁾ This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽¹⁶⁸⁾ The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{INCCJ}}^{(171), (172)}$	Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz)	-750	—	+750	ps (p-p)
$t_{\text{OUTPJ_DC}}^{(173)}$	Period Jitter for dedicated clock output in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTPJ_DC}}^{(173)}$	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹⁷⁶⁾ , 17.5 ⁽¹⁷⁴⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}^{(173)}$	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}^{(173)}$	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹⁷⁶⁾ , 17.5 ⁽¹⁷⁴⁾	mUI (p-p)

⁽¹⁷¹⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽¹⁷²⁾ The f_{REF} is f_{IN}/N specification applies when $N = 1$.

⁽¹⁷³⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.

⁽¹⁷⁴⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

Description	Min	Typ	Max	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

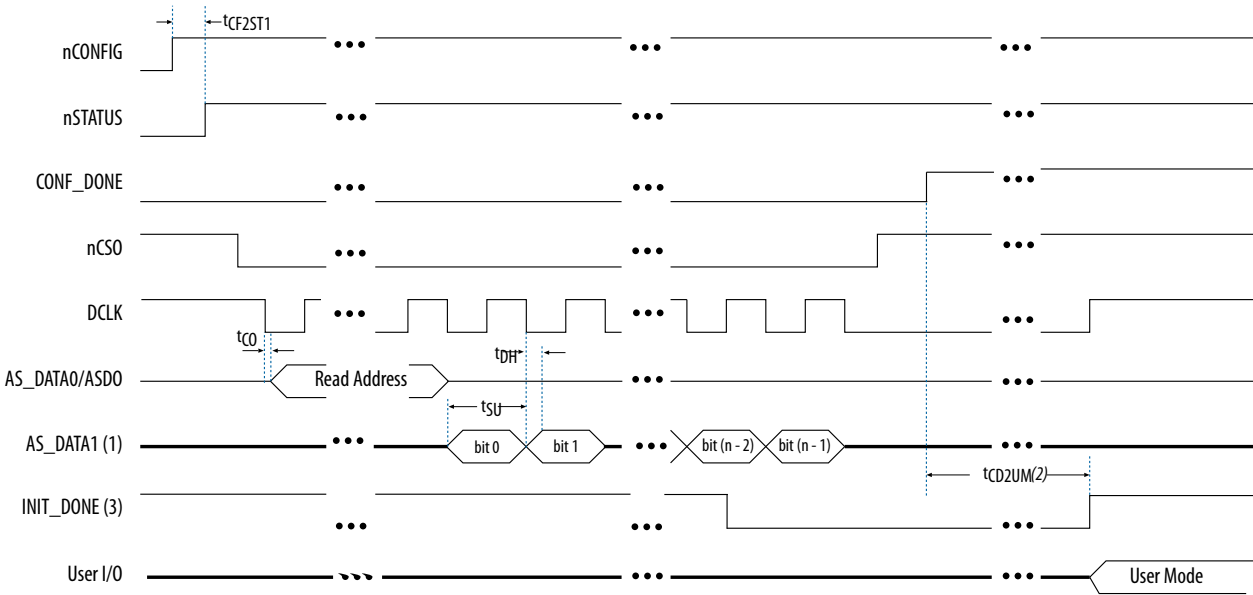
Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing

Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.



- Notes:
- 1. If you are using AS x4 mode, this signal represents the AS_DATA[3:0] and ERQ sends in 4-bits of data for each DCLK cycle.
 - 2. The initialization clock can be from internal oscillator or CLKUSR pin
 - 3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.

Date	Version	Changes
July 2014	3.8	- Updated Table 21. - Updated Table 22 V_{OCM} (DC Coupled) condition. - Updated the DCLK note to Figure 6, Figure 7, and Figure 9. - Added note to Table 5 and Table 6. - Added the DCLK specification to Table 50. - Added note to Table 51. - Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	- Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. - Updated “PLL Specifications”.
August 2013	3.5	Updated Table 28.
August 2013	3.4	- Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. - Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	- Added Table 23. - Updated Table 5, Table 22, Table 26, and Table 57. - Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	- Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. - Updated “Maximum Allowed Overshoot and Undershoot Voltage”.
December 2012	3.0	Initial release.