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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 21225 |
| Number of Logic Elements/Cells | 450000 |
| Total RAM Bits | 40249344 |
| Number of I/O | 674 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agzme7k3f40c4n |

## Transceiver Specifications for Arria V GT and ST Devices

### Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300(42)/2000 | mV |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | — | 1.2 | — | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | mV |

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

## Typical TX $V_{OD}$ Setting for Arria V Transceiver Channels with termination of 100 Ω

**Table 1-32: Typical TX $V_{OD}$ Setting for Arria V Transceiver Channels with termination of 100 Ω**

| Symbol | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| $V_{OD}$ differential peak-to-peak typical | 6[59] | 120 | 34 | 680 |
| | 7[59] | 140 | 35 | 700 |
| | 8[59] | 160 | 36 | 720 |
| | 9 | 180 | 37 | 740 |
| | 10 | 200 | 38 | 760 |
| | 11 | 220 | 39 | 780 |
| | 12 | 240 | 40 | 800 |
| | 13 | 260 | 41 | 820 |
| | 14 | 280 | 42 | 840 |
| | 15 | 300 | 43 | 860 |
| | 16 | 320 | 44 | 880 |
| | 17 | 340 | 45 | 900 |
| | 18 | 360 | 46 | 920 |
| | 19 | 380 | 47 | 940 |
| | 20 | 400 | 48 | 960 |
| | 21 | 420 | 49 | 980 |
| | 22 | 440 | 50 | 1000 |
| | 23 | 460 | 51 | 1020 |
| | 24 | 480 | 52 | 1040 |

[58] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.
[59] Only valid for data rates ≤ 5 Gbps.

## Memory Output Clock Jitter Specifications

### Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) $10^{-12}$, equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

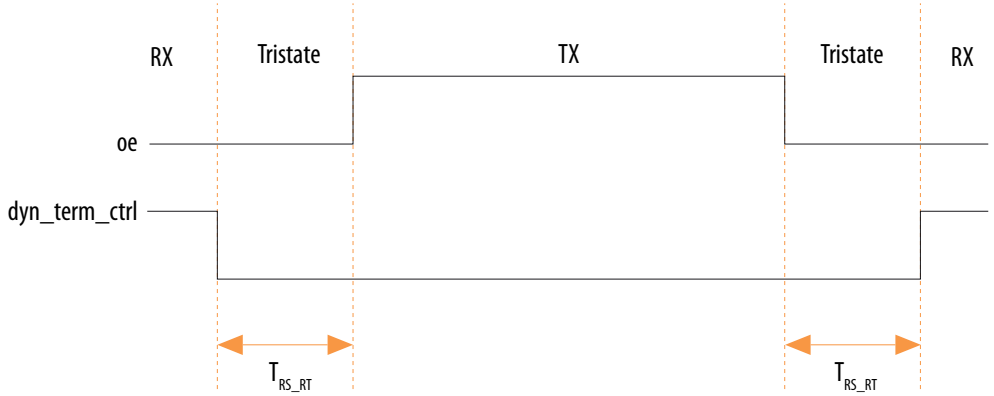
| Parameter | Clock Network | Symbol | –I3, –C4 | | –I5, –C5 | | –C6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Clock period jitter | PHYCLK | $t_{JIT(per)}$ | –41 | 41 | –50 | 50 | –55 | 55 | ps |
| Cycle-to-cycle period jitter | PHYCLK | $t_{JIT(cc)}$ | 63 | | 90 | | 94 | | ps |

## OCT Calibration Block Specifications

### Table 1-46: OCT Calibration Block Specifications for Arria V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for $R_S$ OCT/$R_T$ OCT calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS\_RT}$ | Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between $R_S$ OCT and $R_T$ OCT | — | 2.5 | — | ns |

**Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals**




## Duty Cycle Distortion (DCD) Specifications

**Table 1-47: Worst-Case DCD on Arria V I/O Pins**

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

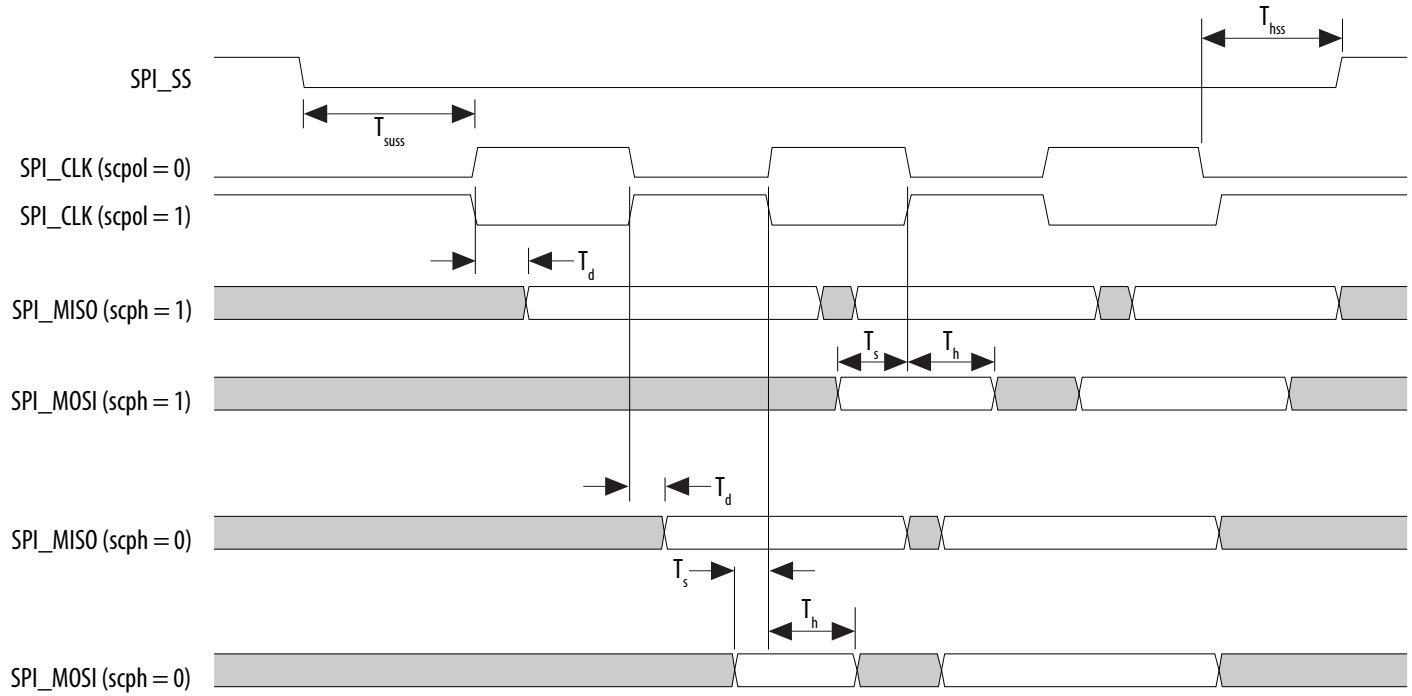
| Symbol | –I3, –C4 | | –C5, –I5 | | –C6 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

# HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

**Figure 1-10: SPI Slave Timing Diagram**




**Related Information**

**SPI Controller, Arria V Hard Processor System Technical Reference Manual**
Provides more information about rx_sample_delay.

## SD/MMC Timing Characteristics

**Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices**

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smplsel` via the system manager. `drvsel` can be set from 1 to 7 and `smplsel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{sdmmc\_clk}$ (internal reference clock) | SDMMC_CLK clock period (Identification mode) | 20 | — | ns |
| | SDMMC_CLK clock period (Default speed mode) | 5 | — | ns |
| | SDMMC_CLK clock period (High speed mode) | 5 | — | ns |
| $T_{sdmmc\_clk\_out}$ (interface output clock) | SDMMC_CLK_OUT clock period (Identification mode) | 2500 | — | ns |
| | SDMMC_CLK_OUT clock period (Default speed mode) | 40 | — | ns |
| | SDMMC_CLK_OUT clock period (High speed mode) | 20 | — | ns |
| $T_{dutycycle}$ | SDMMC_CLK_OUT duty cycle | 45 | 55 | % |
| $T_d$ | SDMMC_CMD/SDMMC_D output delay | ($T_{sdmmc\_clk}$ × `drvsel`)/2 – 1.23 (87) | ($T_{sdmmc\_clk}$ × `drvsel`)/2 + 1.69 (87) | ns |
| $T_{su}$ | Input setup time | 1.05 – ($T_{sdmmc\_clk}$ × `smplsel`)/2 (88) | — | ns |
| $T_h$ | Input hold time | ($T_{sdmmc\_clk}$ × `smplsel`)/2 (88) | — | ns |

(87) `drvsel` is the drive clock phase shift select value.
(88) `smplsel` is the sample clock phase shift select value.

**Table 1-57: RGMII RX Timing Requirements for Arria V Devices**

| Symbol | Description | Min | Typ | Unit |
|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | RX_CLK clock period | — | 8 | ns |
| $T_{clk}$ (100Base-T) | RX_CLK clock period | — | 40 | ns |
| $T_{clk}$ (10Base-T) | RX_CLK clock period | — | 400 | ns |
| $T_{su}$ | RX_D/RX_CTL setup time | 1 | — | ns |
| $T_h$ | RX_D/RX_CTL hold time | 1 | — | ns |

**Figure 1-14: RGMII RX Timing Diagram**

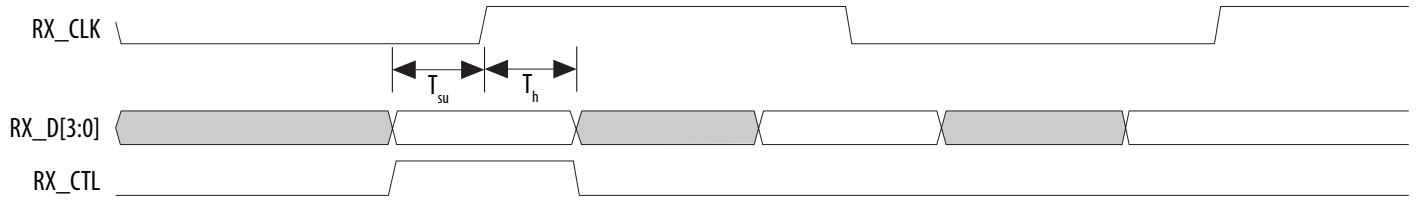



**Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | MDC clock period | — | 400 | — | ns |
| $T_d$ | MDC to MDIO output data delay | 10 | — | 20 | ns |
| $T_s$ | Setup time for MDIO data | 10 | — | — | ns |
| $T_h$ | Hold time for MDIO data | 0 | — | — | ns |

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{dh}$ (89) | Data to write enable hold time | 5 | — | ns |
| $T_{cea}$ | Chip enable to data access time | — | 25 | ns |
| $T_{rea}$ | Read enable to data access time | — | 16 | ns |
| $T_{rhz}$ | Read enable to data high impedance | — | 100 | ns |
| $T_{rr}$ | Ready to read enable low | 20 | — | ns |

**Figure 1-17: NAND Command Latch Timing Diagram**

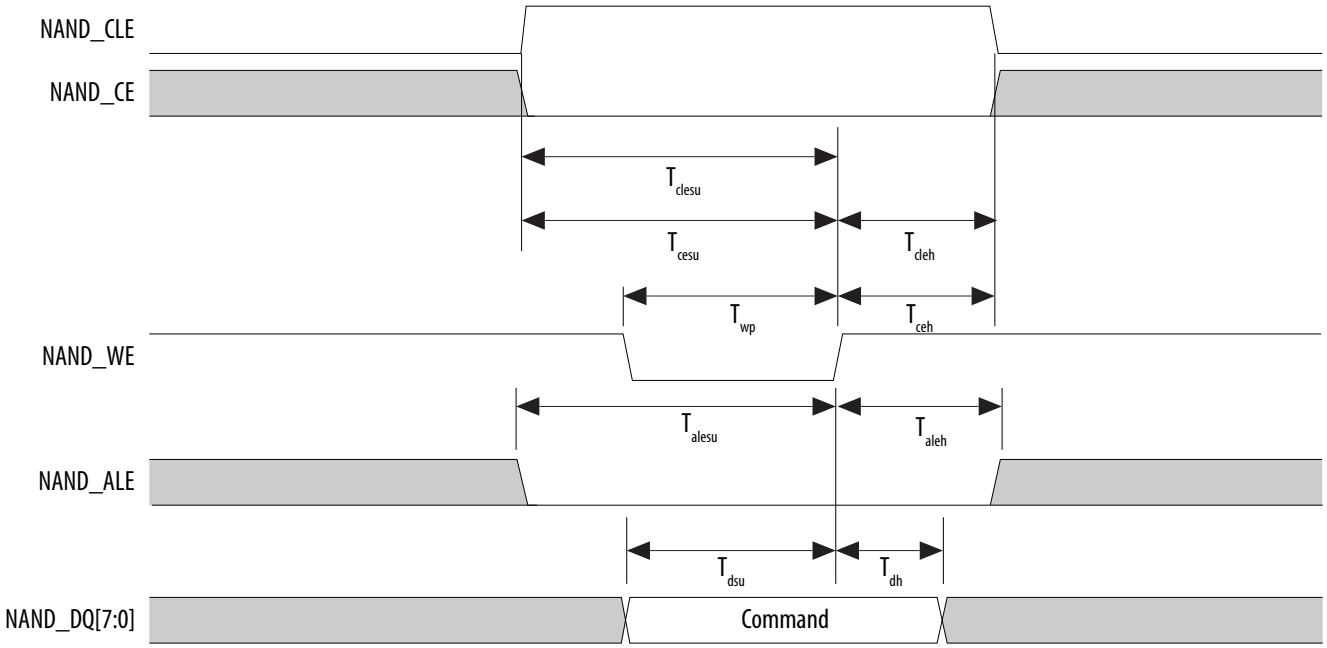
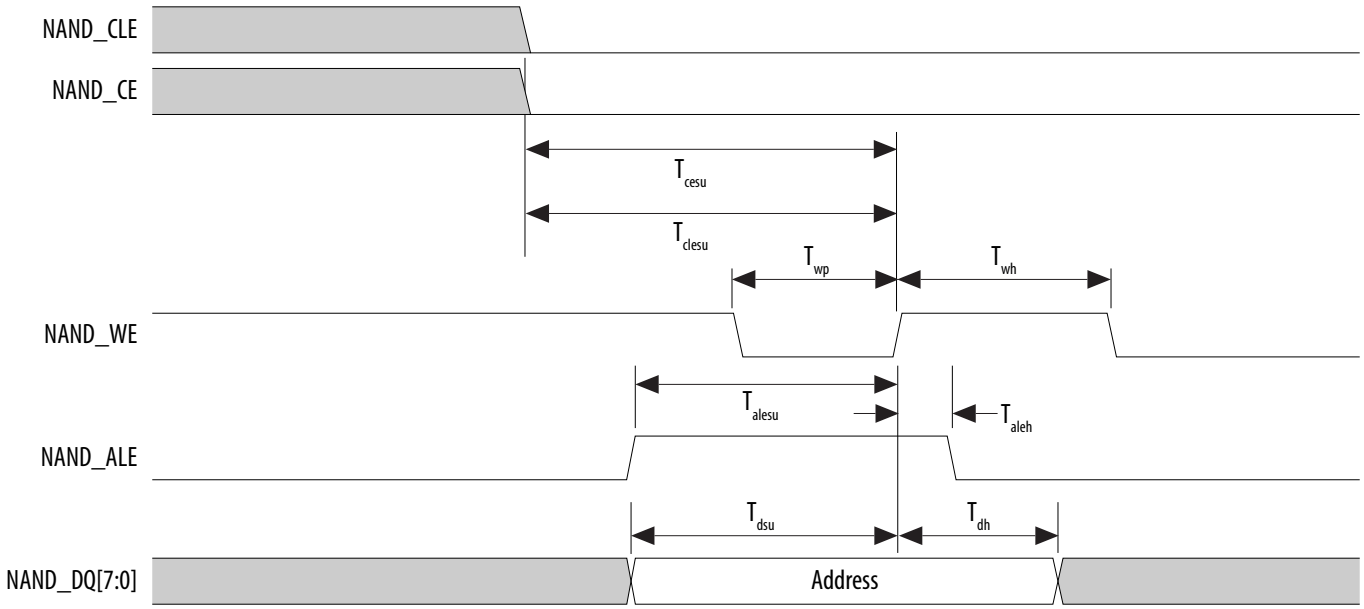


**Figure 1-18: NAND Address Latch Timing Diagram**



# FPP Configuration Timing

## DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

**Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices**

| Configuration Scheme | Encryption | Compression | DCLK-to-DATA[] Ratio (r) |
|---|---|---|---|
| FPP (8-bit wide) | Off | Off | 1 |
| | On | Off | 1 |
| | Off | On | 2 |
| | On | On | 2 |
| FPP (16-bit wide) | Off | Off | 1 |
| | On | Off | 2 |
| | Off | On | 4 |
| | On | On | 4 |

## FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

**Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices**

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

**Arria V I/O Timing Spreadsheet**
Provides the Arria V Excel-based I/O timing spreadsheet.

## Programmable IOE Delay

**Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices**

| Parameter[112] | Available Settings | Minimum Offset[113] | Fast Model | | Slow Model | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | –C4 | –C5 | –C6 | –I3 | –I5 | |
| D1 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |
| D3 | 8 | 0 | 1.763 | 1.795 | 2.999 | 3.496 | 3.571 | 3.031 | 3.643 | ns |
| D4 | 32 | 0 | 0.508 | 0.518 | 0.869 | 1.063 | 1.063 | 1.063 | 1.057 | ns |
| D5 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |

## Programmable Output Buffer Delay

**Table 1-77: Programmable Output Buffer Delay for Arria V Devices**

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

(112) You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.
(113) Minimum offset does not include the intrinsic delay.

| Date | Version | Changes |
|---|---|---|
| November 2012 | 3.0 | • Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.<br>• Removed table: Transceiver Block Jitter Specifications for Arria V Devices.<br>• Added HPS information:<br>  • Added "HPS Specifications" section.<br>  • Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.<br>  • Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.<br>  • Updated Table 3 and Table 5. |
| October 2012 | 2.4 | • Updated Arria V GX $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ minimum and maximum values, and data rate in Table 4.<br>• Added receiver $V_{ICM}$ (AC coupled) and $V_{ICM}$ (DC coupled) values, and transmitter $V_{OCM}$ (AC coupled) and $V_{OCM}$ (DC coupled) values in Table 20 and Table 21. |
| August 2012 | 2.3 | Updated the SERDES factor condition in Table 30. |
| July 2012 | 2.2 | • Updated the maximum voltage for $V_I$ (DC input voltage) in Table 1.<br>• Updated Table 20 to include the Arria V GX -I3 speed grade.<br>• Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21.<br>• Updated the SERDES factor condition in Table 30.<br>• Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade. |
| June 2012 | 2.1 | Updated $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ values in Table 4. |

## Bus Hold Specifications

### Table 2-9: Bus Hold Parameters for Arria V GZ Devices

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

### Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.

| Symbol | Description | Conditions | Calibration Accuracy | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | % |
| 50-Ω $R_S$ | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | $V_{CCIO}$ = 1.2 V | ±15 | ±15 | % |
| 50-Ω $R_T$ | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 V | –10 to +40 | –10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω $R_T$ | Internal parallel termination with calibration (20-Ω , 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 V | –10 to +40 | –10 to +40 | % |
| 60-Ω and 120-Ω $R_T$ | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | $V_{CCIO}$ = 1.2 | –10 to +40 | –10 to +40 | % |
| 25-Ω $R_{S\_left\_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | % |

**Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices**

| Symbol | Description | Conditions | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 25-Ω R, 50-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.0 and 2.5 V | ±40 | ±40 | % |

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |

**Table 2-18: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC gain setting = 0 | — | 0 | — | — | 0 | — | dB |
| | DC gain setting = 1 | — | 2 | — | — | 2 | — | dB |
| | DC gain setting = 2 | — | 4 | — | — | 4 | — | dB |
| | DC gain setting = 3 | — | 6 | — | — | 6 | — | dB |
| | DC gain setting = 4 | — | 8 | — | — | 8 | — | dB |

**Related Information**

**Arria V Device Overview**
For more information about device ordering codes.

## Transmitter

### Table 2-25: Transmitter Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O Standards | 1.4-V and 1.5-V PCML | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 9900 | 600 | — | 8800 | Mbps |
| Data rate (10G PCS) | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |

## Typical VOD Settings

### Table 2-32: Typical $V_{OD}$ Setting for Arria V GZ Channel, TX Termination = 100 Ω

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| $V_{OD}$ **differential peak to peak typical** | 0 (166) | 0 | 32 | 640 |
| | 1 (166) | 20 | 33 | 660 |
| | 2 (166) | 40 | 34 | 680 |
| | 3 (166) | 60 | 35 | 700 |
| | 4 (166) | 80 | 36 | 720 |
| | 5 (166) | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |

(166) If TX termination resistance = 100 Ω,this VOD setting is illegal.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 (182), (183) | (184) | — | 1250 | (184) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA (185), (186), (187), (188) | (184) | — | 1600 | (184) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (184) | — | (189) | (184) | — | (189) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (184) | — | (189) | (184) | — | (189) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{HSDR}$ (data rate) (190) | SERDES factor J = 4 to 10 (191) | (184) | — | 840 | (184) | — | 840 | Mbps |

(182) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
(183) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(184) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(185) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(186) Requires package skew compensation with PCB trace length.
(187) Do not mix single-ended I/O buffer within LVDS I/O bank.
(188) Chip-to-chip communication only with a maximum load of 5 pF.
(189) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(190) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
(191) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197) | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197) | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (198) | — | (200) | (198) | — | (200) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |

(192) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

# JTAG Configuration Specifications

**Table 2-54: JTAG Timing Parameters and Values for Arria V GZ Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30 | — | ns |
| $t_{JCP}$ | TCK clock period | 167 (203) | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 (204) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 (204) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 (204) | ns |

## Fast Passive Parallel (FPP) Configuration Timing

### DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

(203) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

(204) A 1-ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 12 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.