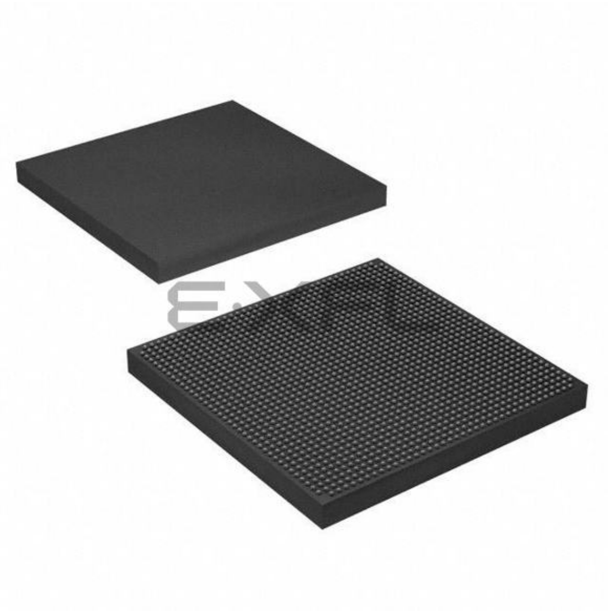
Intel - 5AGZME7K3F40I4N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	21225
Number of Logic Elements/Cells	450000
Total RAM Bits	40249344
Number of I/O	674
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agzme7k3f40i4n

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–I3, –C4	–I5, –C5	–C6	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	−10 to +40	−10 to +40	−10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	−10 to +40	−10 to +40	−10 to +40	%

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter `REFCLK` phase noise[43]	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	≥ 1 MHz	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver)[44]	—	611	—	6553.6	Mbps

---

[43] The transmitter `REFCLK` phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

[44] To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor J ≥ 8(76)(78), LVDS TX with RX DPA	(77)	—	1600	(77)	—	1500	(77)	—	1250	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(77)	—	(79)	(77)	—	(79)	(77)	—	(79)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate)(80)	SERDES factor J = 4 to 10(81)	(77)	—	945	(77)	—	945	(77)	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)(80)	SERDES factor J = 4 to 10(81)	(77)	—	200	(77)	—	200	(77)	—	200	Mbps
$t_{x\ Jitter}$ -True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

---

(78) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.

(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\text{ Jitter}}$ -Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	260	—	—	300	—	—	350	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.16	—	—	0.18	—	—	0.21	UI
$t_{x\text{ Jitter}}$ -Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.15	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} and t_{FALL}	True Differential I/O Standards(82)	—	—	160	—	—	180	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Network	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	—	—	500	—	—	500	—	—	500	ps

---

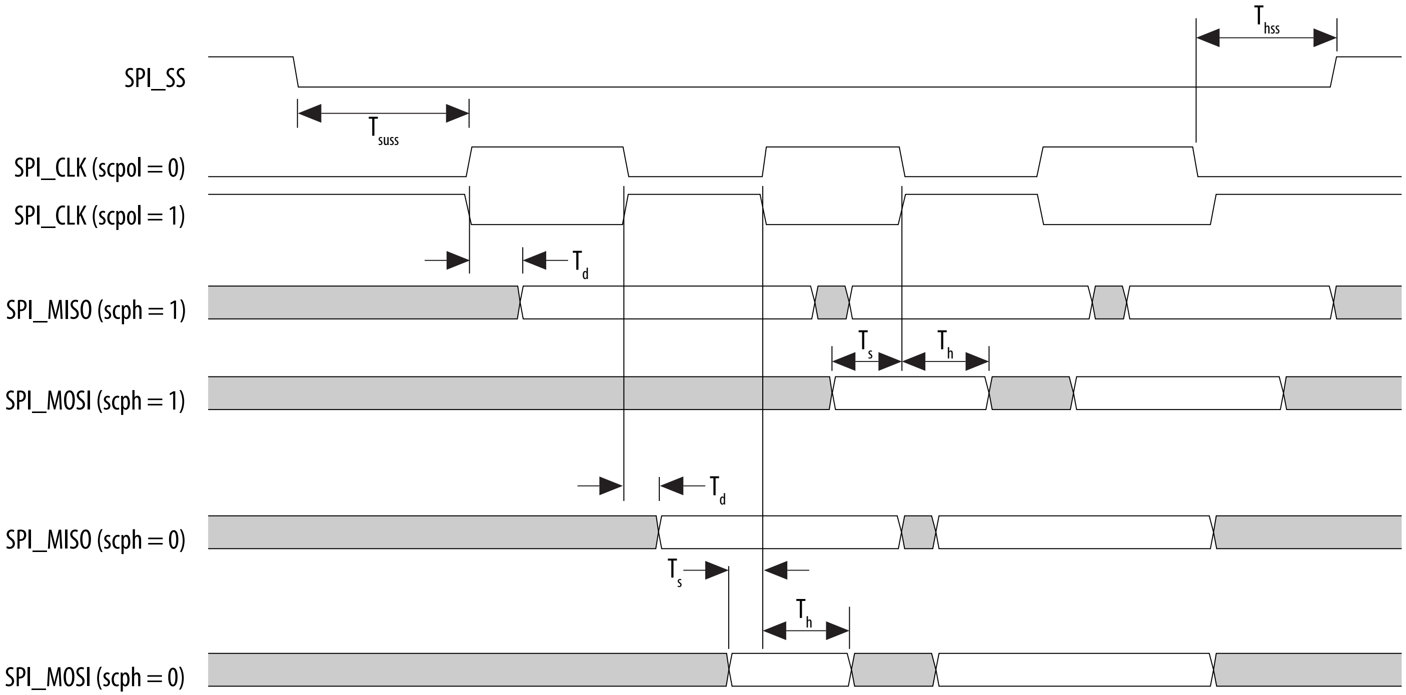
(82) This applies to default pre-emphasis and V_{OD} settings only.

Symbol		Condition	–I3, –C4			–I5, –C5			–C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J =3 to 10(76)	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J ≥ 8 with DPA(76)(78)	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(77)	—	(83)	(77)	—	(83)	(77)	—	(83)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(77)	—	(79)	(77)	—	(79)	(77)	—	(79)	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	±ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

---

(83) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Figure 1-10: SPI Slave Timing Diagram



Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

Symbol	Parameter	Minimum	Maximum	Unit
t_{STATUS}	`nSTATUS` low pulse width	268	1506[94]	µs
t_{CF2ST1}	`nCONFIG` high to `nSTATUS` high	—	1506[95]	µs
t_{CF2CK}[96]	`nCONFIG` high to first rising edge on `DCLK`	1506	—	µs
t_{ST2CK}[96]	`nSTATUS` high to first rising edge of `DCLK`	2	—	µs
t_{DSU}	`DATA[]` setup time before rising edge on `DCLK`	5.5	—	ns
t_{DH}	`DATA[]` hold time after rising edge on `DCLK`	0	—	ns
t_{CH}	`DCLK` high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	`DCLK` low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	`DCLK` period	$1/f_{MAX}$	—	s
f_{MAX}	`DCLK` frequency (FPP ×8/ ×16)	—	125	MHz
t_{CD2UM}	`CONF_DONE` high to user mode[97]	175	437	µs
t_{CD2CU}	`CONF_DONE` high to `CLKUSR` enabled	4× maximum `DCLK` period	—	—
t_{CD2UMC}	`CONF_DONE` high to user mode with `CLKUSR` option on	t_{CD2CU} + (T_{init} × `CLKUSR` period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

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[94] You can obtain this value if you do not delay configuration by extending the `nCONFIG` or the `nSTATUS` low pulse width.

[95] You can obtain this value if you do not delay configuration by externally holding the `nSTATUS` low.

[96] If `nSTATUS` is monitored, follow the t_{ST2CK} specification. If `nSTATUS` is not monitored, follow the t_{CF2CK} specification.

[97] The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Term	Definition
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes

December 2016	2016.12.09	• Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table.
		• Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table.
		• Updated T_{init} specifications in the following tables:
		  • FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices
		  • FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices
		  • AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices
		  • PS Timing Parameters for Arria V Devices

June 2016	2016.06.10	• Changed pin capacitance to maximum values.
		• Updated SPI Master Timing Requirements for Arria V Devices table.
		  • Added T_{su} and T_h specifications.
		  • Removed T_{dinmax} specifications.
		• Updated SPI Master Timing Diagram.
		• Updated T_{clk} spec from maximum to minimum in I^2C Timing Requirements for Arria V Devices table.

Date	Version	Changes

November 2012	3.0	• Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.
		• Removed table: Transceiver Block Jitter Specifications for Arria V Devices.
		• Added HPS information:
		  • Added "HPS Specifications" section.
		  • Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.
		  • Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.
		  • Updated Table 3 and Table 5.

October 2012	2.4	• Updated Arria V GX $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ minimum and maximum values, and data rate in Table 4. • Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	• Updated the maximum voltage for V_I (DC input voltage) in Table 1. • Updated Table 20 to include the Arria V GX -I3 speed grade. • Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. • Updated the SERDES factor condition in Table 30. • Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ values in Table 4.

Date	Version	Changes
June 2012	2.0	• Updated for the Quartus II software v12.0 release: • Restructured document. • Updated “Supply Current and Power Consumption” section. • Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. • Added Table 22, Table 23, and Table 33. • Added Figure 1–1 and Figure 1–2. • Added “Initialization” and “Configuration Files” sections.
February 2012	1.3	• Updated Table 2–1. • Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. • Updated V_{CCP} description.
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	• Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. • Added Table 2–5. • Added Figure 2–4.
August 2011	1.0	Initial release.

Arria V GZ Device Datasheet

2

2017.02.10

AV-51002

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This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information

Arria V Device Overview

For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

Symbol	Description	Condition	Minimum(114)	Typical	Maximum (114)	Unit
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} (116)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V_{CCBAT} (117)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V

---

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(116) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(117) If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

I/O Standard	V_{CCIO} (V) (128)			V_{ID} (mV) (129)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (130)			V_{OCM} (V) (130)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
RSDS (HIO) (133)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (134)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (135), (136)	—	—	—	300	—	—	0.6	D_{MAX} ≤ 700 Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	D_{MAX} > 700 Mbps	1.6	—	—	—	—	—	—

Related Information

Glossary on page 2-73

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(128) Differential inputs are powered by VCCPD which requires 2.5 V.

(129) The minimum VID value is applicable over the entire common mode range, VCM.

(130) RL range: 90 ≤ RL ≤ 110 Ω.

(133) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(134) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(135) LVPECL is only supported on dedicated clock input pins.

(136) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (146)	$V_{CCR\_GXB} = 1.0$ V ($V_{ICM} = 0.75$ V)	—	—	1.8	—	—	1.8	V
	$V_{CCR\_GXB} = 0.85$ V ($V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins (147)(148)	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85–Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100–Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120–Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150–Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	Ω

---

(146) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(147) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(148) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	3250/ 3125[158]	600	—	3250/ 3125 [158]	Mbps
$t_{pll\_powerdown}$[159]	—	1	—	—	1	—	—	µs
t_{pll_lock} [160]	—	—	—	10		—	10	µs

Related Information

Arria V Device Overview

For more information about device ordering codes.

Clock Network Data Rate

Table 2-29: Clock Network Maximum Data Rate Transmitter Specifications

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

Clock Network	ATX PLL			CMU PLL [161]			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 [162]	12.5	—	6	12.5	—	6	3.125	—	3
x6 [162]	—	12.5	6	—	12.5	6	—	3.125	6
x6 PLL Feedback [163]	—	12.5	Side-wide	—	12.5	Side-wide	—	—	—

---

[158] When you use fPLL as a TXPLL of the transceiver.

[159] $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

[160] t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

[161] ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

[162] Channel span is within a transceiver bank.

[163] Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} (167)	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
f_{VCO} (168)	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

---

(167) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(168) The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Mode	Performance			Unit
	C3, I3L	C4	I4	
One sum of two 27 × 27	380	300	290	MHz
One sum of two 36 × 18	380	300		MHz
One complex 18 × 18	400	350		MHz
One 36 × 36	380	300		MHz
Modes using Three DSP Blocks				
One complex 18 × 25	340	275	265	MHz
Modes using Four DSP Blocks				
One complex 27 × 27	350	310		MHz

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Memory	C3	C4	I3L	I4	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

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(178) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Description	Min	Typ	Max	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	`CONF_DONE` high to `CLKUSR` enabled	4 × maximum `DCLK` period	—	—
t_{CD2UMC}	`CONF_DONE` high to user mode with `CLKUSR` option on	t_{CD2CU} + (8576 × `CLKUSR` period)(209)	—	—

Related Information

- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

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(208) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(209) To enable the `CLKUSR` pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.