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Intel - 5ASTFD5K3F40I5NES Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are **Embedded - System On Chip (SoC)**?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore [™] with CoreSight [™]
Flash Size	
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5astfd5k3f40i5nes

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
		3.3 V	3.135	3.3	3.465	V
	-	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V	1/O buffers newer supply	1.8 V	1.71	1.8	1.89	V
V CCIO	1/O bullets power supply	1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	_	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V
VI	DC input voltage	_	-0.5	_	3.6	V
V _O	Output voltage	_	0	_	V _{CCIO}	V
Ţ	Operating junction temperature	Commercial	0	_	85	°C
1 j	Operating junction temperature	Industrial	-40	_	100	°C
+ (4)	Power supply ramp time	Standard POR	200 µs	_	100 ms	_
t _{RAMP} ⁽⁴⁾	rower supply famp time	Fast POR	200 µs	_	4 ms	_



⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

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Symbol	Description	Condition (V)	Ca	су	Unit	
Symbol	Description		-I3, -C4	–I5, –C5	-C6	
60- Ω and 120- Ω R_{T}	Internal parallel termination with calibration (60- Ω and 120- Ω setting)	$V_{CCIO} = 1.2$	-10 to +40	-10 to +40	-10 to +40	%
25- $\Omega R_{S_left_shift}$	Internal left shift series termination with calibration (25- $\Omega R_{s_left_shift}$ setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

OCT Without Calibration Resistance Tolerance Specifications

Table 1-9: OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

This table lists the Arria V OCT without calibration resistance to PVT changes.

Symbol	Description	Condition (V)	Re	sistanceTolerar	Unit	
Symbol	Description		–I3, –C4	–I5, –C5	-C6	Ont
$25-\Omega R_S$	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
$25-\Omega R_S$	Internal series termination without calibration (25- Ω setting)	$V_{CCIO} = 1.2$	±35	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.2$	±35	±50	±50	%
100-Ω R _D	Internal differential termination $(100-\Omega \text{ setting})$	$V_{CCIO} = 2.5$	±25	±40	±40	%



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I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Single-Ended I/O Standards

I/O Standard	dard V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹³⁾	Ι ⁽¹³⁾ (mΔ)
	Min	Тур	Max	Min	Мах	Min	Мах	Мах	Min	(mA)	IOH (IIIA)
3.3-V LVTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} – 0.2	2	-2
3.0-V LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} – 0.2	0.1	-0.1
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{\rm CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	V _{CCIO} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 1-14: Single-Ended I/O Standards for Arria V Devices

(13) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



• Transceiver Specifications for Arria V GT and ST Devices on page 1-29 Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition -	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description		Min	Тур	Max	Min	Тур	Max	Onic
Supported I/O standards	1.2 V PCM	L, 1.4 V PCM	IL,1.5 V PCML	, 2.5 V PCMI	., Differentia	LVPECL ⁽²³⁾	HCSL, and	LVDS
Input frequency from REFCLK input pins	—	27	—	710	27		710	MHz
Rise time	Measure at $\pm 60 \text{ mV of}$ differential signal ⁽²⁴⁾			400			400	ps
Fall time	Measure at $\pm 60 \text{ mV of}$ differential signal ⁽²⁴⁾	_		400	_		400	ps
Duty cycle	_	45	_	55	45	_	55	%
Peak-to-peak differential input voltage	—	200		300 ⁽²⁵⁾ / 2000	200	_	300 ⁽²⁵⁾ / 2000	mV



⁽²³⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

REFCLK performance requires to meet transmitter REFCLK phase noise specification. (24)

⁽²⁵⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			llnit		
symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit		
Supported I/O standards		1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS								
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps		
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V		
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V		
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V		
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V		



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

1-40 Transceiver Compliance Specification

Quartus Prime 1st			Quar	tus Prime V _{OD} Se	etting			
Post Tap Pre- Emphasis Setting	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	Unit
16	_	_	9.56	7.73	6.49		_	dB
17	_		10.43	8.39	7.02		_	dB
18	_		11.23	9.03	7.52		_	dB
19	_		12.18	9.7	8.02		_	dB
20	_		13.17	10.34	8.59		_	dB
21	_		14.2	11.1			_	dB
22	_		15.38	11.87			_	dB
23	_		_	12.67	_	_	_	dB
24	_		_	13.48			_	dB
25	_		_	14.37			_	dB
26	_						_	dB
27	_						_	dB
28	_	_	_	_	_	_	_	dB
29	_		_				_	dB
30	_						_	dB
31	_				_		_	dB

Related Information

SPICE Models for Altera Devices

Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
	Input clock frequency	-3 speed grade	5	—	800 ⁽⁶¹⁾	MHz
f		-4 speed grade	5		800 ⁽⁶¹⁾	MHz
IIN		–5 speed grade	5	_	750 ⁽⁶¹⁾	MHz
		-6 speed grade	5		625(61)	MHz
f _{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	_	5	_	325	MHz
f _{fINPFD}	Fractional input clock frequency to the PFD		50	_	160	MHz
	PLL voltage-controlled oscillator (VCO) operating range	-3 speed grade	600	—	1600	MHz
f (62)		-4 speed grade	600	_	1600	MHz
IVCO		–5 speed grade	600		1600	MHz
		-6 speed grade	600		1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	_	40		60	%
		-3 speed grade	_	_	500 ⁽⁶³⁾	MHz
f	Output frequency for internal global or	-4 speed grade	—	—	500 ⁽⁶³⁾	MHz
LOUT	regional clock	-5 speed grade	_	_	500 ⁽⁶³⁾	MHz
		-6 speed grade	_	_	400 ⁽⁶³⁾	MHz



⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
t _{CASC_OUTPJ_DC} ⁽⁶⁷⁾⁽⁷¹⁾	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$			175	ps (p-p)
	in cascaded PLLs	F _{OUT} < 100 MHz			17.5	mUI (p-p)
t _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_			±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	_	8	24	32	bits
k _{VALUE}	Numerator of fraction	_	128	8388608	2147483648	_
f _{RES}	Resolution of VCO frequency	$f_{INPFD} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz



⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

HPS JTAG Timing Specifications

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30	_	ns
t _{JCH}	TCK clock high time	14		ns
t _{JCL}	TCK clock low time	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2		ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3		ns
t _{JPH}	JTAG port hold time	5		ns
t _{JPCO}	JTAG port clock to output		12 ⁽⁹⁰⁾	ns
t _{JPZX}	JTAG port high impedance to valid output		14 ⁽⁹⁰⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance		14 ⁽⁹⁰⁾	ns

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 ⁽⁹¹⁾	ms

⁽⁹⁰⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

⁽⁹¹⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.



FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	Off	Off	1
EDD (9 bit wide)	On	Off	1
frr (o-bit wide)	Off	On	2
	On	On	2
	Off	Off	1
EDD (16 bit wide)	On	Off	2
fif (lo-bit wide)	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLKto-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs

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Altera Corporation



1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles



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	Symbol	Parameter	Typical	Unit
			0 (default)	ps
D _{OUTBUF}	Rising and/or falling edge delay	50	ps	
		100	ps	
		150	ps	

Glossary

Table 1-78: Glossary

Term	Definition	
Differential I/O standards	Receiver Input Waveforms	
	Single-Ended Waveform	
		Positive Channel (p) = V_{IH}
	V _{CM}	Negative Channel (n) $= V_{IL}$
		Ground
	Differential Waveform	
	VID	a 11
		p - n = 0 V



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Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 µA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹²⁴⁾
I _{XCVR-TX (DC)}	DC current per transceiver transmitter pin	100 mA
I _{XCVR-RX (DC)}	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

Symbol	Description	V _{CCIO} Conditions (V) ⁽¹²⁵⁾	Value ⁽¹²⁶⁾	Unit
R _{PU}		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

⁽¹²⁴⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.





 $^{^{(125)}}$ The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

 $^{^{(126)}}$ These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)			
	Min	Тур	Max	Min	Тур	Max	Min	Тур	Мах	
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 imes V_{ m CCIO}$	0.49 × V _{CCIO}	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$	$0.49 \times V_{ m CCIO}$	0.5 × VCCIO	$0.51 \times V_{CCIO}$	
SSTL-12 Class I, II	1.14	1.20	1.26	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$	0.49 × V _{CCIO}	0.5 × VCCIO	$0.51 \times V_{CCIO}$	
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V _{CCIO} /2	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V _{CCIO} /2	_	
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.53 \times V_{ m CCIO}$	_	V _{CCIO} /2	_	
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$			_	

Table 2-18: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	L.(mA)	I. (mA)
	Min	Max	Min	Max	Мах	Min	Max	Min		
SSTL-2 Class I	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7



2-44 Periphery Performance

Description	Min	Тур	Мах	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps



Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification

Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350



Table 2-55: DCLK-to-DATA[] Ratio for Arria V GZ Devices

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4
FPP ×32	Disabled	Disabled	1
	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8





Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

- 1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
- 3. After power-up, before and during configuration, CONF_DONE is low.
- 4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
- 6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.



2-70 Remote System Upgrades Circuitry Timing Specification

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
Variant		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽²²⁶⁾	250	_	ns
t _{RU_nRSTIMER} ⁽²²⁷⁾	250	_	ns

⁽²²³⁾ The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Date	Version	Changes
June 2016	2016.06.20	 Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table. Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table. Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table: True RSDS output standard: data rates of up to 230 Mbps True mini-LVDS output standard: data rates of up to 340 Mbps
December 2015	2015.12.16	 Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table. Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table. Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table. Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table.
June 2015	2015.06.16	 Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table. Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table.
January 2015	2015.01.30	 Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table. Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table. Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table.

