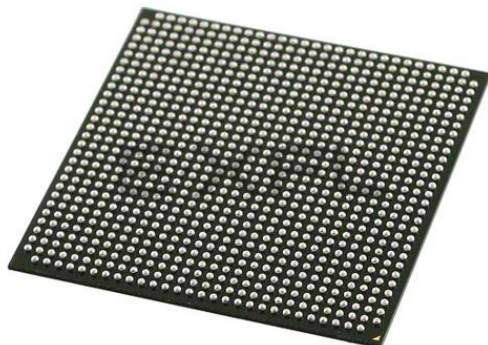




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA, FC (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxmb5e4f31i3n

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	–0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	–0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	–0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	–0.50	3.90	V
V _{CCIO}	I/O power supply	–0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	–0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	–0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V _{CCR_GXB}	Receiver power	–0.50	1.50	V
V _{CCT_GXB}	Transmitter power	–0.50	1.50	V
V _{CCL_GXB}	Transceiver clock network power	–0.50	1.50	V
V _I	DC input voltage	–0.50	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	–0.50	3.90	V

Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	–0.50	3.25	V
I _{OUT}	DC output current per pin	–25	40	mA
T _J	Operating junction temperature	–55	125	°C
T _{STG}	Storage temperature (no bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Transceiver Power Supply Operating Conditions

Table 1-4: Transceiver Power Supply Operating Conditions for Arria V Devices

Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.500	2.625	V
V _{CCA_GXBR}	Transceiver high voltage power (right side)				
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1.1/1.15 ⁽⁶⁾	1.14/1.18	V
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)				
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1.17	1.20	1.23	V
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)				
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1.1/1.15 ⁽⁶⁾	1.14/1.18	V
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)				
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1.17	1.20	1.23	V
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)				
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.500	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power (right side)				

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate ≤ 3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate > 3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIOMAX}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIOMAX}$	-30	—	30	μA

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V _{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold, high, sustaining current	I _{SUSH}	V _{IN} < V _{IH} (min)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus-hold, low, overdrive current	I _{ODL}	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold, high, overdrive current	I _{ODH}	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA

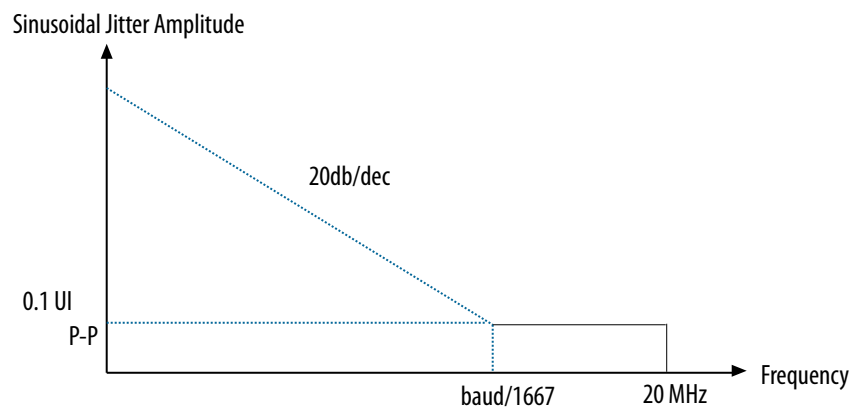
Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 1-16: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL}^{(14)} (mA)$	$I_{OH}^{(14)} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.608$	$V_{TT} + 0.608$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.603$	$V_{TT} + 0.603$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
SSTL-125	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	-I3, -C4	-I5, -C5	-C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock ($t_{\text{DQS_PSERR}}$) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	-I3, -C4	-I5, -C5	-C6	Unit
2	40	80	80	ps

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

$$\text{Maximum input jitter} = \text{Input clock period} \times \text{Divide value (N)} \times 0.02$$

Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

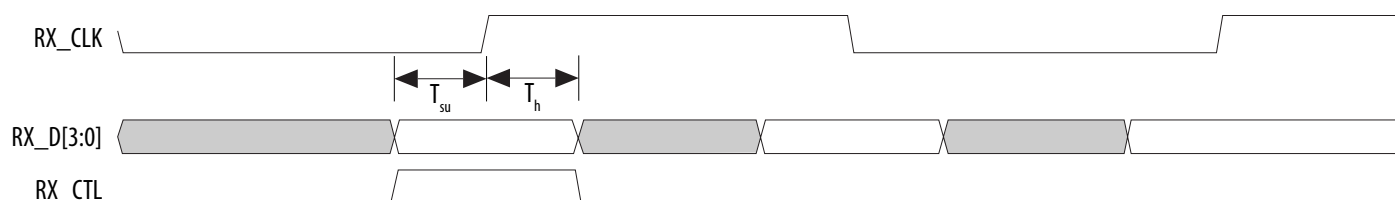
Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

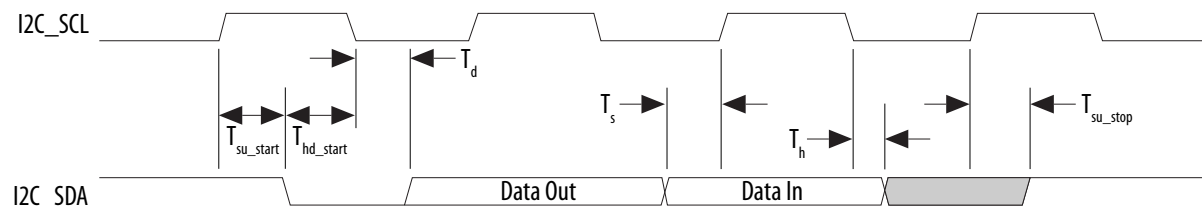
Symbol	Description	Min	Typ	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
T _{dutycycle}	SCLK_OUT duty cycle	45	—	55	%
T _{dssfrst}	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T _{dio}	I/O data output delay	–1	—	1	ns
T _{din_start}	Input data valid start	—	—	$(2 + R_{\text{delay}}) \times T_{\text{qspi_clk}} - 7.52^{(85)}$	ns

Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_h	RX_D/RX_CTL hold time	1	—	ns

Figure 1-14: RGMII RX Timing Diagram**Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10	—	20	ns
T_s	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 1-16: I²C Timing Diagram

NAND Timing Characteristics

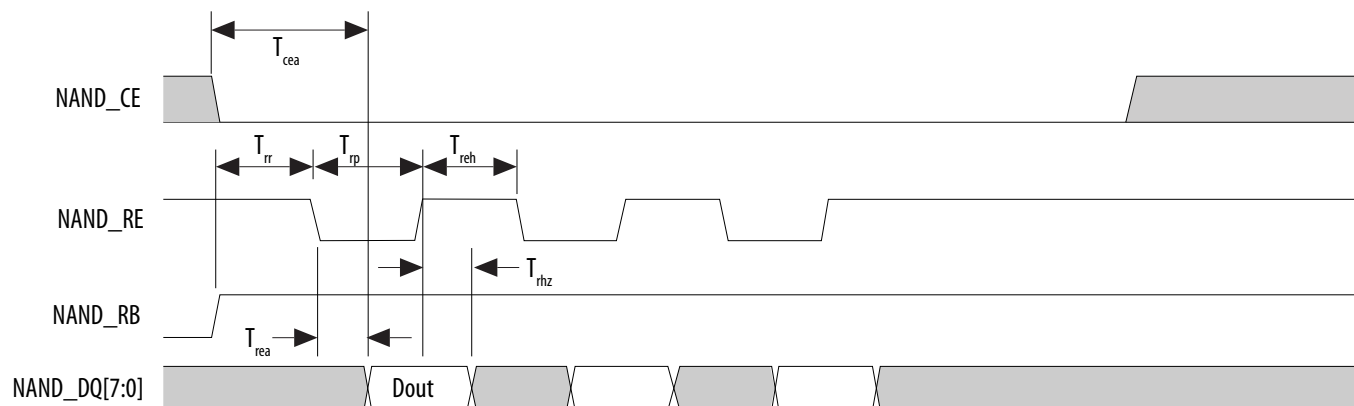
Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
$T_{wp}^{(89)}$	Write enable pulse width	10	—	ns
$T_{wh}^{(89)}$	Write enable hold time	7	—	ns
$T_{rp}^{(89)}$	Read enable pulse width	10	—	ns
$T_{reh}^{(89)}$	Read enable hold time	7	—	ns
$T_{clesu}^{(89)}$	Command latch enable to write enable setup time	10	—	ns
$T_{cleh}^{(89)}$	Command latch enable to write enable hold time	5	—	ns
$T_{cesu}^{(89)}$	Chip enable to write enable setup time	15	—	ns
$T_{ceh}^{(89)}$	Chip enable to write enable hold time	5	—	ns
$T_{alesu}^{(89)}$	Address latch enable to write enable setup time	10	—	ns
$T_{aleh}^{(89)}$	Address latch enable to write enable hold time	5	—	ns
$T_{dsu}^{(89)}$	Data to write enable setup time	10	—	ns

⁽⁸⁹⁾ Timing of the NAND interface is controlled through the NAND configuration registers.

Figure 1-20: NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 1-61: ARM Trace Timing Requirements for Arria V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 μ s. The pulse width is based on a debounce clock frequency of 1 MHz.

Symbol	Parameter	Minimum	Maximum	Unit
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁹⁴⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁹⁵⁾	μs
t _{CF2CK} ⁽⁹⁶⁾	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽⁹⁶⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CL}	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CLK}	DCLK period	$1/f_{\text{MAX}}$	—	s
f _{MAX}	DCLK frequency (FPP × 8/ × 16)	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁹⁷⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (T _{init} × CLKUSR period)	—	—
T _{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

⁽⁹⁴⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁹⁵⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁹⁶⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽⁹⁷⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Term	Definition
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes
December 2016	2016.12.09	- Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table. - Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table. - Updated T_{init} specifications in the following tables: - FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices - FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices - AS Timing Parameters for AS $\times 1$ and $\times 4$ Configurations in Arria V Devices - PS Timing Parameters for Arria V Devices
June 2016	2016.06.10	- Changed pin capacitance to maximum values. - Updated SPI Master Timing Requirements for Arria V Devices table. - Added T_{su} and T_h specifications. - Removed T_{dinmax} specifications. - Updated SPI Master Timing Diagram. - Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Arria V Devices table.

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R _S	Internal series termination with calibration (25-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34-Ω and 40-Ω R _S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V _{CCIO} = 1.2 V	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	%
25-Ω R _{S_left_shift}	Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±40	±40	%

Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	—	100	—	710	100	—	710	MHz

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	MHz

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Receiver**Table 2-24: Receiver Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) ⁽¹⁴³⁾ , ⁽¹⁴⁴⁾	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS) ⁽¹⁴³⁾ , ⁽¹⁴⁴⁾	—	600	—	12500	600	—	10312.5	Mbps
Absolute V _{MAX} for a receiver pin ⁽¹⁴⁵⁾	—	—	—	1.2	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	—	−0.4	—	—	−0.4	—	—	V

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)
V _{OD} differential peak to peak typical	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Symbol	Parameter	Min	Typ	Max	Unit
k_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency ($f_{\text{INPFD}} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Related Information

- [Duty Cycle Distortion \(DCD\) Specifications](#) on page 2-56
- [DLL Range Specifications](#) on page 2-53

DSP Block Specifications**Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices**

Mode	Performance			Unit
	C3, I3L	C4	I4	
Modes using One DSP Block				
Three 9×9	480	420		MHz
One 18×18	480	420	400	MHz
Two partial 18×18 (or 16×16)	480	420	400	MHz
One 27×27	400	350		MHz
One 36×18	400	350		MHz
One sum of two 18×18 (One sum of two 16×16)	400	350		MHz
One sum of square	400	350		MHz
One 18×18 plus $36(a \times b) + c$	400	350		MHz
Modes using Two DSP Blocks				
Three 18×18	400	350		MHz
One sum of four 18×18	380	300		MHz

JTAG Configuration Specifications

Table 2-54: JTAG Timing Parameters and Values for Arria V GZ Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCP}	TCK clock period	167 ⁽²⁰³⁾	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	2	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 ⁽²⁰⁴⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽²⁰⁴⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽²⁰⁴⁾	ns

Fast Passive Parallel (FPP) Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

⁽²⁰³⁾ The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

⁽²⁰⁴⁾ A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Date	Version	Changes
July 2014	3.8	- Updated Table 21. - Updated Table 22 V_{OCM} (DC Coupled) condition. - Updated the DCLK note to Figure 6, Figure 7, and Figure 9. - Added note to Table 5 and Table 6. - Added the DCLK specification to Table 50. - Added note to Table 51. - Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	- Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. - Updated “PLL Specifications”.
August 2013	3.5	Updated Table 28.
August 2013	3.4	- Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. - Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	- Added Table 23. - Updated Table 5, Table 22, Table 26, and Table 57. - Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	- Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. - Updated “Maximum Allowed Overshoot and Undershoot Voltage”.
December 2012	3.0	Initial release.