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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56303ag100

1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Type	State During Reset	State During Stop or Wait	Signal Description
D[0–23]	Input/ Output	Ignored Input	Last state: *Input*: Ignored *Output*: Tri-stated	**Data Bus**—When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tri-stated.

1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
AA[0–3]	Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals.
$\overline{\text{RAS}}$[0–3]	Output		**Row Address Strobe**—When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated.
$\overline{\text{TA}}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56303 is the bus master and there is no external bus activity, or the DSP56303 is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. To use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion; otherwise, improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously depending on the setting of the TAS bit in the Operating Mode Register. $\overline{\text{TA}}$ functionality cannot be used during DRAM type accesses; otherwise improper operation may result.
$\overline{\text{BR}}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Asserted when the DSP requests bus mastership. $\overline{\text{BR}}$ is deasserted when the DSP no longer needs the bus. $\overline{\text{BR}}$ may be asserted or deasserted independently of whether the DSP56303 is a bus master or a bus slave. Bus “parking” allows $\overline{\text{BR}}$ to be deasserted even though the DSP56303 is the bus master. (See the description of bus “parking” in the $\overline{\text{BB}}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{\text{BR}}$ to be asserted under software control even though the DSP does not need the bus. $\overline{\text{BR}}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{\text{BR}}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{\text{BR}}$ is deasserted and the arbitration is reset to the bus slave state.

1.8 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the serial peripheral interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PC0	Input or Output		**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.
SRD0	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received.
PC4	Input or Output		**Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.
2. This timing depends on several settings:
   • For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
   • For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
   • For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
   • For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
   • PLC value for PLL disable is 0.
   • The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100 percent tested.
4. Value depends on clock source:
   • For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
   • For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
   • When the V_{CC} is valid, but the other “required $\overline{\text{RESET}}$ duration” conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. If PLL does not lose lock.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF.
7. WS = number of wait states (measured in clock cycles, number of T_C).
8. Use the expression to compute a maximum value.

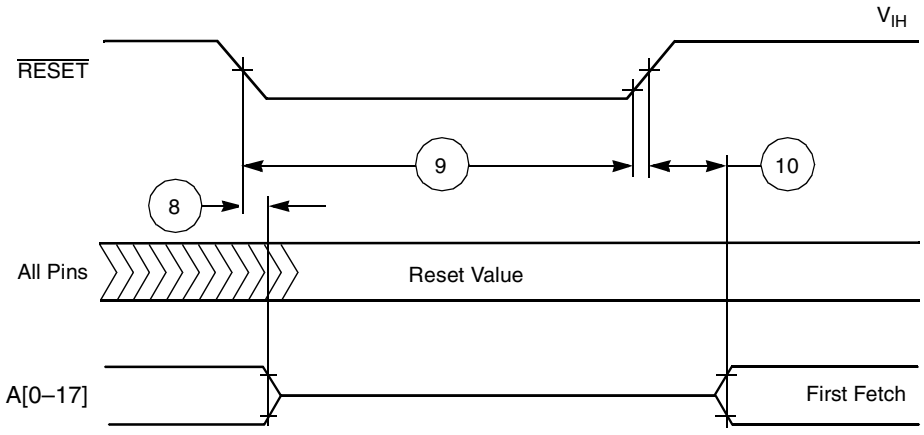

Figure 2-3. Reset Timing

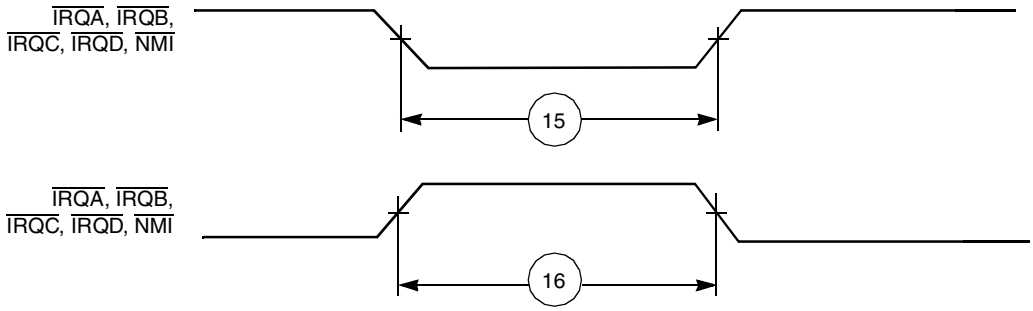

Figure 2-6. External Interrupt Timing (Negative Edge-Triggered)

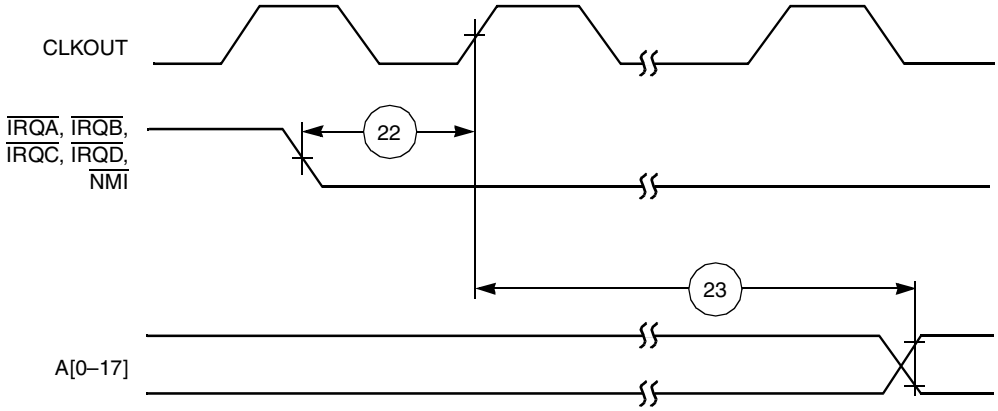

Figure 2-7. Synchronous Interrupt from Wait State Timing

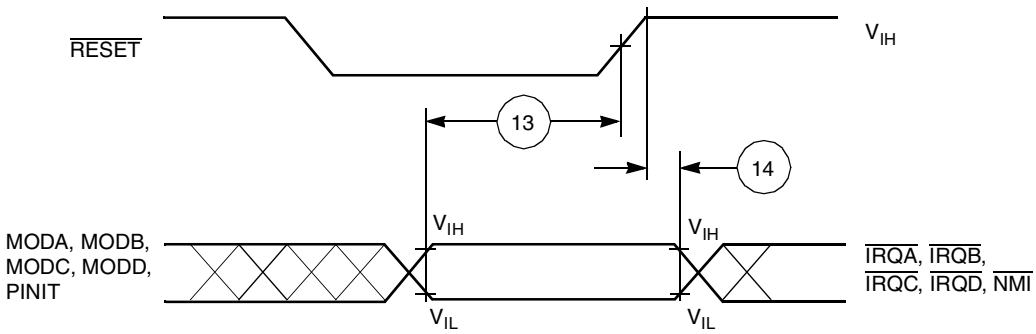

Figure 2-8. Operating Mode Select Timing

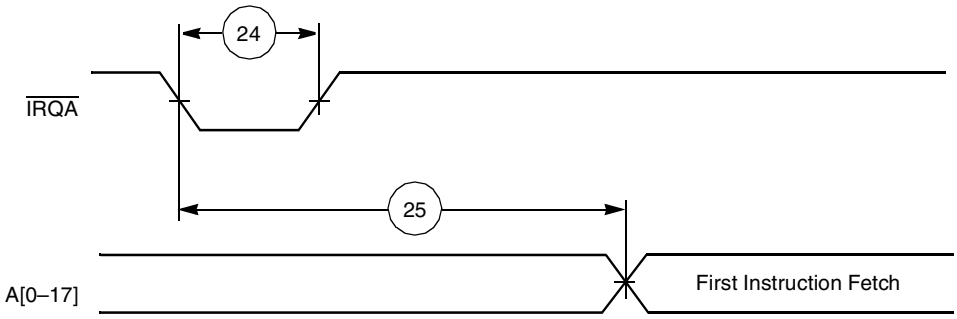

Figure 2-9. Recovery from Stop State Using $\overline{\text{IRQA}}$

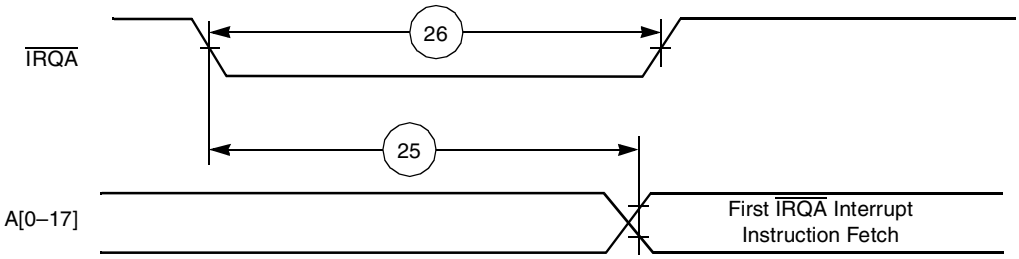

Figure 2-10. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

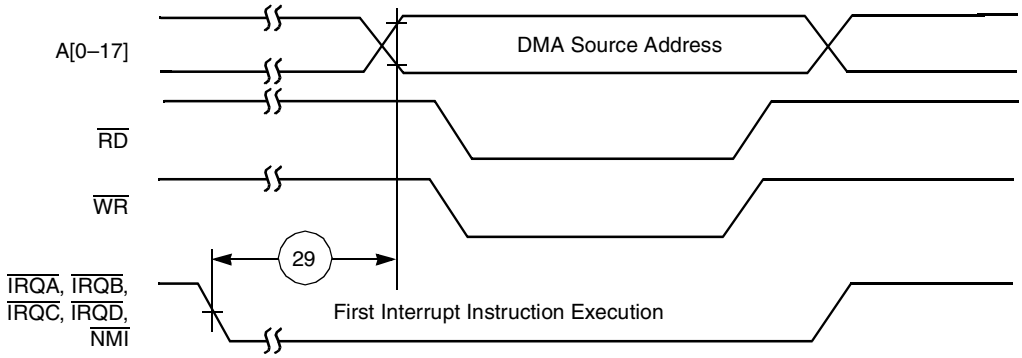

Figure 2-11. External Memory Access (DMA Source) Timing

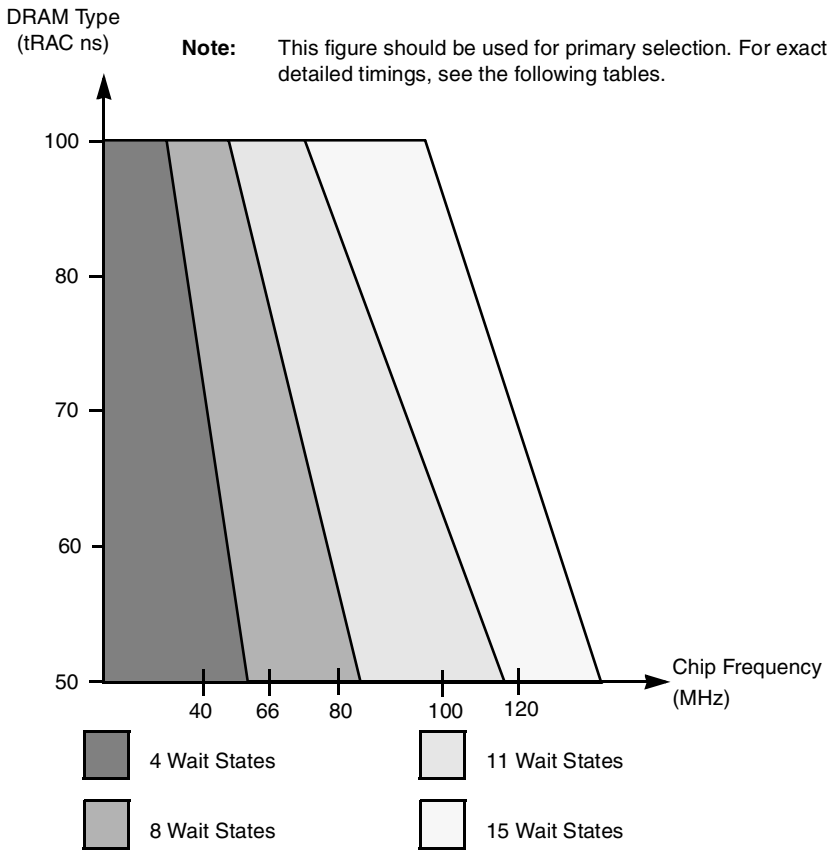

Figure 2-17. DRAM Out-of-Page Wait State Selection Guide

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2]

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$6.25 \times T_C - 7.0$	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$3.75 \times T_C - 7.0$	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	$4.5 \times T_C - 7.0$	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 4.0$	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 4.0$	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 6.0$	36.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	38.5	—	ns

2.5.5.5 Asynchronous Bus Arbitration Timings

Table 2-15. Asynchronous Bus Timings[1, 2]

No.	Characteristics	Expression[3]	100 MHz[4]		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion[5]	2.5 × Tc + 5	—	30	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion[5]	2 × Tc + 5	25	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
2. If Asynchronous Arbitration mode is active, none of the timings in **Table 2-14** is required.
3. An expression is used to compute the maximum or minimum value listed, as appropriate.
4. Asynchronous Arbitration mode is recommended for operation at 100 MHz.
5. In order to guarantee timings 250, and 251, BG inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in **Figure 2-26**.

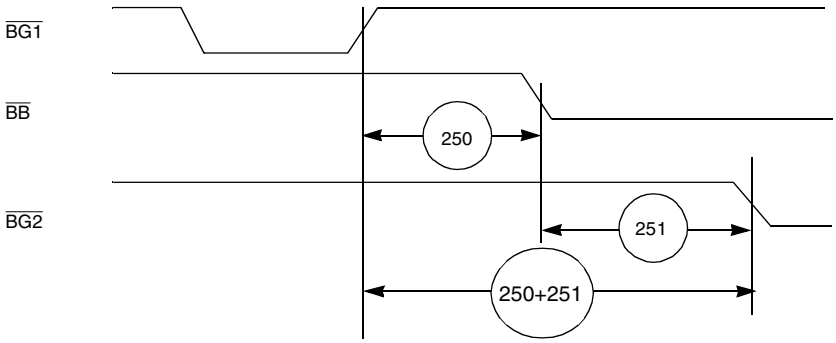

Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

2.5.8 ESSI0/ESSI1 Timing

Table 2-18. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	30.0 40.0	— —	x ck i ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C$ - 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C$ –10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in set-up time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr)[7] high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl)[7] high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input set-up before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (word-length) low			— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	x ck i ck	ns

2.5.9 Timer Timing

Table 2-19. Timer Timing[1]

No.	Characteristics	Expression[2]	100 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	22.0	—	ns
481	TIO High	$2 \times T_C + 2.0$	22.0	—	ns
482	Timer set-up time from TIO (Input) assertion to CLKOUT rising edge		9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	$10.25 \times T_C + 1.0$	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 5.5 —	 — 24.8	 ns ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 5.5 —	 — 24.8	 ns ns

Notes: 1. V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF.
2. An expression is used to compute the number listed as the minimum or maximum value as appropriate.

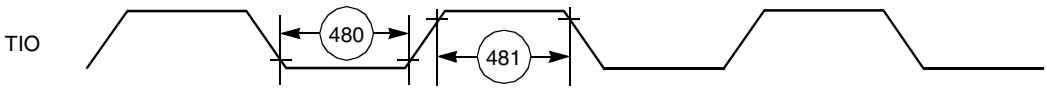

Figure 2-40. TIO Timer Event Input Restrictions

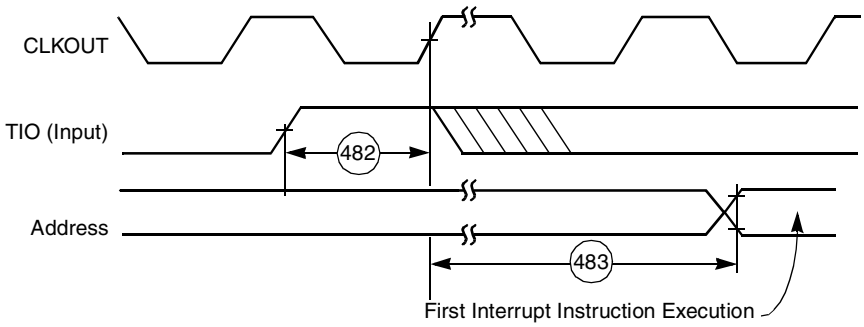

Figure 2-41. Timer Interrupt Generation

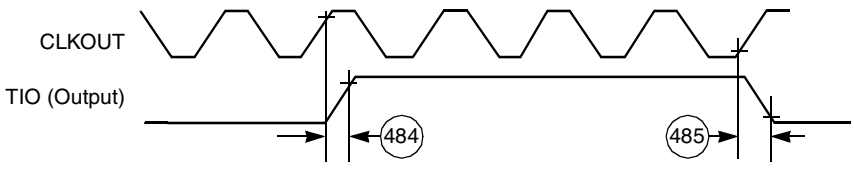

Figure 2-42. External Pulse Generation

Packaging 3

This section includes diagrams of the DSP56303 package pin-outs and tables showing how the signals described in **Chapter 1**, are allocated for each package.

The DSP56303 is available in two package types:

- 144-pin Thin Quad Flat Pack (TQFP)
- 196-pin Molded Array Process-Ball Grid Array (MAP-BGA)

Table 3-1. DSP56303 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	SRD1 or PD4	26	GND_S	51	AA2/$\overline{RAS2}$
2	STD1 or PD5	27	TIO2	52	$\overline{CAS}$
3	SC02 or PC2	28	TIO1	53	XTAL
4	SC01 or PC1	29	TIO0	54	GND_Q
5	$\overline{DE}$	30	$\overline{HCS}$/HCS, HA10, or PB13	55	EXTAL
6	PINIT/$\overline{NMI}$	31	HA2, HA9, or PB10	56	V_{CCQ}
7	SRD0 or PC4	32	HA1, HA8, or PB9	57	V_{CCC}
8	V_{CCS}	33	HA0, $\overline{HAS}$/HAS, or PB8	58	GND_C
9	GND_S	34	H7, HAD7, or PB7	59	CLKOUT
10	STD0 or PC5	35	H6, HAD6, or PB6	60	BCLK
11	SC10 or PD0	36	H5, HAD5, or PB5	61	$\overline{BCLK}$
12	SC00 or PC0	37	H4, HAD4, or PB4	62	$\overline{TA}$
13	RXD or PE0	38	V_{CCH}	63	$\overline{BR}$
14	TXD or PE1	39	GND_H	64	$\overline{BB}$
15	SCLK or PE2	40	H3, HAD3, or PB3	65	V_{CCC}
16	SCK1 or PD3	41	H2, HAD2, or PB2	66	GND_C
17	SCK0 or PC3	42	H1, HAD1, or PB1	67	$\overline{WR}$
18	V_{CCQ}	43	H0, HAD0, or PB0	68	$\overline{RD}$
19	GND_Q	44	$\overline{RESET}$	69	AA1/$\overline{RAS1}$
20	Not Connected (NC), reserved	45	V_{CCP}	70	AA0/$\overline{RAS0}$
21	$\overline{HDS}$/HDS, $\overline{HWR}$/HWR, or PB12	46	PCAP	71	$\overline{BG}$
22	HRW, $\overline{HRD}$/HRD, or PB11	47	GND_P	72	A0
23	$\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, or PB15	48	GND_{P1}	73	A1
24	$\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, or PB14	49	Not Connected (NC), reserved	74	V_{CCA}
25	V_{CCS}	50	AA3/$\overline{RAS3}$	75	GND_A

Table 3-2. DSP56303 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	72	$\overline{BG}$	71	D7	109
A1	73	$\overline{BR}$	63	D8	110
A10	88	$\overline{CAS}$	52	D9	113
A11	89	CLKOUT	59	$\overline{DE}$	5
A12	92	D0	100	EXTAL	55
A13	93	D1	101	GND_A	75
A14	94	D10	114	GND_A	81
A15	97	D11	115	GND_A	87
A16	98	D12	116	GND_A	96
A17	99	D13	117	GND_C	58
A2	76	D14	118	GND_C	66
A3	77	D15	121	GND_D	104
A4	78	D16	122	GND_D	112
A5	79	D17	123	GND_D	120
A6	82	D18	124	GND_D	130
A7	83	D19	125	GND_H	39
A8	84	D2	102	GND_P	47
A9	85	D20	128	GND_{P1}	48
AA0	70	D21	131	GND_Q	19
AA1	69	D22	132	GND_Q	54
AA2	51	D23	133	GND_Q	90
AA3	50	D3	105	GND_Q	127
$\overline{BB}$	64	D4	106	GND_S	9
BCLK	60	D5	107	GND_S	26
$\overline{BCLK}$	61	D6	108	H0	43

Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{\text{RAS0}}$	70	SRD1	1	V_{CCC}	57
$\overline{\text{RAS1}}$	69	STD0	10	V_{CCC}	65
$\overline{\text{RAS2}}$	51	STD1	2	V_{CCD}	103
$\overline{\text{RAS3}}$	50	$\overline{\text{TA}}$	62	V_{CCD}	111
$\overline{\text{RD}}$	68	TCK	141	V_{CCD}	119
$\overline{\text{RESET}}$	44	TDI	140	V_{CCD}	129
RXD	13	TDO	139	V_{CCH}	38
SC00	12	TIO0	29	V_{CCP}	45
SC01	4	TIO1	28	V_{CCQ}	18
SC02	3	TIO2	27	V_{CCQ}	56
SC10	11	TMS	142	V_{CCQ}	91
SC11	144	$\overline{\text{TRST}}$	138	V_{CCQ}	126
SC12	143	TXD	14	V_{CCS}	8
SCK0	17	V_{CCA}	74	V_{CCS}	25
SCK1	16	V_{CCA}	80	$\overline{\text{WR}}$	67
SCLK	15	V_{CCA}	86	XTAL	53
SRD0	7	V_{CCA}	95		

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	Not Connected (NC), reserved	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQ}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	F8	GND	J9	H4	N3
GND	F9	GND	J10	H5	P2
GND	F10	GND	J11	H6	N1
GND	F11	GND	K4	H7	N2
GND	G4	GND	K5	HA0	M3
GND	G5	GND	K6	HA1	M1
GND	G6	GND	K7	HA10	L1
GND	G7	GND	K8	HA2	M2
GND	G8	GND	K9	HA8	M1
GND	G9	GND	K10	HA9	M2
GND	G10	GND	K11	$\overline{\text{HACK}}$/HACK	J1
GND	G11	GND	L4	HAD0	M5
GND	H4	GND	L5	HAD1	P4
GND	H5	GND	L6	HAD2	N4
GND	H6	GND	L7	HAD3	P3
GND	H7	GND	L8	HAD4	N3
GND	H8	GND	L9	HAD5	P2
GND	H9	GND	L10	HAD6	N1
GND	H10	GND	L11	HAD7	N2
GND	H11	GND_P	N6	$\overline{\text{HAS}}$/HAS	M3
GND	J4	GND_{P1}	P6	$\overline{\text{HCS}}$/HCS	L1
GND	J5	H0	M5	$\overline{\text{HDS}}$/HDS	J3
GND	J6	H1	P4	$\overline{\text{HRD}}$/HRD	J2
GND	J7	H2	N4	$\overline{\text{HREQ}}$/HREQ	K2
GND	J8	H3	P3	$\overline{\text{HRRQ}}$/HRRQ	J1

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HRW	J2	PB14	K2	PE2	G2
$\overline{\text{HTRQ}}$/HTRQ	K2	PB15	J1	PINIT	D1
$\overline{\text{HWR}}$/HWR	J3	PB2	N4	$\overline{\text{RAS0}}$	N13
$\overline{\text{IRQA}}$	C4	PB3	P3	$\overline{\text{RAS1}}$	P12
$\overline{\text{IRQB}}$	A5	PB4	N3	$\overline{\text{RAS2}}$	P7
$\overline{\text{IRQC}}$	C5	PB5	P2	$\overline{\text{RAS3}}$	N7
$\overline{\text{IRQD}}$	B5	PB6	N1	$\overline{\text{RD}}$	M12
MODA	C4	PB7	N2	$\overline{\text{RESET}}$	N5
MODB	A5	PB8	M3	RXD	F1
MODC	C5	PB9	M1	SC00	F3
MODD	B5	PC0	F3	SC01	D2
NC	A1	PC1	D2	SC02	C1
NC	A14	PC2	C1	SC10	F2
NC	B14	PC3	H3	SC11	A2
NC	H1	PC4	E3	SC12	B2
NC	M7	PC5	E1	SCK0	H3
NC	P1	PCAP	P5	SCK1	G1
NC	P14	PD0	F2	SCLK	G2
NMI	D1	PD1	A2	SRD0	E3
PB0	M5	PD2	B2	SRD1	B1
PB1	P4	PD3	G1	STD0	E1
PB10	M2	PD4	B1	STD1	C2
PB11	J2	PD5	C2	$\overline{\text{TA}}$	P10
PB12	J3	PE0	F1	TCK	C3
PB13	L1	PE1	G3	TDI	B3

```
        dc      $6A39E8
        dc      $81E801
        dc      $C666A6
        dc      $46F8E7
        dc      $AAEC94
        dc      $24233D
        dc      $802732
        dc      $2E3C83
        dc      $A43E00
        dc      $C2B639
        dc      $85A47E
        dc      $ABFDDF
        dc      $F3A2C
        dc      $2D7CF5
        dc      $E16A8A
        dc      $ECB8FB
        dc      $4BED18
        dc      $43F371
        dc      $83A556
        dc      $E1E9D7
        dc      $ACA2C4
        dc      $8135AD
        dc      $2CE0E2
        dc      $8F2C73
        dc      $432730
        dc      $A87FA9
        dc      $4A292E
        dc      $A63CCF
        dc      $6BA65C
        dc      $E06D65
        dc      $1AA3A
        dc      $A1B6EB
        dc      $48AC48
        dc      $EF7AE1
        dc      $6E3006
        dc      $62F6C7
        dc      $6064F4
        dc      $87E41D
        dc      $CB2692
        dc      $2C3863
        dc      $C6BC60
        dc      $43A519
        dc      $6139DE
        dc      $ADF7BF
        dc      $4B3E8C
        dc      $6079D5
        dc      $E0F5EA
        dc      $8230DB
        dc      $A3B778
        dc      $2BFE51
        dc      $E0A6B6
        dc      $68FFB7
        dc      $28F324
        dc      $8F2E8D
        dc      $667842
        dc      $83E053
        dc      $A1FD90
        dc      $6B2689
        dc      $85B68E
        dc      $622EAF
```

```
M_DI EQU 12                          ; Data Input
M_DO EQU 13                          ; Data Output
M_PCE EQU  15                        ; Prescaled Clock Enable
M_TOF EQU 20                         ; Timer Overflow Flag
M_TCF EQU 21                         ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000                    ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22

;      Timer Control Bits
M_TC0 EQU 4                          ; Timer Control 0
M_TC1 EQU 5                          ; Timer Control 1
M_TC2 EQU 6                          ; Timer Control 2
M_TC3 EQU 7                          ; Timer Control 3


;------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4                    ; DMA Status Register
M_DOR0 EQU $FFFFF3                   ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2                   ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1                   ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0                   ; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF                   ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE                   ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED                   ; DMA0 Counter
M_DCR0 EQU $FFFFEC                   ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB                   ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA                   ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9                   ; DMA1 Counter
M_DCR1 EQU $FFFFE8                   ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7                   ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6                   ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5                   ; DMA2 Counter
M_DCR2 EQU $FFFFE4                   ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3                   ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2                   ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1                   ; DMA3 Counter
M_DCR3 EQU $FFFFE0                   ; DMA3 Control Register
```

```
;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF                  ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE                  ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD                  ; DMA4 Counter
M_DCR4 EQU $FFFFDC                  ; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB                  ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA                  ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9                  ; DMA5 Counter
M_DCR5 EQU $FFFFD8                  ; DMA5 Control Register

;       DMA Control Register

M_DSS EQU $3                        ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0                        ; DMA Source Memory space 0
M_DSS1 EQU 1                        ; DMA Source Memory space 1
M_DDS EQU $C                        ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2                        ; DMA Destination Memory Space 0
M_DDS1 EQU 3                        ; DMA Destination Memory Space 1
M_DAM EQU $3f0                      ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0  EQU 4                       ; DMA Address Mode 0
M_DAM1  EQU 5                       ; DMA Address Mode 1
M_DAM2  EQU 6                       ; DMA Address Mode 2
M_DAM3  EQU 7                       ; DMA Address Mode 3
M_DAM4  EQU 8                       ; DMA Address Mode 4
M_DAM5  EQU 9                       ; DMA Address Mode 5
M_D3D EQU 10                        ; DMA Three Dimensional Mode
M_DRS EQU $F800                     ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16                       ; DMA Continuous Mode
M_DPR EQU $60000                    ; DMA Channel Priority
M_DPR0 EQU 17                       ; DMA Channel Priority Level (low)
M_DPR1 EQU 18                       ; DMA Channel Priority Level (high)
M_DTM EQU $380000                   ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19                       ; DMA Transfer Mode 0
M_DTM1 EQU 20                       ; DMA Transfer Mode 1
M_DTM2 EQU 21                       ; DMA Transfer Mode 2
M_DIE EQU 22                        ; DMA Interrupt Enable bit
M_DE EQU 23                         ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F                       ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0                        ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1                        ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2                        ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3                        ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4                        ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5                        ; DMA Channel Transfer Done Status 5
M_DACT EQU  8                       ; DMA Active State
M_DCH EQU  $E00                     ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU  9                       ; DMA Active Channel 0
M_DCH1 EQU  10                      ; DMA Active Channel 1
M_DCH2 EQU  11                      ; DMA Active Channel 2

;---------------------------------------------------------------------------
```

```
;
;       EQUATES for Phase Locked Loop (PLL)
;
;------------------------------------------------------------------------

;       Register Addresses Of PLL

M_PCTL EQU $FFFFFD                  ; PLL Control Register

;       PLL Control Register

M_MF EQU $FFF                       ; Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000                      ; Division Factor Bits Mask (DF0-DF2)
M_XTLR EQU 15                       ; XTAL Range select bit
M_XTLD EQU 16                       ; XTAL Disable Bit
M_PSTP EQU 17                       ; STOP Processing State Bit
M_PEN EQU 18                        ; PLL Enable Bit
M_PCOD EQU 19                       ; PLL Clock Output Disable Bit
M_PD EQU $F00000                    ; PreDivider Factor Bits Mask (PD0-PD3)



;------------------------------------------------------------------------
;
;       EQUATES for BIU
;
;------------------------------------------------------------------------

;       Register Addresses Of BIU


M_BCR EQU $FFFFFB                   ; Bus Control Register
M_DCR EQU $FFFFFA                   ; DRAM Control Register
M_AAR0 EQU $FFFFF9                  ; Address Attribute Register 0
M_AAR1 EQU $FFFFF8                  ; Address Attribute Register 1
M_AAR2 EQU $FFFFF7                  ; Address Attribute Register 2
M_AAR3 EQU $FFFFF6                  ; Address Attribute Register 3
M_IDR EQU  $FFFFF5                  ; ID Register

;       Bus Control Register

M_BA0W EQU $1F                      ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0                     ; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00                    ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000                    ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000                  ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21                        ; Bus State
M_BLH EQU 22                        ; Bus Lock Hold
M_BRH EQU 23                        ; Bus Request Hold

;       DRAM Control Register

M_BCW EQU $3                        ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C                        ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300                      ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11                       ; Page Logic Enable
M_BME EQU 12                        ; Mastership Enable
M_BRE EQU 13                        ; Refresh Enable
M_BSTR EQU 14                       ; Software Triggered Refresh
M_BRF EQU $7F8000                   ; Refresh Rate Bits Mask (BRF0-BRF7)
```