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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

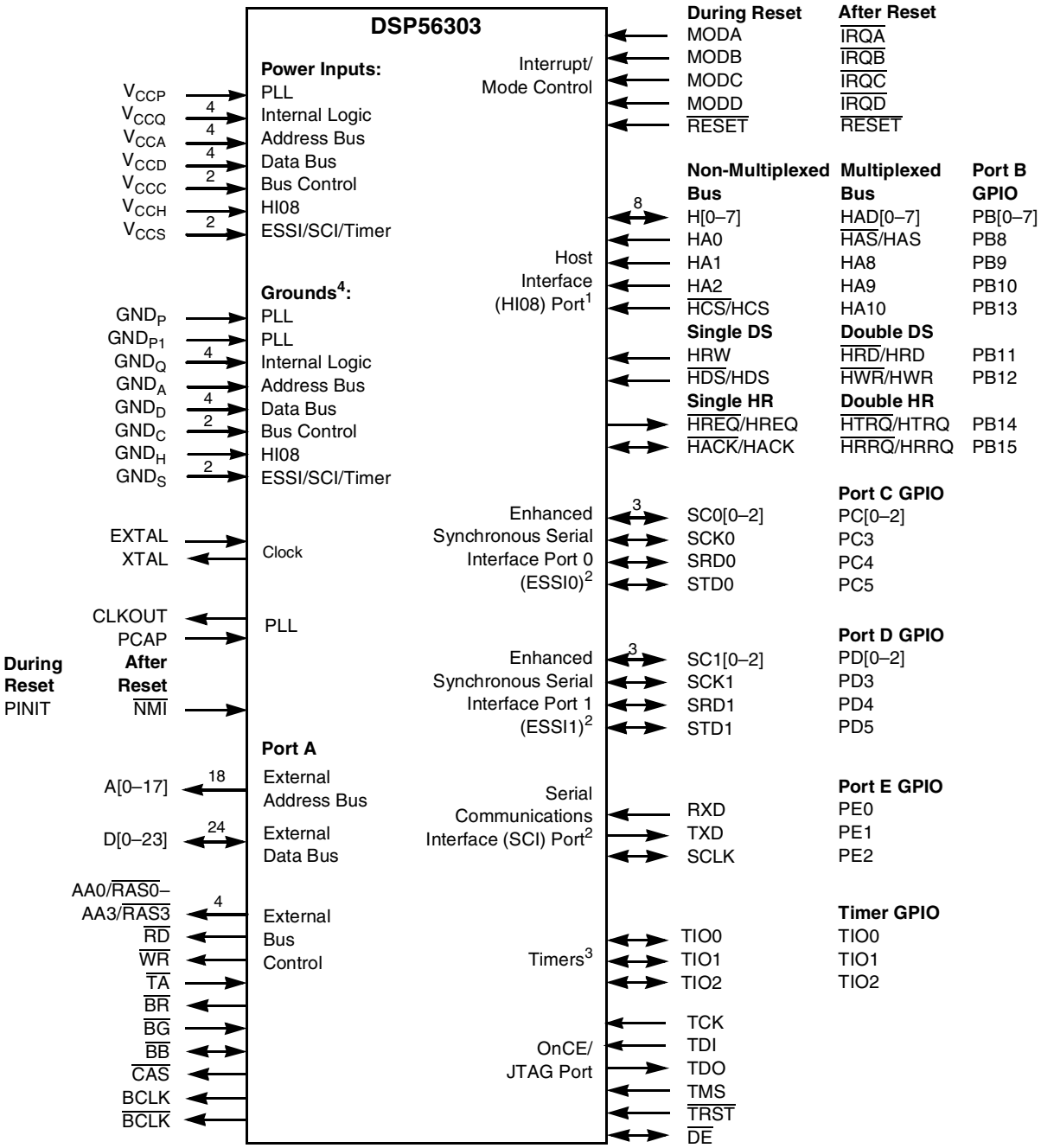
Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56303ag100b1

Features

Table 1 lists the features of the DSP56303 device.

Table 1. DSP56303 Features

<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>High-Performance DSP56300 Core</td><td>
• 100 million multiply-accumulates per second (MMACS) with a 100 MHz clock at 3.3 V nominal
• Object code compatible with the DSP56000 core with highly parallel instruction set
• Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
• Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
• Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
• Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination
• Hardware debugging support including on-chip emulation (OnCE‘) module, Joint Test Action Group (JTAG) test access port (TAP)
</td></tr>
<tr><td>Internal Peripherals</td><td>
• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs
• Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
• Serial communications interface (SCI) with baud rate generator
• Triple timer module
• Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled
</td></tr>
<tr><td>Internal Memories</td><td>
• 192 × 24-bit bootstrap ROM
• 8 K × 24-bit RAM total
• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:
<table>
<tr><th>Program RAM Size</th><th>Instruction Cache Size</th><th>X Data RAM Size</th><th>Y Data RAM Size</th><th>Instruction Cache</th><th>Switch Mode</th></tr>
<tr><td>4096 × 24-bit</td><td>0</td><td>2048 × 24-bit</td><td>2048 × 24-bit</td><td>disabled</td><td>disabled</td></tr>
<tr><td>3072 × 24-bit</td><td>1024 × 24-bit</td><td>2048 × 24-bit</td><td>2048 × 24-bit</td><td>enabled</td><td>disabled</td></tr>
<tr><td>2048 × 24-bit</td><td>0</td><td>3072 × 24-bit</td><td>3072 × 24-bit</td><td>disabled</td><td>enabled</td></tr>
<tr><td>1024 × 24-bit</td><td>1024 × 24-bit</td><td>3072 × 24-bit</td><td>3072 × 24-bit</td><td>enabled</td><td>enabled</td></tr>
</table>
</td></tr>
<tr><td>External Memory Expansion</td><td>
• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines
• Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines
• External memory expansion port
• Chip select logic for glueless interface to static random access memory (SRAMs)
• Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)
</td></tr>
<tr><td>Power Dissipation</td><td>
• Very low-power CMOS design
• Wait and Stop low-power standby modes
• Fully static design specified to operate down to 0 Hz (dc)
• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
</td></tr>
<tr><td>Packaging</td><td>
• 144-pin TQFP package in lead-free or lead-bearing versions
• 196-pin molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions
</td></tr>
</table>



Notes:

1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternatively as GPIO signals (PB[0–15]). Signals with dual designations (for example, HAS/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
3. TIO[0–2] can be configured as GPIO signals.
4. Ground connections shown in this figure are for the TQFP package. In the MAP-BGA package, in addition to the GND_P and GND_{P1} connections, there are 64 GND connections to a common internal package ground plane.

Figure 1-1. Signals Identified by Functional Group

Table 2-3. DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit

Notes:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
2. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 100°C.
3. In order to obtain these results, all inputs must be terminated (that is, not allowed to float).
4. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
5. Periodically sampled and not 100 percent tested.
6. V_{CC} = 3.3 V ±0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CC} and the maximum V_{ILX} should be no higher than 0.1 × V_{CC}.

2.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.5.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—

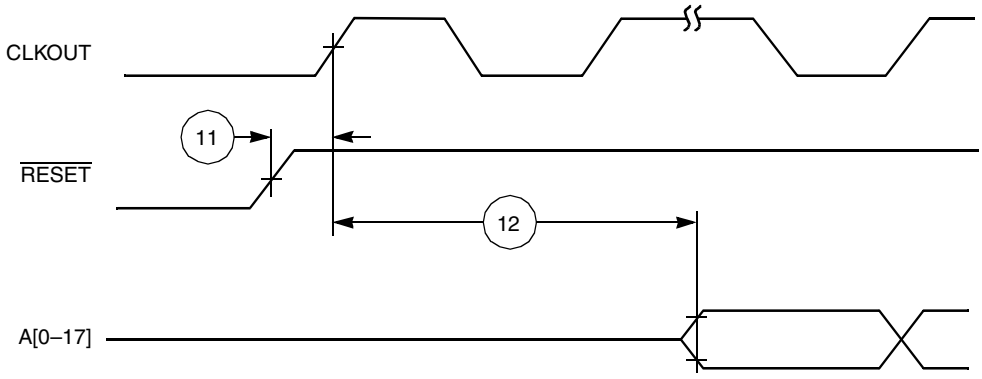
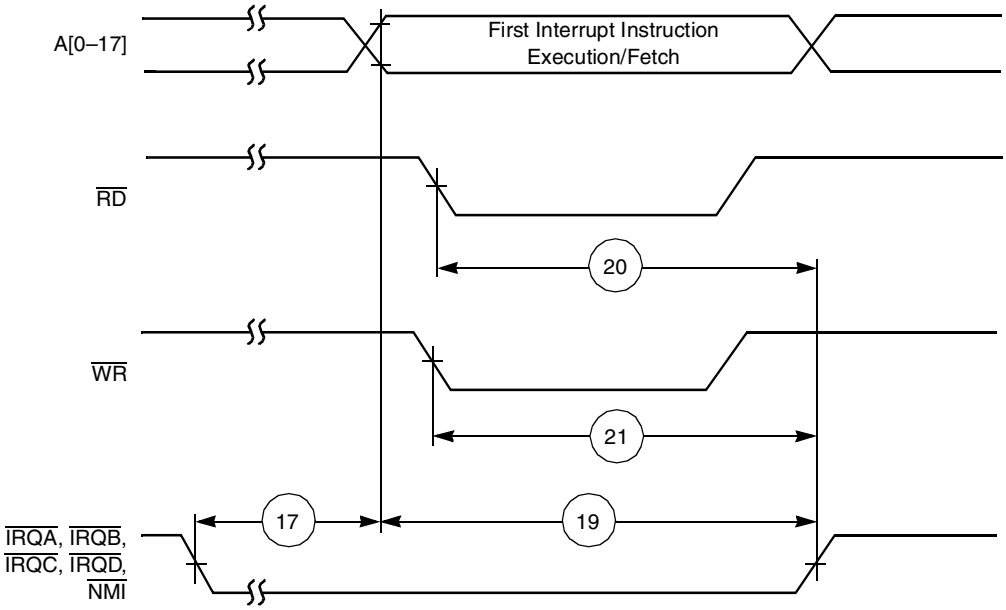
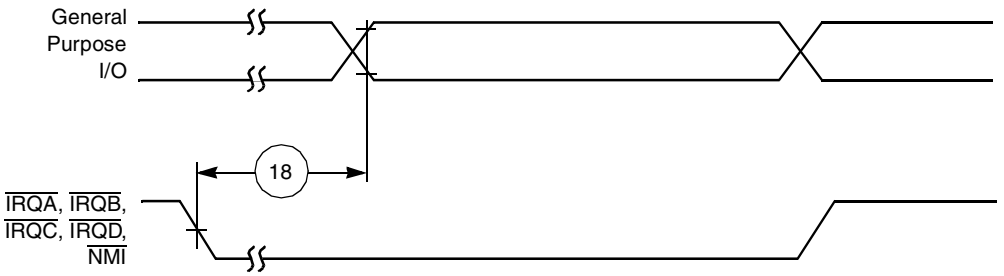


Figure 2-4. Synchronous Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-5. External Fast Interrupt Timing

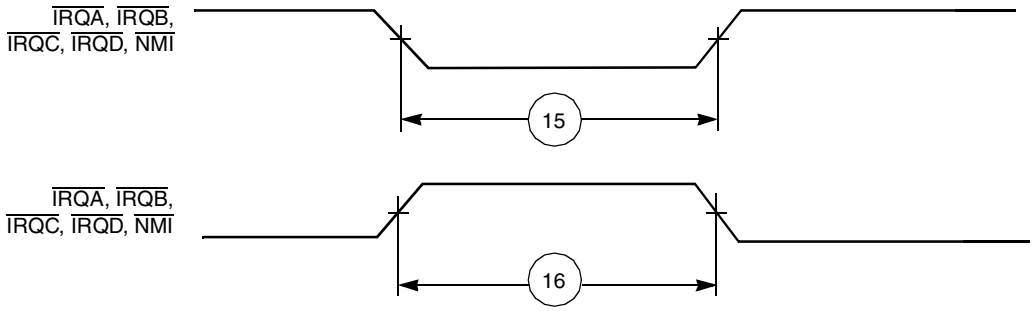


Figure 2-6. External Interrupt Timing (Negative Edge-Triggered)

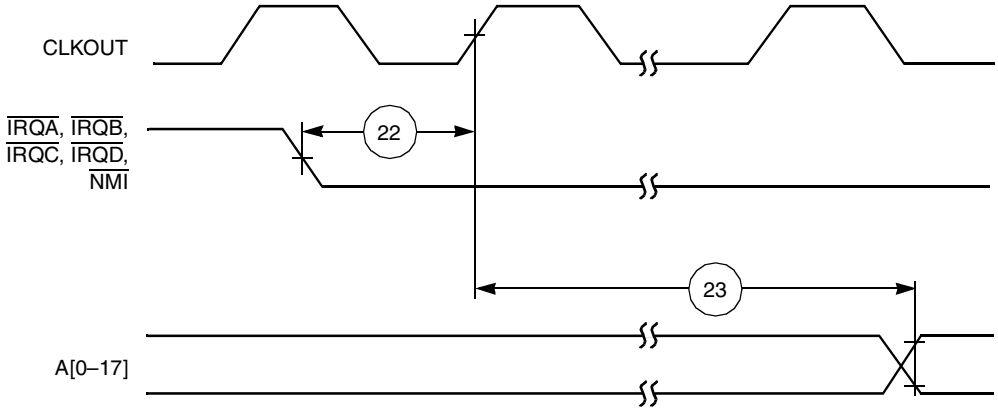


Figure 2-7. Synchronous Interrupt from Wait State Timing

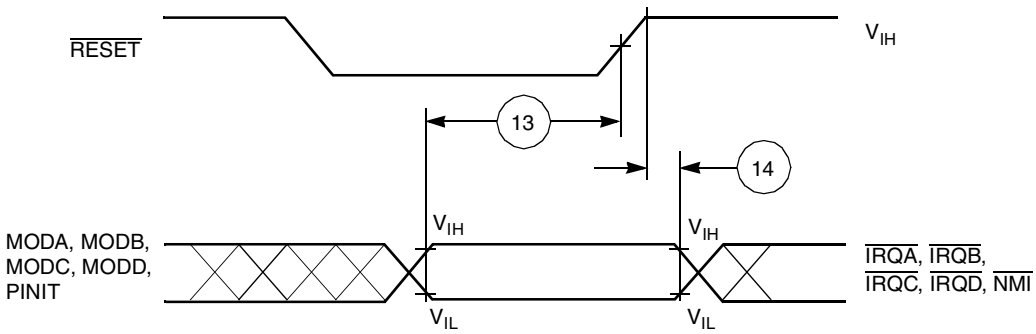


Figure 2-8. Operating Mode Select Timing

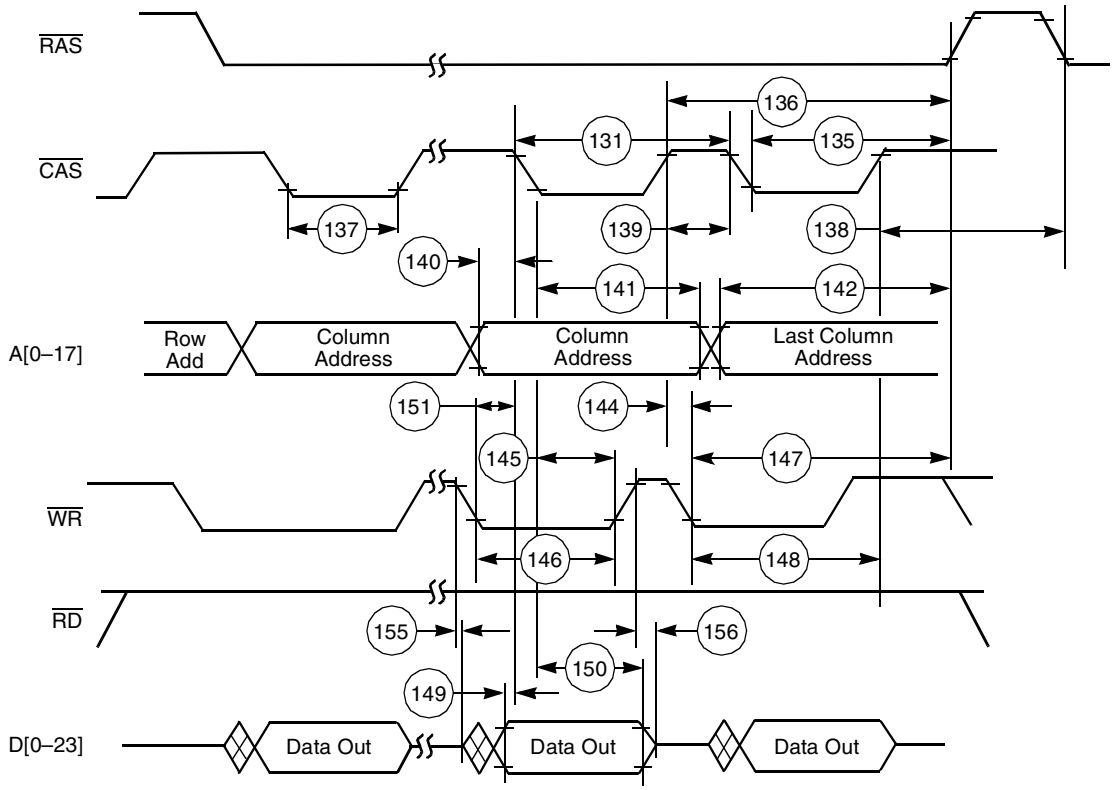


Figure 2-15. DRAM Page Mode Write Accesses

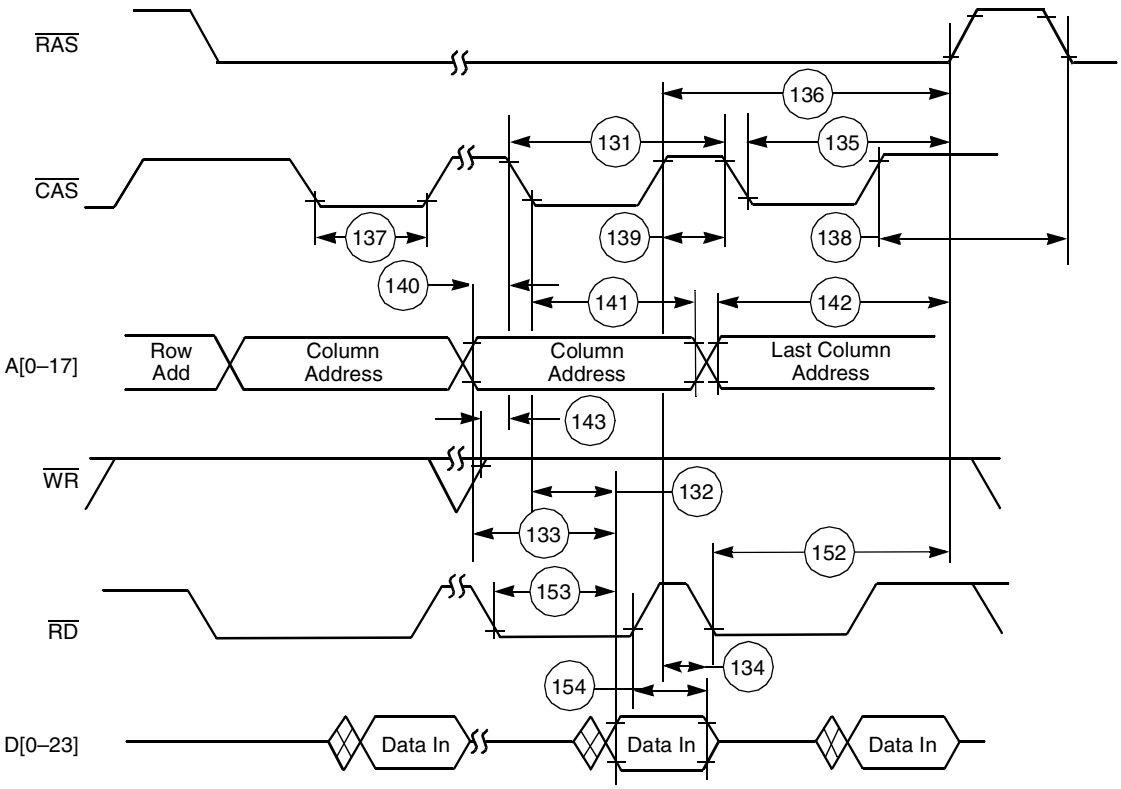


Figure 2-16. DRAM Page Mode Read Accesses

2.5.6 Host Interface Timing

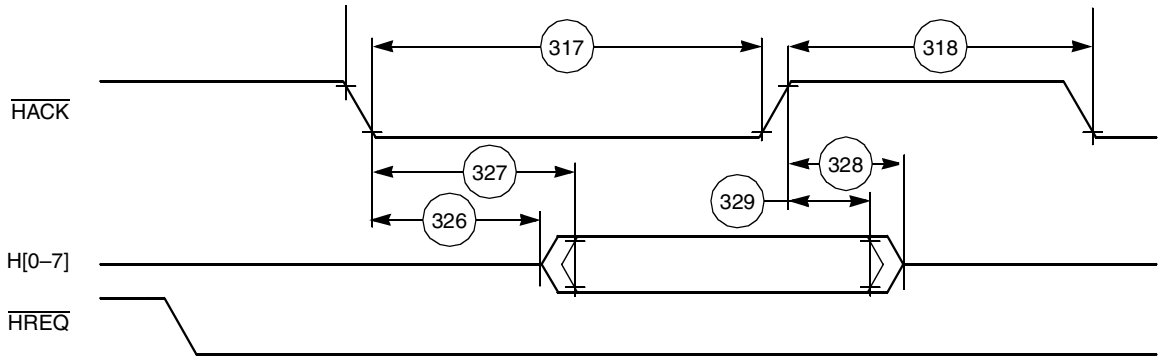
Table 2-16. Host Interface Timings[1,2,12]

No.	Characteristic[10]	Expression	100 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[5] $\overline{HACK}$ assertion width	$T_C + 9.9$	19.9	—	ns
318	Read data strobe deassertion width[5] $\overline{HACK}$ deassertion width		9.9	—	ns
319	Read data strobe deassertion width[5] after "Last Data Register" reads[8,11], or between two consecutive CVR, ICR, or ISR reads[3] $\overline{HACK}$ deassertion width after "Last Data Register" reads[8,11]	$2.5 \times T_C + 6.6$	31.6	—	ns
320	Write data strobe assertion width[6]		13.2	—	ns
321	Write data strobe deassertion width[8] $\overline{HACK}$ write deassertion width • after ICR, CVR and "Last Data Register" writes • after IVR writes, or after TXH:TXM:TXL writes (with HLEND= 0), or after TXL:TXM:TXH writes (with HLEND = 1)	$2.5 \times T_C + 6.6$	31.8 16.5	— —	ns ns
322	$\overline{HAS}$ assertion width		9.9	—	ns
323	$\overline{HAS}$ deassertion to data strobe assertion[4]		0.0	—	ns
324	Host data input setup time before write data strobe deassertion[6]		9.9	—	ns
325	Host data input hold time after write data strobe deassertion[6]		3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[5] $\overline{HACK}$ assertion to output data active from high impedance		3.3	—	ns
327	Read data strobe assertion to output data valid[5] $\overline{HACK}$ assertion to output data valid		—	24.5	ns
328	Read data strobe deassertion to output data high impedance[5] $\overline{HACK}$ deassertion to output data high impedance		—	9.9	ns
329	Output data hold time after read data strobe deassertion[5] Output data hold time after $\overline{HACK}$ deassertion		3.3	—	ns
330	$\overline{HCS}$ assertion to read data strobe deassertion[5]	$T_C + 9.9$	19.9	—	ns
331	$\overline{HCS}$ assertion to write data strobe deassertion[6]		9.9	—	ns
332	$\overline{HCS}$ assertion to output data valid		—	19.3	ns
333	$\overline{HCS}$ hold time after data strobe deassertion[4]		0.0	—	ns
334	Address (HAD[0–7]) setup time before $\overline{HAS}$ deassertion (HMUX=1)		4.6	—	ns
335	Address (HAD[0–7]) hold time after $\overline{HAS}$ deassertion (HMUX=1)		3.3	—	ns
336	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[4] • Read • Write		 0 4.6	 — —	 ns ns
337	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[4]		3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for "Last Data Register" read[5, 7, 8]	$T_C + 5.3$	15.3	—	ns
339	Delay from write data strobe deassertion to host request assertion for "Last Data Register" write[6, 7, 8]	$1.5 \times T_C + 5.3$	20.3	—	ns

Table 2-16. Host Interface Timings[1,2,12] (Continued)

No.	Characteristic[10]	Expression	100 MHz		Unit
			Min	Max	
340	Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=0)[4, 7, 8]		—	19.3	ns
341	Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=1, open drain host request)[4, 7, 8, 9]		—	300.0	ns

Notes:
1. See the Programmer's Model section in the chapter on the HI08 in the *DSP56303 User's Manual*.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. This timing is applicable only if two consecutive reads from one of these registers are executed.
4. The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (HDS) in the Single Data Strobe mode.
5. The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
6. The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
7. The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
8. The "Last Data Register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Big Endian mode (HLEND = 0; HLEND is the Interface Control Register bit 7—ICR[7]), or RXH/TXH in the Little Endian mode (HLEND = 1).
9. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
10. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
11. This timing is applicable only if a read from the "Last Data Register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.
12. After the external host writes a new value to the ICR, the HI08 is ready for operation after three DSP clock cycles (3 × Tc).



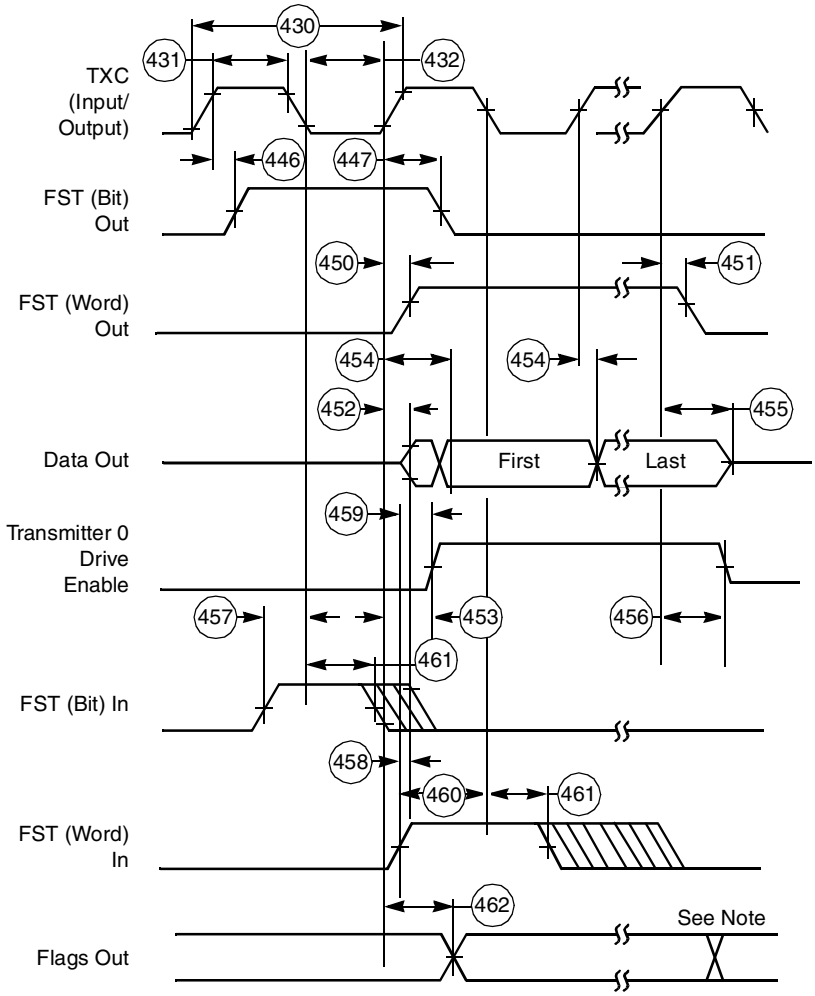
Note: The IVR is read only by an MC680xx host processor in non-multiplexed mode.

Figure 2-27. Host Interrupt Vector Register (IVR) Read Timing Diagram

2.5.8 ESSI0/ESSI1 Timing

Table 2-18. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	30.0 40.0	— —	x ck i ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C$ - 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C$ –10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in set-up time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr)[7] high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl)[7] high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input set-up before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (word-length) low			— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	x ck i ck	ns



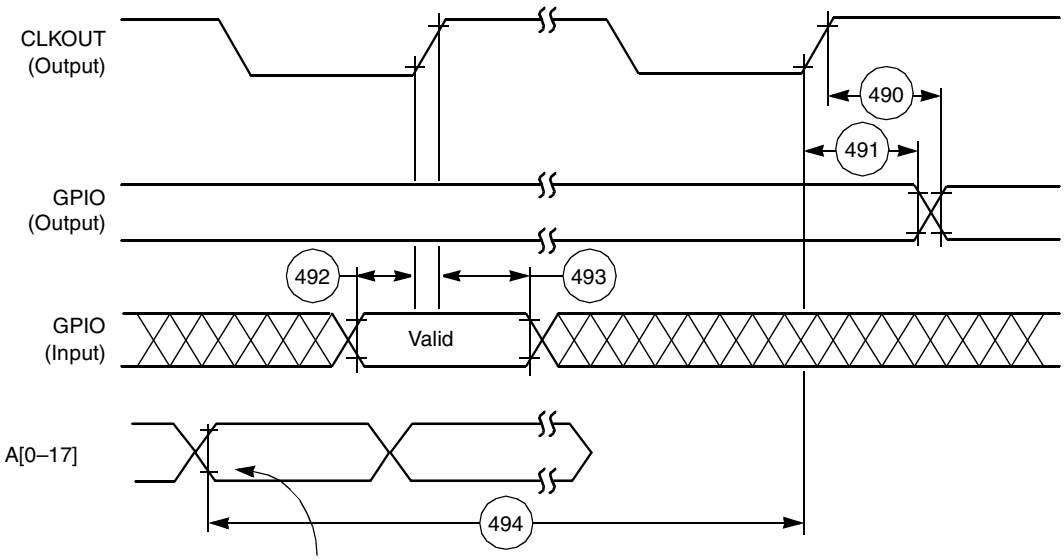
Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-38. ESSI Transmitter Timing

2.5.10 GPIO Timing

Table 2-20. GPIO Timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: 6.75 × T_C	67.5	—	ns
Note:	V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF				



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-43. GPIO Timing

Packaging 3

This section includes diagrams of the DSP56303 package pin-outs and tables showing how the signals described in **Chapter 1**, are allocated for each package.

The DSP56303 is available in two package types:

- 144-pin Thin Quad Flat Pack (TQFP)
- 196-pin Molded Array Process-Ball Grid Array (MAP-BGA)

Table 3-2. DSP56303 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	72	$\overline{BG}$	71	D7	109
A1	73	$\overline{BR}$	63	D8	110
A10	88	$\overline{CAS}$	52	D9	113
A11	89	CLKOUT	59	$\overline{DE}$	5
A12	92	D0	100	EXTAL	55
A13	93	D1	101	GND_A	75
A14	94	D10	114	GND_A	81
A15	97	D11	115	GND_A	87
A16	98	D12	116	GND_A	96
A17	99	D13	117	GND_C	58
A2	76	D14	118	GND_C	66
A3	77	D15	121	GND_D	104
A4	78	D16	122	GND_D	112
A5	79	D17	123	GND_D	120
A6	82	D18	124	GND_D	130
A7	83	D19	125	GND_H	39
A8	84	D2	102	GND_P	47
A9	85	D20	128	GND_{P1}	48
AA0	70	D21	131	GND_Q	19
AA1	69	D22	132	GND_Q	54
AA2	51	D23	133	GND_Q	90
AA3	50	D3	105	GND_Q	127
$\overline{BB}$	64	D4	106	GND_S	9
BCLK	60	D5	107	GND_S	26
$\overline{BCLK}$	61	D6	108	H0	43

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
M1	HA1, HA8, or PB9	N3	H4, HAD4, or PB4	P5	PCAP
M2	HA2, HA9, or PB10	N4	H2, HAD2, or PB2	P6	GND_{P1}
M3	HA0, $\overline{HAS}$/HAS, or PB8	N5	$\overline{RESET}$	P7	AA2/$\overline{RAS2}$
M4	V_{CCH}	N6	GND_P	P8	XTAL
M5	H0, HAD0, or PB0	N7	AA3/$\overline{RAS3}$	P9	V_{CCC}
M6	V_{CCP}	N8	$\overline{CAS}$	P10	$\overline{TA}$
M7	NC	N9	V_{CCQ}	P11	$\overline{BB}$
M8	EXTAL	N10	BCLK	P12	AA1/$\overline{RAS1}$
M9	CLKOUT	N11	$\overline{BR}$	P13	$\overline{BG}$
M10	$\overline{BCLK}$	N12	V_{CCC}	P14	NC
M11	$\overline{WR}$	N13	AA0/$\overline{RAS0}$		
M12	$\overline{RD}$	N14	A0		

Notes: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike in the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.

- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.
- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{\text{RESET}}$ must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of $\overline{\text{RESET}}$.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $I = C \times V \times f$

Where:

C	=	node/pin capacitance
V	=	voltage swing
f	=	frequency of node/pin toggle

Example 4-1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.

Power Consumption Benchmark A

The following benchmark program evaluates DSP56303 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;************************************************************************
;************************************************************************
;*                                                                      *
;*                    CHECKS   Typical Power Consumption                *
;*                                                                      *
;************************************************************************

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0; INTERNAL X-data memory starting address
INT_YDAT  EQU $0; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "intequ.asm"

        list

        org     P:START
;
        movep #$0243FF,x:M_BCR ;; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
        movep   #$0d0000,x:M_PCTL      ; XTAL disable
                                       ; PLL enable
                                       ; CLKOUT disable
;
; Load the program
;
        move    #INT_PROG,r0
        move    #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,p:(r0)+
        nop
PLOAD_LOOP
;
; Load the X-data
;
        move    #INT_XDAT,r0
        move    #XDAT_START,r1
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
```

```
M_SCRIE EQU 11                          ; SCI Receive Interrupt Enable
M_SCTIE EQU 12                          ; SCI Transmit Interrupt Enable
M_TMIE EQU 13                           ; Timer Interrupt Enable
M_TIR EQU 14                            ; Timer Interrupt Rate
M_SCKP EQU 15                           ; SCI Clock Polarity
M_REIE EQU 16                           ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0                            ; Transmitter Empty
M_TDRE EQU 1                            ; Transmit Data Register Empty
M_RDRF EQU 2                            ; Receive Data Register Full
M_IDLE EQU 3                            ; Idle Line Flag
M_OR EQU 4                              ; Overrun Error Flag
M_PE EQU 5                              ; Parity Error
M_FE EQU 6                              ; Framing Error Flag
M_R8 EQU 7                              ; Received Bit 8 (R8) Address

;       SCI Clock Control Register

M_CD EQU $FFF                           ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                            ; Clock Out Divider
M_SCP EQU 13                            ; Clock Prescaler
M_RCM EQU 14                            ; Receive Clock Mode Source Bit
M_TCM EQU 15                            ; Transmit Clock Source Bit

;---------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;---------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC                      ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB                      ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA                      ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9                      ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8                       ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7                    ; SSI0 Status Register
M_CRB0 EQU $FFFFB6                      ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5                      ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4                     ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3                     ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2                     ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1                     ; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC                      ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB                      ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA                      ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9                      ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8                       ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7                    ; SSI1 Status Register
M_CRB1 EQU $FFFFA6                      ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5                      ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4                     ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3                     ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2                     ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1                     ; SSI1 Receive Slot Mask Register B
```

```
M_DI EQU 12                          ; Data Input
M_DO EQU 13                          ; Data Output
M_PCE EQU  15                        ; Prescaled Clock Enable
M_TOF EQU 20                         ; Timer Overflow Flag
M_TCF EQU 21                         ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000                    ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22

;      Timer Control Bits
M_TC0 EQU 4                          ; Timer Control 0
M_TC1 EQU 5                          ; Timer Control 1
M_TC2 EQU 6                          ; Timer Control 2
M_TC3 EQU 7                          ; Timer Control 3


;------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4                    ; DMA Status Register
M_DOR0 EQU $FFFFF3                   ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2                   ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1                   ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0                   ; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF                   ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE                   ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED                   ; DMA0 Counter
M_DCR0 EQU $FFFFEC                   ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB                   ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA                   ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9                   ; DMA1 Counter
M_DCR1 EQU $FFFFE8                   ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7                   ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6                   ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5                   ; DMA2 Counter
M_DCR2 EQU $FFFFE4                   ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3                   ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2                   ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1                   ; DMA3 Counter
M_DCR3 EQU $FFFFE0                   ; DMA3 Control Register
```