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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56303ag100r2

Target Applications

Examples include:

- Multi-line voice/data/fax processing
- Video conferencing
- Audio applications
- Control

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56303 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56303 Documentation

Name	Description	Order Number
DSP56303 User's Manual	Detailed functional description of the DSP56303 memory configuration, operation, and register programming	DSP56303UM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56303 product website

1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Schmitt-trigger Input	**Reset**—Places the chip in the Reset state and resets the internal phase generator. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after powerup.
MODA	Input	Schmitt-trigger Input	**Mode Select A**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQA}}$	Input		**External Interrupt Request A**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the STOP or WAIT standby state and $\overline{\text{IRQA}}$ is asserted, the processor exits the STOP or WAIT state.
MODB	Input	Schmitt-trigger Input	**Mode Select B**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQB}}$	Input		**External Interrupt Request B**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQB}}$ is asserted, the processor exits the WAIT state.
MODC	Input	Schmitt-trigger Input	**Mode Select C**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQC}}$	Input		**External Interrupt Request C**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQC}}$ is asserted, the processor exits the WAIT state.
MODD	Input	Schmitt-trigger Input	**Mode Select D**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQD}}$	Input		**External Interrupt Request D**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQD}}$ is asserted, the processor exits the WAIT state.
Note: These signals are all 5 V tolerant.			

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1 PD3	Input/Output Input or Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. **Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1 PD4	Input Input or Output	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received. **Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1 PD5	Output Input or Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted. **Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.
Notes: **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, the signal is tri-stated. **2.** The Wait processing state does not affect the signal state. **3.** All inputs are 5 V tolerant.			

Specifications 2

The DSP56303 is fabricated in high-density CMOS with transistor-transistor logic (TTL) compatible inputs and outputs.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

2.2 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +4.0	V
All input voltages excluding “5 V tolerant” inputs	V_{IN}	GND −0.3 to V_{CC} + 0.3	V
All “5 V tolerant” input voltages[2]	V_{IN5}	GND −0.3 to 5.5	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	−40 to +100	°C
Storage temperature	T_{STG}	−55 to +150	°C

Notes:
1. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
2. At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

2.3 Thermal Characteristics

Table 2-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	MAP-BGA[3] Value	MAP-BGA[4] Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	56	57	28	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	11	15	—	°C/W
Thermal characterization parameter	Ψ_{JT}	7	8	—	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per JEDEC Specification JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values. See note 1 for test board conditions.
4. These are simulated values. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

2.4 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage • D[0–23], $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{TA}}$ • MOD[1]/$\overline{\text{IRQ}}$[1], $\overline{\text{RESET}}$, PINIT/$\overline{\text{NMI}}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	V_{IH} V_{IHP} V_{IHX}	2.0 2.0 $0.8 \times V_{CC}$	— — —	V_{CC} 5.25 V_{CC}	V V V
Input low voltage • D[0–23], $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{TA}}$, MOD[1]/$\overline{\text{IRQ}}$[1], $\overline{\text{RESET}}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	V_{IL} V_{ILP} V_{ILX}	–0.3 –0.3 –0.3	— — —	0.8 0.8 $0.2 \times V_{CC}$	V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7] • CMOS (I_{OH} = –10 µA)[5]	V_{OH}	2.4 $V_{CC} - 0.01$	— —	— —	V V
Output low voltage • TTL (I_{OL} = 1.6 mA, open-drain pins I_{OL} = 6.7 mA)[5,7] • CMOS (I_{OL} = 10 µA)[5]	V_{OL}	— —	— —	0.4 0.01	V V
Internal supply current[2]: • In Normal mode • In Wait mode[3] • In Stop mode[4]	I_{CCI} I_{CCW} I_{CCS}	— — —	127 7.5 100	— — —	mA mA µA
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Table 2-3. DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit

Notes:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
2. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 100°C.
3. In order to obtain these results, all inputs must be terminated (that is, not allowed to float).
4. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
5. Periodically sampled and not 100 percent tested.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CC} and the maximum V_{ILX} should be no higher than 0.1 × V_{CC}.

2.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.5.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—

2.5.5 External Memory Expansion Port (Port A)

2.5.5.1 SRAM Timing

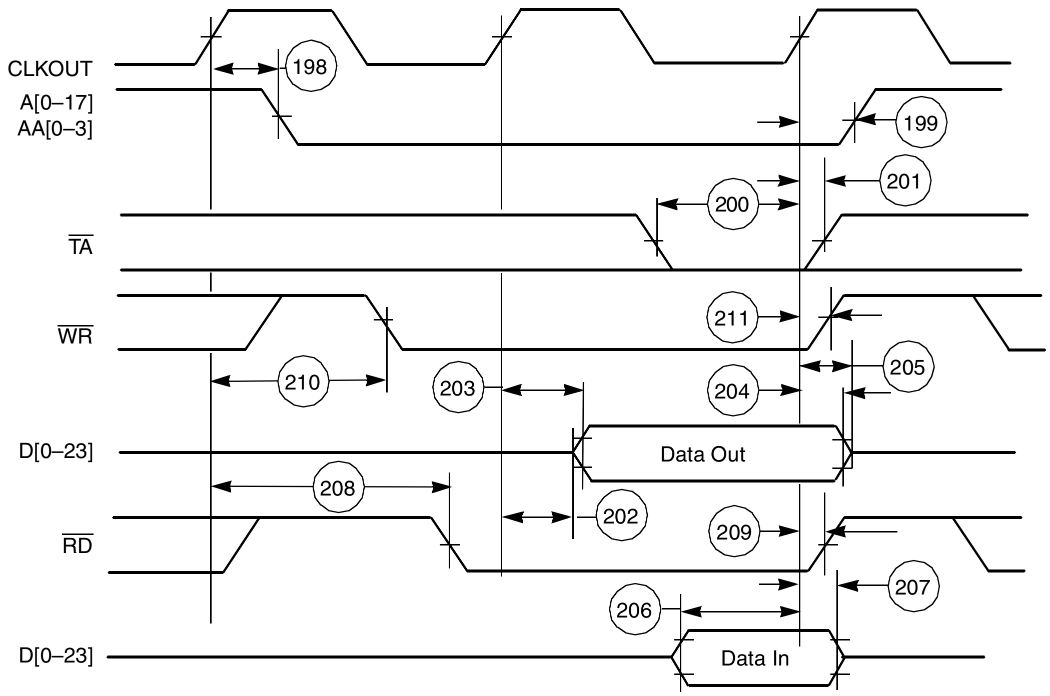
Table 2-8. SRAM Read and Write Accesses

No.	Characteristics	Symbol	Expression[1]	100 MHz Min	100 MHz Max	Unit
100	Address valid and AA assertion pulse width[2]	t_{RC}, t_{WC}	(WS + 1) × T_C −4.0 [1 ≤WS ≤3] (WS + 2) × T_C −4.0 [4 ≤WS ≤7] (WS + 3) × T_C −4.0 [WS ≥ 8]	16.0 56.0 106.0	— — —	ns ns ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	0.25 × T_C −2.0 [WS = 1] 0.75 × T_C −2.0 [2 ≤WS ≤3] 1.25 × T_C −2.0 [WS ≥ 4]	0.5 5.5 10.5	— — —	ns ns ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	1.5 × T_C −4.0 [WS = 1] WS × T_C −4.0 [2 ≤WS ≤3] (WS −0.5) × T_C −4.0 [WS ≥ 4]	11.0 16.0 31.0	— — —	ns ns ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	0.25 × T_C −2.0 [1 ≤WS ≤3] 1.25 × T_C −4.0 [4 ≤WS ≤7] 2.25 × T_C −4.0 [WS ≥ 8]	0.5 8.5 18.5	— — —	ns ns ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	(WS + 0.75) × T_C −5.0 [WS ≥ 1]	—	12.5	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	(WS + 0.25) × T_C − 5.0 [WS ≥ 1]	—	7.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	(WS + 0.75) × T_C −4.0 [WS ≥ 1]	13.5	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	(WS −0.25) × T_C −3.0 [WS ≥ 1]	4.5	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	0.25 × T_C −2.0 [1 ≤WS ≤3] 1.25 × T_C −2.0 [4 ≤WS ≤7] 2.25 × T_C −2.0 [WS ≥ 8]	0.5 10.5 20.5	— — —	ns ns ns
110	$\overline{WR}$ assertion to data active	—	0.75 × T_C −3.7 [WS = 1] 0.25 × T_C − 3.7 [2 ≤WS ≤3] −0.25 × T_C −3.7 [WS ≥ 4]	3.8 −1.2 −6.2	— — —	ns ns ns

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2] (Continued)

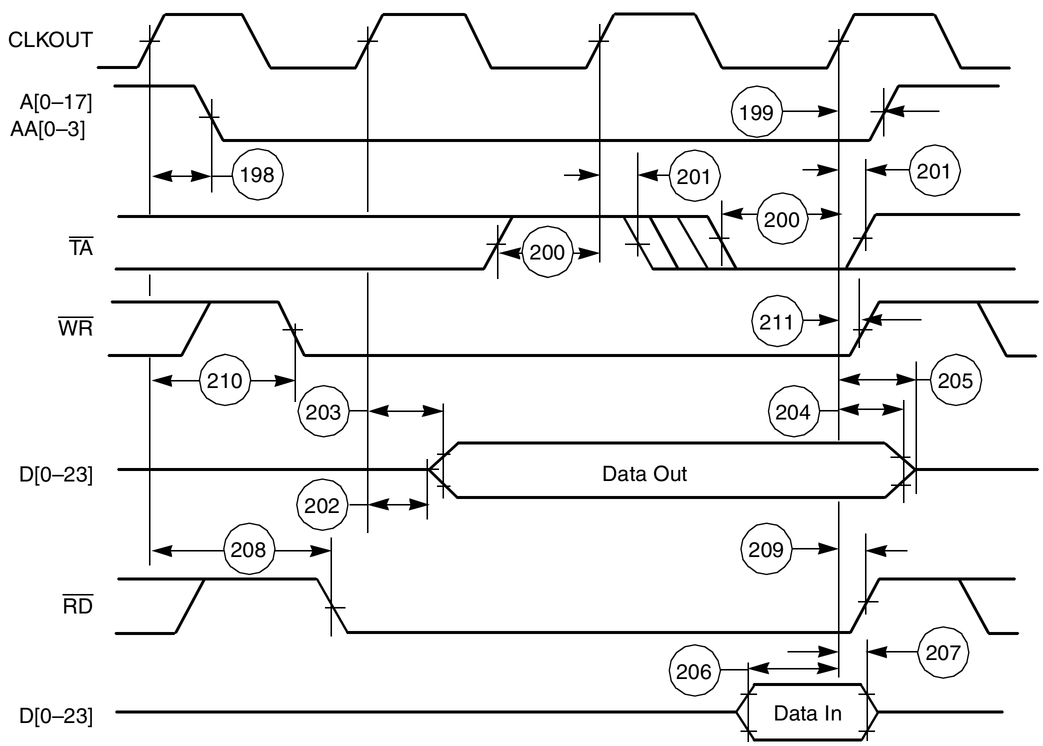
No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	13.5	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	48.5	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	73.5	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	56.0	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$3.0 \times T_C - 4.0$	26.0	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	13.8	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$[4] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	ns
180	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	45.8	—	ns
181	$\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	70.8	—	ns
182	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	110.5	—	ns
183	$\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	113.2	—	ns
184	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	98.2	—	ns
185	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	53.5	—	ns
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	48.5	—	ns
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	73.5	—	ns
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	60.7	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	23.5	—	ns
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$	—	93.0	ns
193	$\overline{\text{RD}}$ deassertion to data not valid[5]	t_{GZ}		0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. Use the expression to compute the maximum or minimum value listed (or both if the expression includes ±).
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.
5. $\overline{\text{RD}}$ deassertion always occurs after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-21. Synchronous Bus Timings 1 WS (BCR Controlled)



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-22. Synchronous Bus Timings 2 WS ($\overline{\text{TA}}$ Controlled)

2.5.6 Host Interface Timing

Table 2-16. Host Interface Timings[1,2,12]

No.	Characteristic[10]	Expression	100 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[5] $\overline{\text{HACK}}$ assertion width	$T_C + 9.9$	19.9	—	ns
318	Read data strobe deassertion width[5] $\overline{\text{HACK}}$ deassertion width		9.9	—	ns
319	Read data strobe deassertion width[5] after "Last Data Register" reads[8,11], or between two consecutive CVR, ICR, or ISR reads[3] $\overline{\text{HACK}}$ deassertion width after "Last Data Register" reads[8,11]	$2.5 \times T_C + 6.6$	31.6	—	ns
320	Write data strobe assertion width[6]		13.2	—	ns
321	Write data strobe deassertion width[8] $\overline{\text{HACK}}$ write deassertion width • after ICR, CVR and "Last Data Register" writes • after IVR writes, or after TXH:TXM:TXL writes (with HLEND= 0), or after TXL:TXM:TXH writes (with HLEND = 1)	$2.5 \times T_C + 6.6$	31.8 16.5	— —	ns ns
322	$\overline{\text{HAS}}$ assertion width		9.9	—	ns
323	$\overline{\text{HAS}}$ deassertion to data strobe assertion[4]		0.0	—	ns
324	Host data input setup time before write data strobe deassertion[6]		9.9	—	ns
325	Host data input hold time after write data strobe deassertion[6]		3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[5] $\overline{\text{HACK}}$ assertion to output data active from high impedance		3.3	—	ns
327	Read data strobe assertion to output data valid[5] $\overline{\text{HACK}}$ assertion to output data valid		—	24.5	ns
328	Read data strobe deassertion to output data high impedance[5] $\overline{\text{HACK}}$ deassertion to output data high impedance		—	9.9	ns
329	Output data hold time after read data strobe deassertion[5] Output data hold time after $\overline{\text{HACK}}$ deassertion		3.3	—	ns
330	$\overline{\text{HCS}}$ assertion to read data strobe deassertion[5]	$T_C + 9.9$	19.9	—	ns
331	$\overline{\text{HCS}}$ assertion to write data strobe deassertion[6]		9.9	—	ns
332	$\overline{\text{HCS}}$ assertion to output data valid		—	19.3	ns
333	$\overline{\text{HCS}}$ hold time after data strobe deassertion[4]		0.0	—	ns
334	Address (HAD[0–7]) setup time before $\overline{\text{HAS}}$ deassertion (HMUX=1)		4.6	—	ns
335	Address (HAD[0–7]) hold time after $\overline{\text{HAS}}$ deassertion (HMUX=1)		3.3	—	ns
336	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/$\overline{\text{W}}$ setup time before data strobe assertion[4] • Read • Write		0 4.6	— —	ns ns
337	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/$\overline{\text{W}}$ hold time after data strobe deassertion[4]		3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for "Last Data Register" read[5, 7, 8]	$T_C + 5.3$	15.3	—	ns
339	Delay from write data strobe deassertion to host request assertion for "Last Data Register" write[6, 7, 8]	$1.5 \times T_C + 5.3$	20.3	—	ns

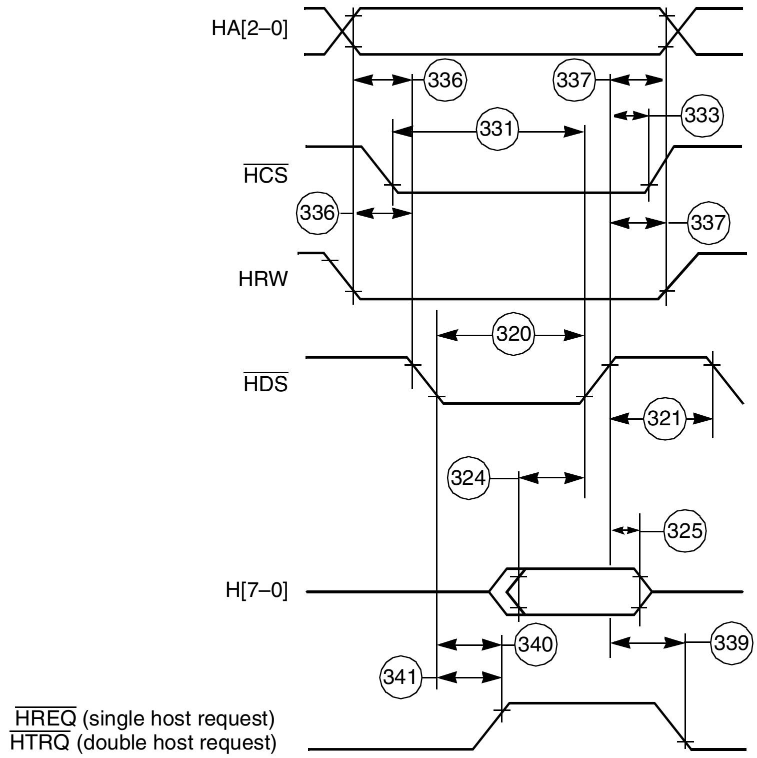


Figure 2-30. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

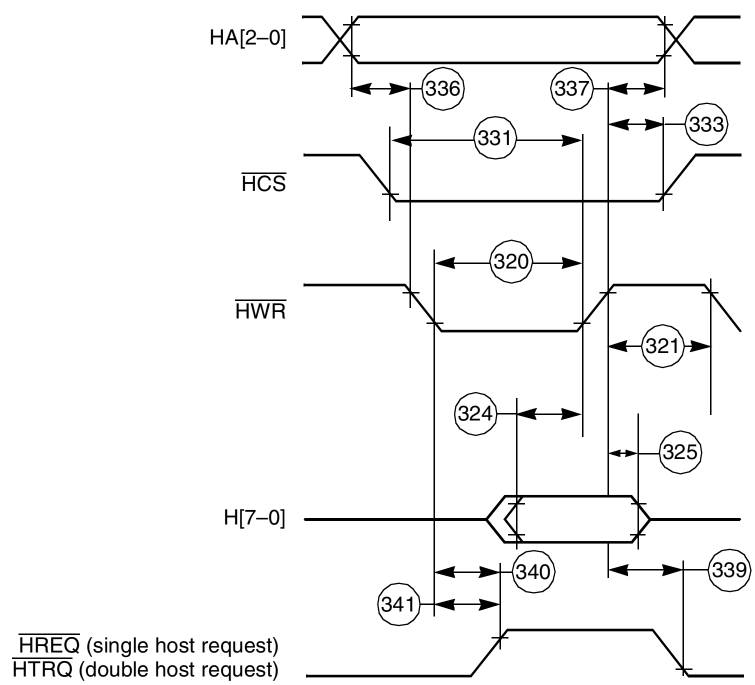


Figure 2-31. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

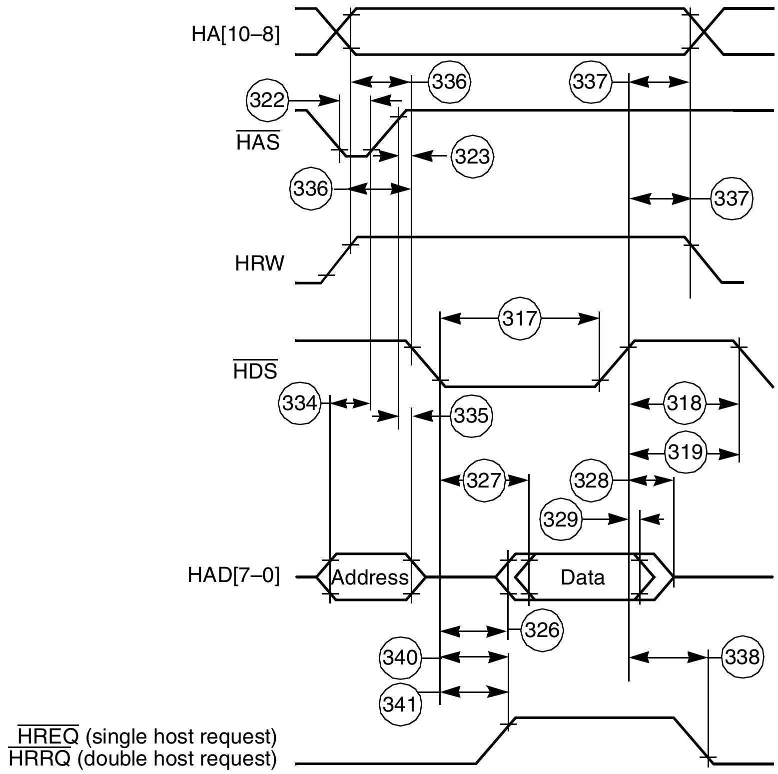


Figure 2-32. Read Timing Diagram, Multiplexed Bus, Single Data Strobe

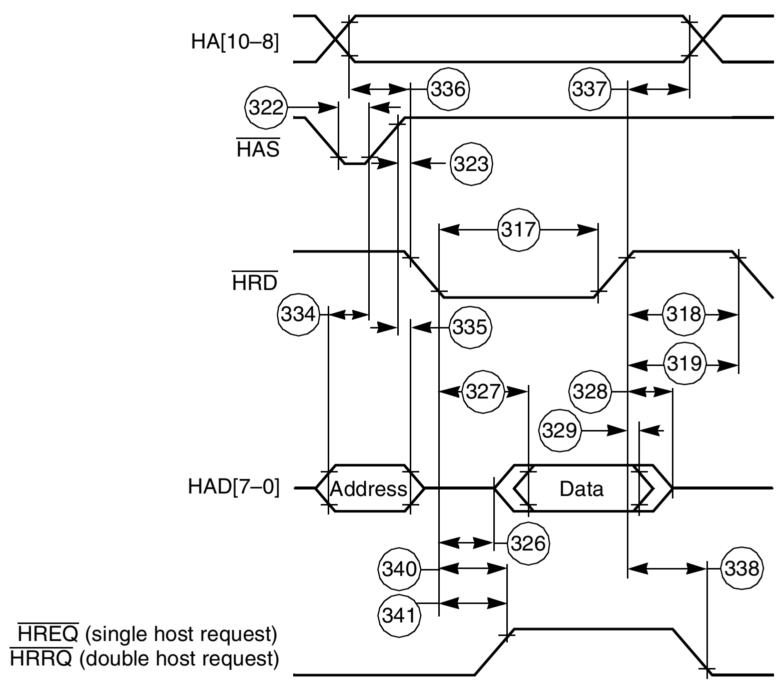


Figure 2-33. Read Timing Diagram, Multiplexed Bus, Double Data Strobe

2.5.10 GPIO Timing

Table 2-20. GPIO Timing

No.	Characteristics	Expression	100 MHz Min	100 MHz Max	Unit
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: $6.75 \times T_C$	67.5	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$				

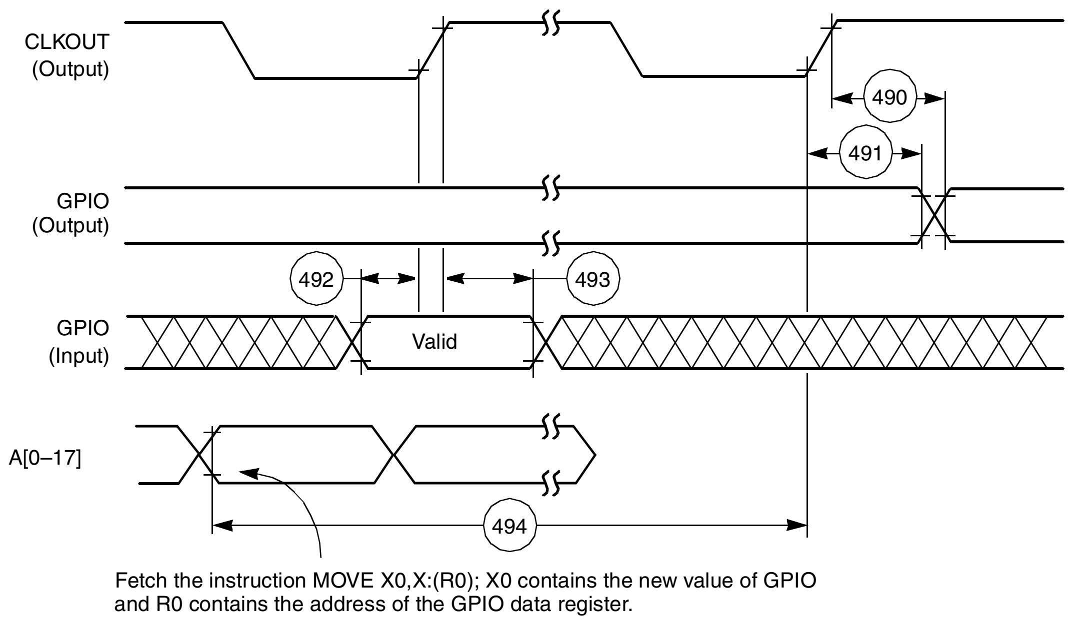


Figure 2-43. GPIO Timing

3.3 MAP-BGA Package Description

Top and bottom views of the MAP-BGA package are shown in **Figure 3-4** and **Figure 3-5** with their pin-outs.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	SC11	TMS	TDO	MODB	D23	V_{CCD}	D19	D16	D14	D11	D9	D7	NC
B	SRD1	SC12	TDI	$\overline{TRST}$	$\overline{MODD}$	D21	D20	D17	D15	D13	D10	D8	D5	NC
C	SC02	STD1	TCK	$\overline{MODA}$	$\overline{MODC}$	D22	V_{CCQ}	D18	V_{CCD}	D12	V_{CCD}	D6	D3	D4
D	PINIT	SC01	$\overline{DE}$	GND	GND	GND	GND	GND	GND	GND	GND	D1	D2	V_{CCD}
E	STD0	V_{CCS}	SRD0	GND	GND	GND	GND	GND	GND	GND	GND	A17	A16	D0
F	RXD	SC10	SC00	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A14	A15
G	SCK1	SCLK	TXD	GND	GND	GND	GND	GND	GND	GND	GND	A13	V_{CCQ}	A12
H	NC	V_{CCQ}	SCK0	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A10	A11
J	$\overline{HACK}$	HRW	$\overline{HDS}$	GND	GND	GND	GND	GND	GND	GND	GND	A8	A7	A9
K	V_{CCS}	$\overline{HREQ}$	TIO2	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A5	A6
L	$\overline{HCS}$	TIO1	TIO0	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A3	A4
M	HA1	HA2	HA0	V_{CCH}	PB0	V_{CCP}	NC	EXTAL	CLK OUT	$\overline{BCLK}$	$\overline{WR}$	$\overline{RD}$	A1	A2
N	H6	H7	H4	H2	$\overline{RESET}$	GND_P	AA3	$\overline{CAS}$	V_{CCQ}	BCLK	$\overline{BR}$	V_{CCC}	AA0	A0
P	NC	H5	H3	H1	PCAP	GND_{P1}	AA2	XTAL	V_{CCC}	$\overline{TA}$	$\overline{BB}$	AA1	$\overline{BG}$	NC

Figure 3-4. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Bottom View

	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	D7	D9	D11	D14	D16	D19	V_{CCD}	D23	MODB	TDO	TMS	SC11	NC
B	NC	D5	D8	D10	D13	D15	D17	D20	D21	$\overline{\text{MODD}}$	$\overline{\text{TRST}}$	TDI	SC12	SRD1
C	D4	D3	D6	V_{CCD}	D12	V_{CCD}	D18	V_{CCQ}	D22	$\overline{\text{MODC}}$	$\overline{\text{MODA}}$	TCK	STD1	SC02
D	V_{CCD}	D2	D1	GND	GND	GND	GND	GND	GND	GND	GND	$\overline{\text{DE}}$	SC01	PINIT
E	D0	A16	A17	GND	GND	GND	GND	GND	GND	GND	GND	SRD0	V_{CCS}	STD0
F	A15	A14	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	SC00	SC10	RXD
G	A12	V_{CCQ}	A13	GND	GND	GND	GND	GND	GND	GND	GND	TXD	SCLK	SCK1
H	A11	A10	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	SCK0	V_{CCQ}	NC
J	A9	A7	A8	GND	GND	GND	GND	GND	GND	GND	GND	$\overline{\text{HDS}}$	HRW	$\overline{\text{HACK}}$
K	A6	A5	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	TIO2	$\overline{\text{HREQ}}$	V_{CCS}
L	A4	A3	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	TIO0	TIO1	$\overline{\text{HCS}}$
M	A2	A1	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{BCLK}}$	CLK OUT	EXTAL	NC	V_{CCP}	PB0	V_{CCH}	HA0	HA2	HA1
N	A0	AA0	V_{CCC}	$\overline{\text{BR}}$	BCLK	V_{CCQ}	$\overline{\text{CAS}}$	AA3	GND_P	$\overline{\text{RESET}}$	H2	H4	H7	H6
P	NC	$\overline{\text{BG}}$	AA1	$\overline{\text{BB}}$	$\overline{\text{TA}}$	V_{CCC}	XTAL	AA2	GND_{P1}	PCAP	H1	H3	H5	NC

Figure 3-5. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
TDO	A4	V_{CCA}	K12	V_{CCP}	M6
TIO0	L3	V_{CCA}	L12	V_{CCQ}	C7
TIO1	L2	V_{CCC}	N12	V_{CCQ}	G13
TIO2	K3	V_{CCC}	P9	V_{CCQ}	H2
TMS	A3	V_{CCD}	A7	V_{CCQ}	N9
$\overline{TRST}$	B4	V_{CCD}	C9	V_{CCS}	E2
TXD	G3	V_{CCD}	C11	V_{CCS}	K1
V_{CCA}	F12	V_{CCD}	D14	$\overline{WR}$	M11
V_{CCA}	H12	V_{CCH}	M4	XTAL	P8

3.4 MAP-BGA Package Mechanical Drawing

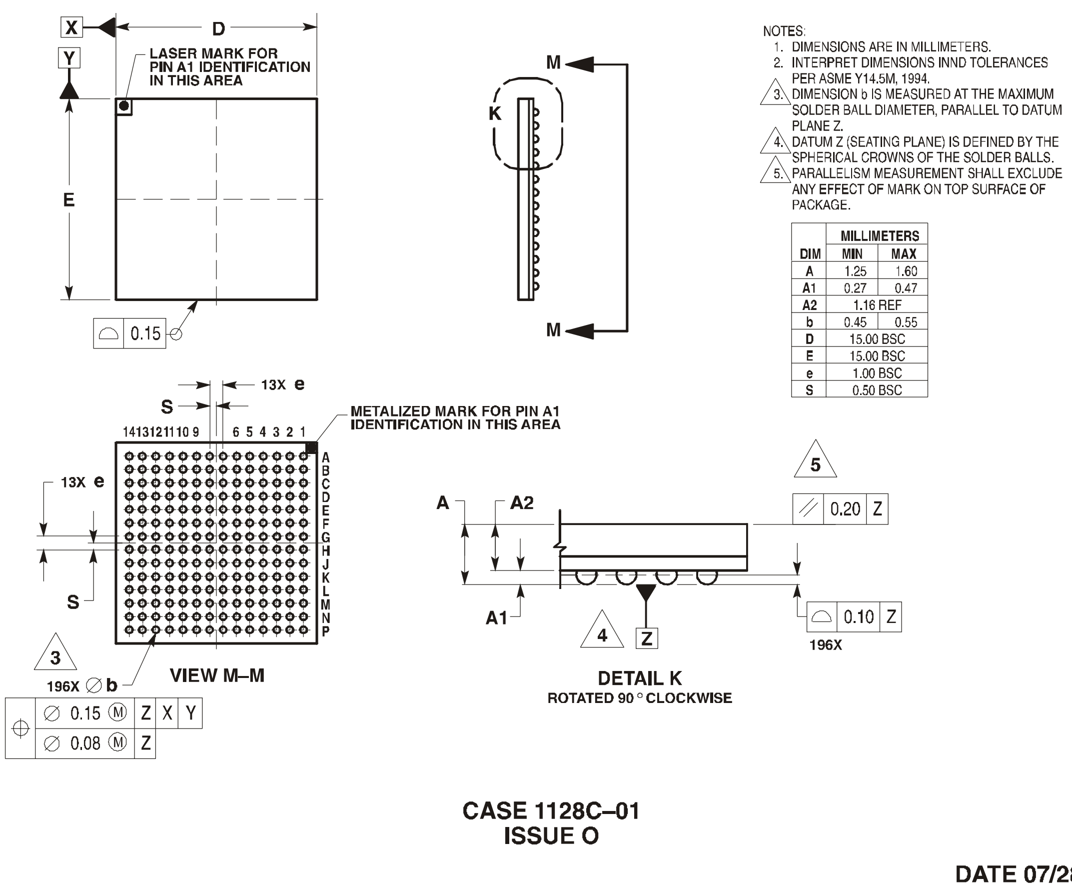


Figure 3-6. DSP56303 Mechanical Information, 196-pin MAP-BGA Package

- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{TRST}$, TMS, $\overline{DE}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{RESET}$ and $\overline{TRST}$.
- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{RESET}$ must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of $\overline{RESET}$.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $I = C \times V \times f$

Where:

C	=	node/pin capacitance
V	=	voltage swing
f	=	frequency of node/pin toggle

Example 4-1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.

Power Consumption Benchmark A

The following benchmark program evaluates DSP56303 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;**************************************************************************
;**************************************************************************
;*                                                                        *
;*                   CHECKS   Typical Power Consumption                   *
;*                                                                        *
;**************************************************************************

       page    200,55,0,0,0
       nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0; INTERNAL X-data memory starting address
INT_YDAT  EQU $0; INTERNAL Y-data memory starting address

       INCLUDE "ioequ.asm"
       INCLUDE "intequ.asm"

       list

       org     P:START
;
       movep #$0243FF,x:M_BCR ;; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
       movep   #$0d0000,x:M_PCTL     ; XTAL disable
                                     ; PLL enable
                                     ; CLKOUT disable
;
; Load the program
;
       move    #INT_PROG,r0
       move    #PROG_START,r1
       do      #(PROG_END-PROG_START),PLOAD_LOOP
       move    p:(r1)+,x0
       move    x0,p:(r0)+
       nop
PLOAD_LOOP
;
; Load the X-data
;
       move    #INT_XDAT,r0
       move    #XDAT_START,r1
       do      #(XDAT_END-XDAT_START),XLOAD_LOOP
```

```
M_BRP EQU 23                    ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3                    ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2                    ; Address Attribute Pin Polarity
M_BPEN EQU 3                    ; Program Space Enable
M_BXEN EQU 4                    ; X Data Space Enable
M_BYEN EQU 5                    ; Y Data Space Enable
M_BAM EQU 6                     ; Address Muxing
M_BPAC EQU 7                    ; Packing Enable
M_BNC EQU $F00                  ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000               ; Address to Compare Bits Mask (BAC0-BAC11)


;       control and status bits in SR

M_CP EQU $c00000                ; mask for CORE-DMA priority bits in SR
M_CA EQU 0                      ; Carry
M_V EQU 1                       ; Overflow
M_Z EQU 2                       ; Zero
M_N EQU 3                       ; Negative
M_U EQU 4                       ; Unnormalized
M_E EQU 5                       ; Extension
M_L EQU 6                       ; Limit
M_S EQU 7                       ; Scaling Bit
M_I0 EQU 8                      ; Interupt Mask Bit 0
M_I1 EQU 9                      ; Interupt Mask Bit 1
M_S0 EQU 10                     ; Scaling Mode Bit 0
M_S1 EQU 11                     ; Scaling Mode Bit 1
M_SC EQU 13                     ; Sixteen_Bit Compatibility
M_DM EQU 14                     ; Double Precision Multiply
M_LF EQU 15                     ; DO-Loop Flag
M_FV EQU 16                     ; DO-Forever Flag
M_SA EQU 17                     ; Sixteen-Bit Arithmetic
M_CE EQU 19                     ; Instruction Cache Enable
M_SM EQU 20                     ; Arithmetic Saturation
M_RM EQU 21                     ; Rounding Mode
M_CP0 EQU 22                    ; bit 0 of priority bits in SR
M_CP1 EQU 23                    ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU $300                  ; mask for CORE-DMA priority bits in OMR
M_MA    equ0                    ; Operating Mode A
M_MB   equ1                     ; Operating Mode B
M_MC    equ2                    ; Operating Mode C
M_MD    equ3                    ; Operating Mode D
M_EBD EQU 4                     ; External Bus Disable bit in OMR
M_SD EQU 6                      ; Stop Delay
M_MS EQU 7                      ; Memory Switch bit in OMR
M_CDP0 EQU 8                    ; bit 0 of priority bits in OMR
M_CDP1 EQU 9                    ; bit 1 of priority bits in OMR
M_BEN   EQU 10                  ; Burst Enable
M_TAS   EQU 11                  ; TA Synchronize Select
M_BRT   EQU 12                  ; Bus Release Timing
M_ATE EQU 15                    ; Address Tracing Enable bit in OMR.
M_XYS EQU 16                    ; Stack Extension space select bit in OMR.
M_EUN EQU 17                    ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18                    ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19                    ; Extended WRaP flag in OMR.
```