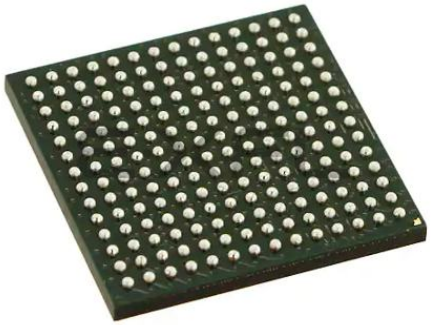

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56303vf100r2

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

1.4 PLL

Table 1-5. Phase-Locked Loop Signals

Signal Name	Type	State During Reset	Signal Description
CLKOUT	Output	Chip-driven	**Clock Output—**Provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PCAP	Input	Input	**PLL Capacitor**—An input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP can be tied to V_{CC}, GND, or left floating.
PINIT $\overline{\text{NMI}}$	Input Input	Input	**PLL Initial**—During assertion of $\overline{\text{RESET}}$, the value of PINIT is written into the PLL enable (PEN) bit of the PLL control (PCTL) register, determining whether the PLL is enabled or disabled. **Nonmaskable Interrupt**—After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, this Schmitt-trigger input is the negative-edge-triggered NMI request internally synchronized to CLKOUT. **Note**: PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.

1.5 External Memory Expansion Port (Port A)

Note: When the DSP56303 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–17], D[0–23], AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$.

1.5.1 External Address Bus

Table 1-6. External Address Bus Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
A[0–17]	Output	Tri-stated	**Address Bus**—When the DSP is the bus master, A[0–17] are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–17] do not change state when external memory spaces are not being accessed.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
$\overline{\text{HDS}}$/HDS	Input	Ignored Input	**Host Data Strobe**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input or Output		**Port B 12**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HREQ}}$/HREQ	Output	Ignored Input	**Host Request**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host request (HREQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input or Output		**Port B 14**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HACK}}$/HACK	Input	Ignored Input	**Host Acknowledge**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input or Output		**Port B 15**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

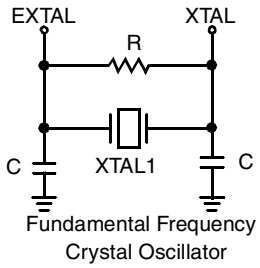
Table 2-4. Internal Clocks, CLKOUT (Continued)

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: 1. DF = Division Factor; Ef = External frequency; ET_C = External clock cycle; MF = Multiplication Factor; PDF = Predivision Factor; T_C = internal clock cycle
2. See the PLL and Clock Generation section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

2.5.2 External Clock Operation

The DSP56303 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; examples are shown in **Figure 2-1**.



Note: Make sure that in the PCTL Register:
- XTLD (bit 16) = 0
- If f_{OSC} > 200 kHz, XTLR (bit 15) = 0

Suggested Component Values:

f_{OSC} = 4 MHz
R = 680 kΩ±10%
C = 56 pF ±20%

f_{OSC} = 20 MHz
R = 680 kΩ±10%
C = 22 pF ±20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
- C_L of 30/20 pF,
- C_0 of 7/6 pF,
- series resistance of 100/20 Ω, and
- drive level of 2 mW.

Figure 2-1. Crystal Oscillator Circuits

If an externally-supplied square wave voltage source is used, disable the internal oscillator circuit during bootup by setting XTLD (PCTL Register bit 16 = 1—see the *DSP56303 User's Manual*). The external square wave source connects to EXTAL; XTAL is not physically connected to the board or socket. **Figure 2-2** shows the relationship between the EXTAL input and the internal clock and CLKOUT.

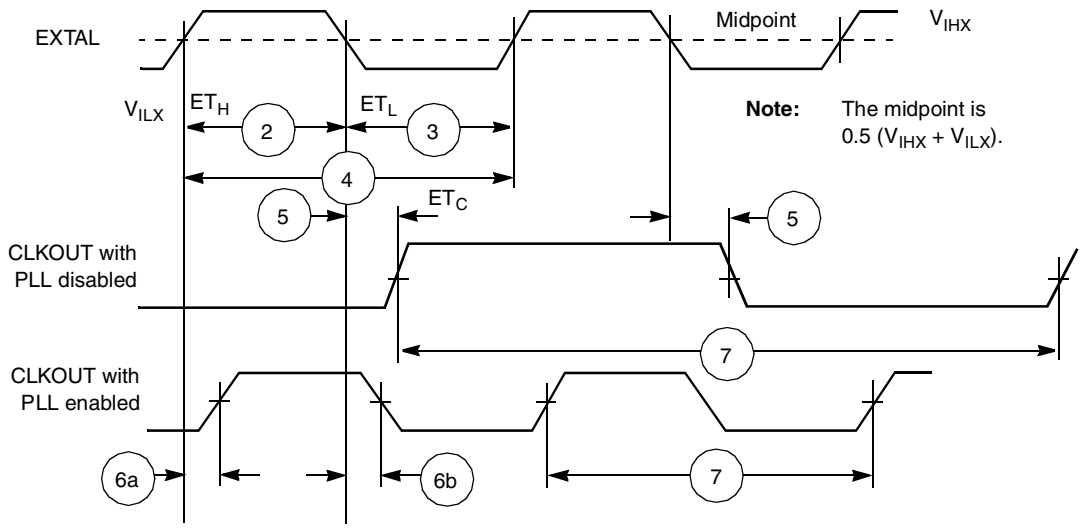


Figure 2-2. External Clock Timing

Table 2-5. Clock Operation

No.	Characteristics	Symbol	100 MHz	
			Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 4.67 ns 4.25 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 4.67 ns 4.25 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 10.00 ns 10.00 ns	 ∞ 273.1 µs
5	Internal clock change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns
6	a.Internal clock rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. Internal clock falling edge from EXTAL falling edge with PLL enabled (MF ≤4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$[4] (see **Table 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 20.0 ns 10.00 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition.
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-4**) and maximum MF.
3. Periodically sampled and not 100 percent tested.
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.5.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	100 MHz		Unit
	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1]) • @ MF ≤4 • @ MF > 4	 (580 × MF) –100 830 × MF	 (780 × MF) –140 1470 × MF	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}) computed using the appropriate expression listed above.

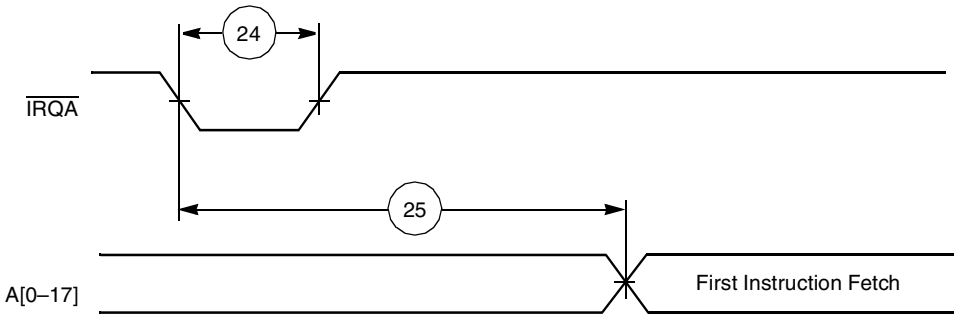


Figure 2-9. Recovery from Stop State Using $\overline{\text{IRQA}}$

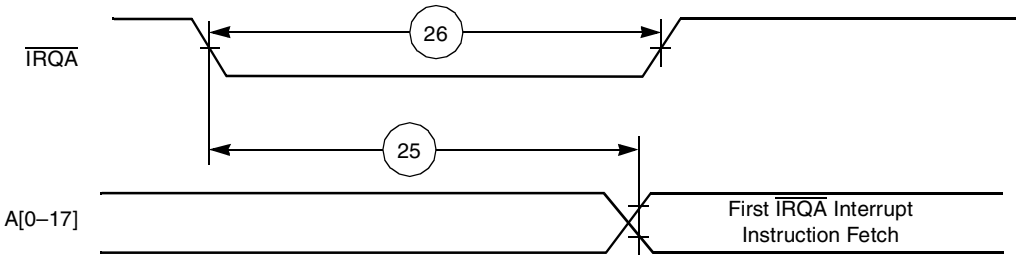


Figure 2-10. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

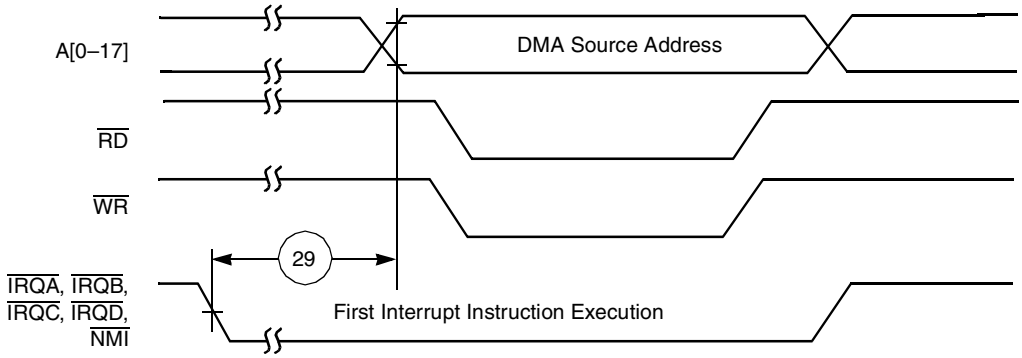


Figure 2-11. External Memory Access (DMA Source) Timing

2.5.5 External Memory Expansion Port (Port A)

2.5.5.1 SRAM Timing

Table 2-8. SRAM Read and Write Accesses

No.	Characteristics	Symbol	Expression[1]	100 MHz		Unit
				Min	Max	
100	Address valid and AA assertion pulse width[2]	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ [1 ≤WS ≤3]	16.0	—	ns
			$(WS + 2) \times T_C - 4.0$ [4 ≤WS ≤7]	56.0	—	ns
			$(WS + 3) \times T_C - 4.0$ [WS ≥ 8]	106.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	$0.25 \times T_C - 2.0$ [WS = 1]	0.5	—	ns
			$0.75 \times T_C - 2.0$ [2 ≤WS ≤3]	5.5	—	ns
			$1.25 \times T_C - 2.0$ [WS ≥ 4]	10.5	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.0$ [WS = 1]	11.0	—	ns
			$WS \times T_C - 4.0$ [2 ≤WS ≤3]	16.0	—	ns
			$(WS - 0.5) \times T_C - 4.0$ [WS ≥ 4]	31.0	—	ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	$0.25 \times T_C - 2.0$ [1 ≤WS ≤3]	0.5	—	ns
			$1.25 \times T_C - 4.0$ [4 ≤WS ≤7]	8.5	—	ns
			$2.25 \times T_C - 4.0$ [WS ≥ 8]	18.5	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	$(WS + 0.75) \times T_C - 5.0$ [WS ≥ 1]	—	12.5	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	$(WS + 0.25) \times T_C - 5.0$ [WS ≥ 1]	—	7.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ [WS ≥ 1]	13.5	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	$(WS - 0.25) \times T_C - 3.0$ [WS ≥ 1]	4.5	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	$0.25 \times T_C - 2.0$ [1 ≤WS ≤3]	0.5	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤WS ≤7]	10.5	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	20.5	—	ns
110	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 3.7$ [WS = 1]	3.8	—	ns
			$0.25 \times T_C - 3.7$ [2 ≤WS ≤3]	–1.2	—	ns
			$-0.25 \times T_C - 3.7$ [WS ≥ 4]	–6.2	—	ns

2.5.5.4 Arbitration Timings

Table 2-14. Arbitration Bus Timings[1]

No.	Characteristics	Expression[2]	100 MHz		Unit
			Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion/deassertion[3]		0.0	4.0	ns
213	$\overline{BG}$ asserted/deasserted to CLKOUT high (setup)		4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted/asserted (hold)		0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input set-up)		4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)		0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)		0.0	4.0	ns
218	CLKOUT high to $\overline{BB}$ deassertion (output)		0.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)		—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	2.5	—	ns
221	CLKOUT high to address and controls high impedance	$0.75 \times T_C$	—	7.5	ns
222	CLKOUT high to AA active	$0.25 \times T_C$	2.5	—	ns
223	CLKOUT high to AA deassertion	maximum: $0.25 \times T_C + 4.0$	2.0	6.5	ns
224	CLKOUT high to AA high impedance	$0.75 \times T_C$	—	7.5	ns

Notes:
1. Synchronous bus arbitration is not recommended. Use Asynchronous mode whenever possible.
2. An expression is used to compute the maximum or minimum value listed, as appropriate. For timing 223, the minimum is an absolute value.
3. T212 is valid for Address Trace mode when the ATE bit in the Operating Mode Register is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.

2.5.5.5 Asynchronous Bus Arbitration Timings

Table 2-15. Asynchronous Bus Timings[1, 2]

No.	Characteristics	Expression[3]	100 MHz[4]		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion[5]	2.5 × Tc + 5	—	30	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion[5]	2 × Tc + 5	25	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
2. If Asynchronous Arbitration mode is active, none of the timings in **Table 2-14** is required.
3. An expression is used to compute the maximum or minimum value listed, as appropriate.
4. Asynchronous Arbitration mode is recommended for operation at 100 MHz.
5. In order to guarantee timings 250, and 251, BG inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in **Figure 2-26**.

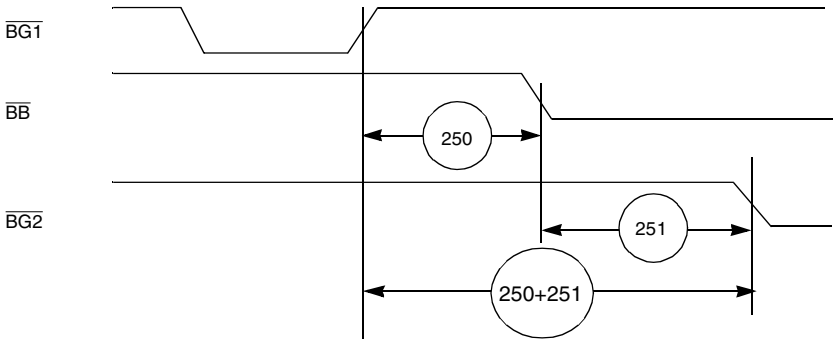


Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

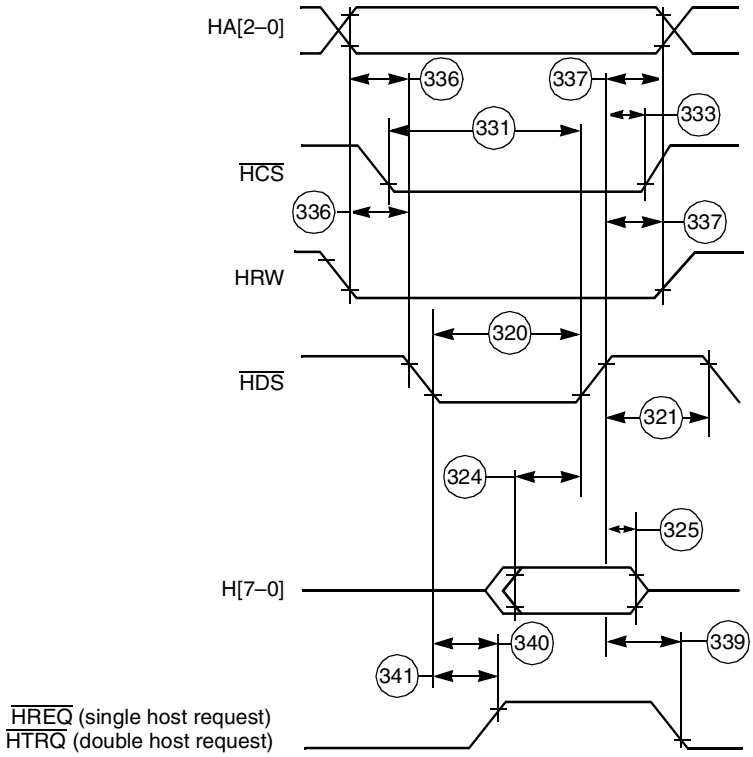


Figure 2-30. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

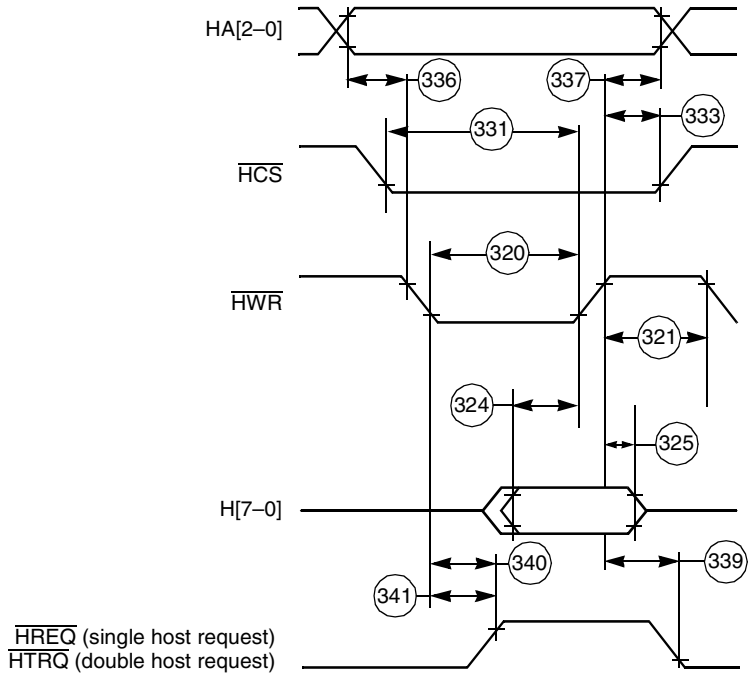


Figure 2-31. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

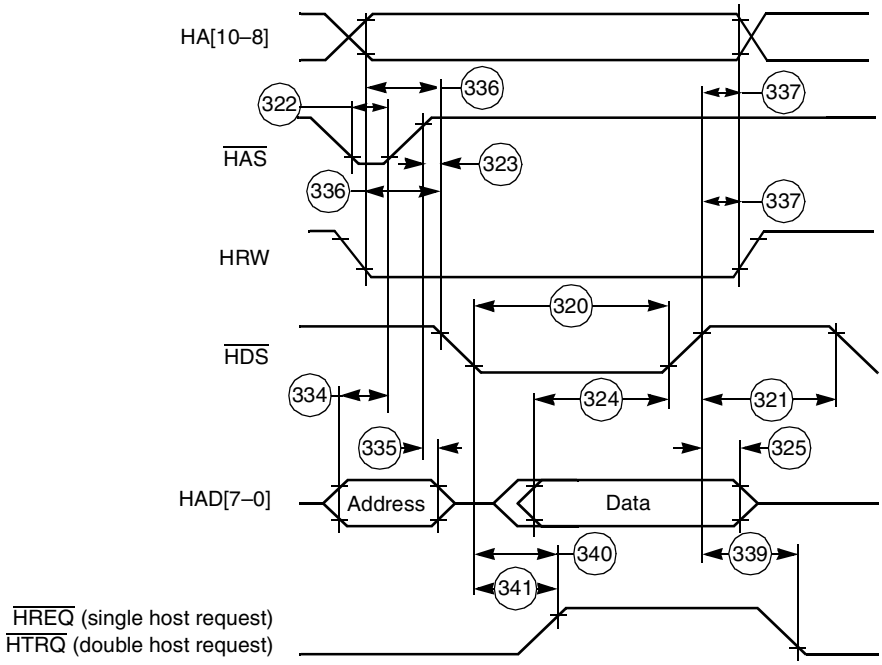


Figure 2-34. Write Timing Diagram, Multiplexed Bus, Single Data Strobe

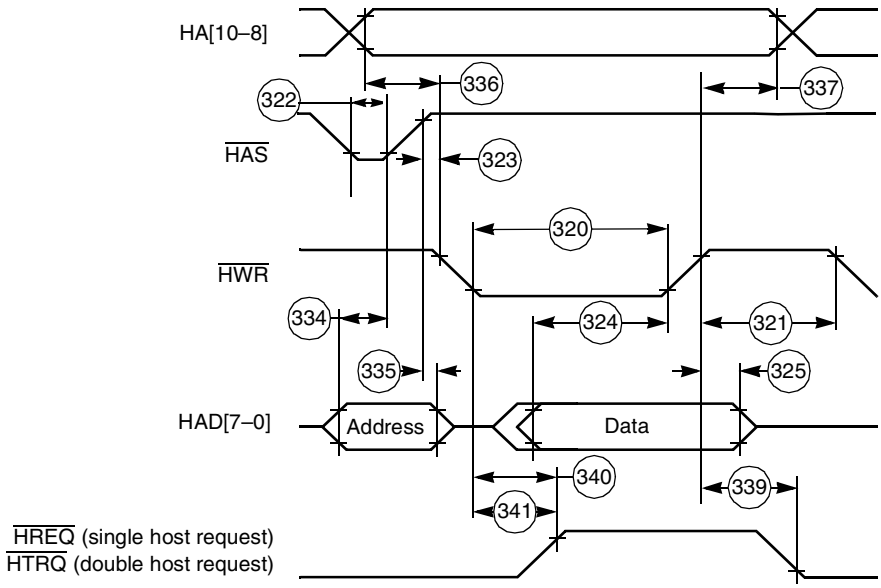
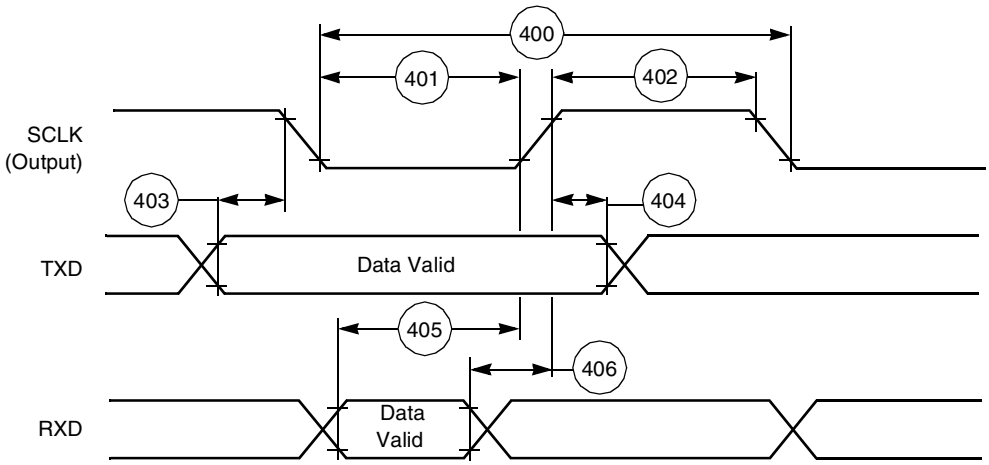
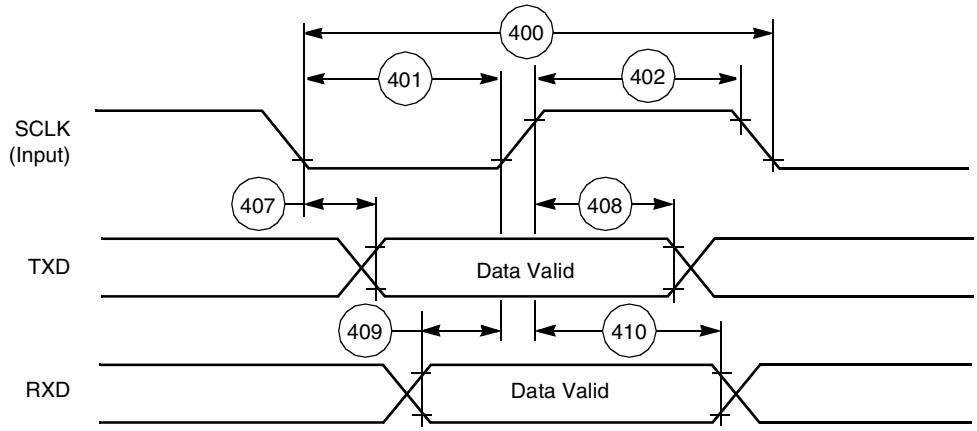


Figure 2-35. Write Timing Diagram, Multiplexed Bus, Double Data Strobe



a) Internal Clock



b) External Clock

Figure 2-36. SCI Synchronous Mode Timing

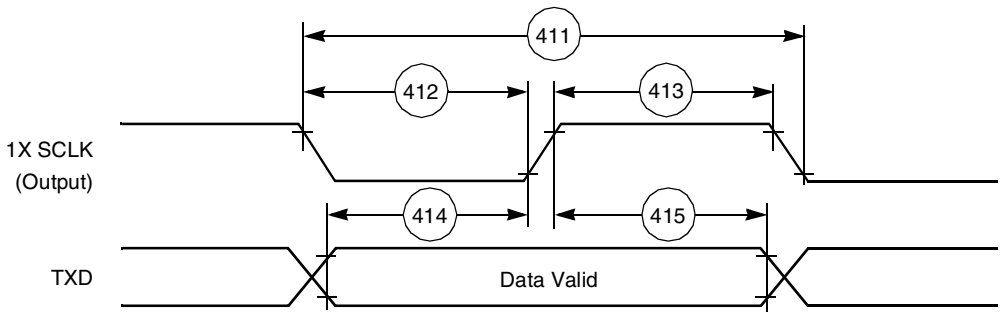


Figure 2-37. SCI Asynchronous Mode Timing

2.5.8 ESSI0/ESSI1 Timing

Table 2-18. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	30.0 40.0	— —	x ck i ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C$ - 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C$ –10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in set-up time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr)[7] high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl)[7] high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input set-up before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (word-length) low			— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	x ck i ck	ns

Table 3-1. DSP56303 TQFP Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	A2	99	A17	122	D16
77	A3	100	D0	123	D17
78	A4	101	D1	124	D18
79	A5	102	D2	125	D19
80	V_{CCA}	103	V_{CCD}	126	V_{CCQ}
81	GND_A	104	GND_D	127	GND_Q
82	A6	105	D3	128	D20
83	A7	106	D4	129	V_{CCD}
84	A8	107	D5	130	GND_D
85	A9	108	D6	131	D21
86	V_{CCA}	109	D7	132	D22
87	GND_A	110	D8	133	D23
88	A10	111	V_{CCD}	134	MODD/$\overline{\text{IRQD}}$
89	A11	112	GND_D	135	MODC/$\overline{\text{IRQC}}$
90	GND_Q	113	D9	136	MODB/$\overline{\text{IRQB}}$
91	V_{CCQ}	114	D10	137	MODA/$\overline{\text{IRQA}}$
92	A12	115	D11	138	$\overline{\text{TRST}}$
93	A13	116	D12	139	TDO
94	A14	117	D13	140	TDI
95	V_{CCA}	118	D14	141	TCK
96	GND_A	119	V_{CCD}	142	TMS
97	A15	120	GND_D	143	SC12 or PD2
98	A16	121	D15	144	SC11 or PD1

Notes: Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/$\overline{\text{IRQx}}$ pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{\text{HAS}}$/HAS. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, Pin 34 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin.

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
F6	GND	H3	SCK0 or PC3	J14	A9
F7	GND	H4	GND	K1	V_{CCS}
F8	GND	H5	GND	K2	$\overline{\text{HREQ}}$/HREQ, $\overline{\text{HTRQ}}$/HTRQ, or PB14
F9	GND	H6	GND	K3	TIO2
F10	GND	H7	GND	K4	GND
F11	GND	H8	GND	K5	GND
F12	V_{CCA}	H9	GND	K6	GND
F13	A14	H10	GND	K7	GND
F14	A15	H11	GND	K8	GND
G1	SCK1 or PD3	H12	V_{CCA}	K9	GND
G2	SCLK or PE2	H13	A10	K10	GND
G3	TXD or PE1	H14	A11	K11	GND
G4	GND	J1	$\overline{\text{HACK}}$/HACK, $\overline{\text{HRRQ}}$/HRRQ, or PB15	K12	V_{CCA}
G5	GND	J2	HRW, $\overline{\text{HRD}}$/HRD, or PB11	K13	A5
G6	GND	J3	$\overline{\text{HDS}}$/HDS, $\overline{\text{HWR}}$/HWR, or PB12	K14	A6
G7	GND	J4	GND	L1	$\overline{\text{HCS}}$/HCS, HA10, or PB13
G8	GND	J5	GND	L2	TIO1
G9	GND	J6	GND	L3	TIO0
G10	GND	J7	GND	L4	GND
G11	GND	J8	GND	L5	GND
G12	A13	J9	GND	L6	GND
G13	V_{CCQ}	J10	GND	L7	GND
G14	A12	J11	GND	L8	GND
H1	NC	J12	A8	L9	GND
H2	V_{CCQ}	J13	A7	L10	GND
L11	GND	M13	A1	P1	NC
L12	V_{CCA}	M14	A2	P2	H5, HAD5, or PB5
L13	A3	N1	H6, HAD6, or PB6	P3	H3, HAD3, or PB3
L14	A4	N2	H7, HAD7, or PB7	P4	H1, HAD1, or PB1

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
M1	HA1, HA8, or PB9	N3	H4, HAD4, or PB4	P5	PCAP
M2	HA2, HA9, or PB10	N4	H2, HAD2, or PB2	P6	GND_{P1}
M3	HA0, $\overline{HAS}$/HAS, or PB8	N5	$\overline{RESET}$	P7	AA2/$\overline{RAS2}$
M4	V_{CCH}	N6	GND_P	P8	XTAL
M5	H0, HAD0, or PB0	N7	AA3/$\overline{RAS3}$	P9	V_{CCC}
M6	V_{CCP}	N8	$\overline{CAS}$	P10	$\overline{TA}$
M7	NC	N9	V_{CCQ}	P11	$\overline{BB}$
M8	EXTAL	N10	BCLK	P12	AA1/$\overline{RAS1}$
M9	CLKOUT	N11	$\overline{BR}$	P13	$\overline{BG}$
M10	$\overline{BCLK}$	N12	V_{CCC}	P14	NC
M11	$\overline{WR}$	N13	AA0/$\overline{RAS0}$		
M12	$\overline{RD}$	N14	A0		

Notes: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike in the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
TDO	A4	V_{CCA}	K12	V_{CCP}	M6
TIO0	L3	V_{CCA}	L12	V_{CCQ}	C7
TIO1	L2	V_{CCC}	N12	V_{CCQ}	G13
TIO2	K3	V_{CCC}	P9	V_{CCQ}	H2
TMS	A3	V_{CCD}	A7	V_{CCQ}	N9
$\overline{TRST}$	B4	V_{CCD}	C9	V_{CCS}	E2
TXD	G3	V_{CCD}	C11	V_{CCS}	K1
V_{CCA}	F12	V_{CCD}	D14	$\overline{WR}$	M11
V_{CCA}	H12	V_{CCH}	M4	XTAL	P8

3.4 MAP-BGA Package Mechanical Drawing

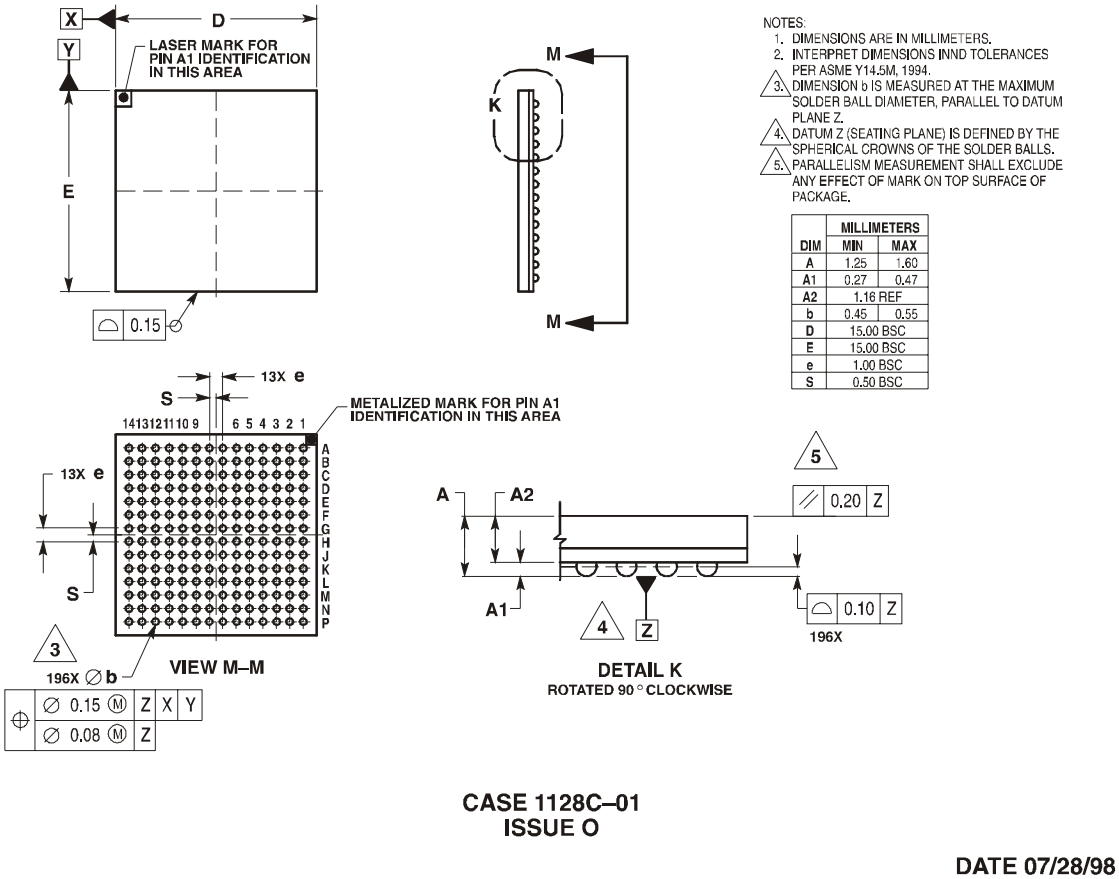


Figure 3-6. DSP56303 Mechanical Information, 196-pin MAP-BGA Package

- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.
- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{\text{RESET}}$ must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of $\overline{\text{RESET}}$.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $$I = C \times V \times f$$

Where:

C	=	node/pin capacitance
V	=	voltage swing
f	=	frequency of node/pin toggle

Example 4-1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $$I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

```
        dc      $6162BC
        dc      $E4A245
YDAT_END

;*************************************************************************
;
;     EQUATES for DSP56303 I/O registers and ports
;
;     Last update: June 11 1995
;
;*************************************************************************

        page    132,55,0,0,0
        opt     mex

ioequ   ident   1,0

;-------------------------------------------------------------------------
;
;       EQUATES for I/O Port Programming
;
;-------------------------------------------------------------------------

;       Register Addresses

M_HDR EQU $FFFFC9                   ; Host port GPIO data Register
M_HDDR EQU $FFFFC8                  ; Host port GPIO direction Register
M_PCRC EQU $FFFFBF                  ; Port C Control Register
M_PRRC EQU $FFFFBE                  ; Port C Direction Register
M_PDRC EQU $FFFFBD                  ; Port C GPIO Data Register
M_PCRD EQU $FFFFAF                  ; Port D Control register
M_PRRD EQU $FFFFAE                  ; Port D Direction Data Register
M_PDRD EQU $FFFFAD                  ; Port D GPIO Data Register
M_PCRE EQU $FFFF9F                  ; Port E Control register
M_PRRE EQU $FFFF9E                  ; Port E Direction Register
M_PDRE EQU $FFFF9D                  ; Port E Data Register
M_OGDB EQU $FFFFFC                  ; OnCE GDB Register


;-------------------------------------------------------------------------
;
;       EQUATES for Host Interface
;
;-------------------------------------------------------------------------

;       Register Addresses

M_HCR EQU $FFFFC2                   ; Host Control Register
M_HSR EQU $FFFFC3                   ; Host Status Register
M_HPCR EQU $FFFFC4                  ; Host Polarity Control Register
M_HBAR EQU $FFFFC5                  ; Host Base Address Register
M_HRX EQU $FFFFC6                   ; Host Receive Register
M_HTX EQU $FFFFC7                   ; Host Transmit Register

;       HCR bits definition
M_HRIE EQU $0                       ; Host Receive interrupts Enable
M_HTIE EQU $1                       ; Host Transmit Interrupt Enable
M_HCIE EQU $2                       ; Host Command Interrupt Enable
M_HF2 EQU $3                        ; Host Flag 2
M_HF3 EQU $4                        ; Host Flag 3
```