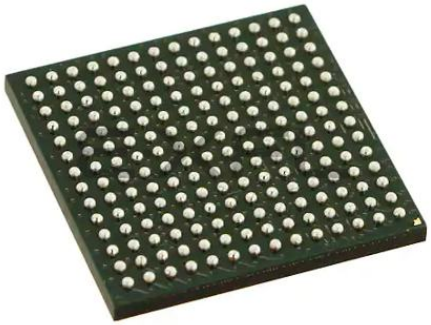

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56303vl100

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCQ}	**Quiet Power**—An isolated power for the core processing logic. This input must be isolated externally from all other chip power inputs.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQ}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQ}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs**,** *except* V_{CCQ}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs**,** *except* V_{CCQ}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQ}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds[1]

Ground Name	Description
GND_P	**PLL Ground**—Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package.
GND_{P1}	**PLL Ground 1**—Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_Q[2]	**Quiet Ground—**An isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_A[2]	**Address Bus Ground—**An isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_D[2]	**Data Bus Ground—**An isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_C[2]	**Bus Control Ground—**An isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_H[2]	**Host Ground—**An isolated ground for the HI08 I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_S[2]	**ESSI, SCI, and Timer Ground—**An isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND[3]	**Ground**—Connected to an internal device ground plane.

Notes:
1. The user must provide adequate external decoupling capacitors for all GND connections.
2. These connections are only used on the TQFP package.
3. These connections are common grounds used on the MAP-BGA package.

1.8 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the serial peripheral interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PC0	Input or Output		**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.
SRD0	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received.
PC4	Input or Output		**Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.

1.12 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56303 support circuit-board test strategies based on the **IEEE®** Std. 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of **IEEE** and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

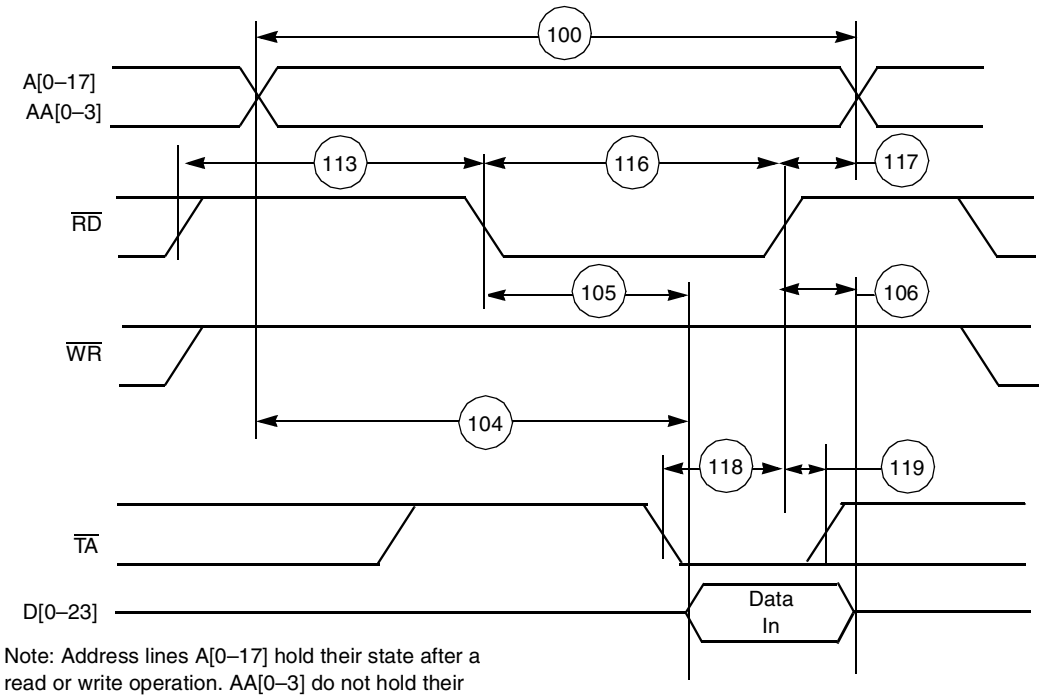
Table 1-16. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted after powerup.
$\overline{\text{DE}}$	Input/ Output (open-drain)	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.
Note: All inputs are 5 V tolerant.			

2.5.4 Reset, Stop, Mode Select, and Interrupt Timing

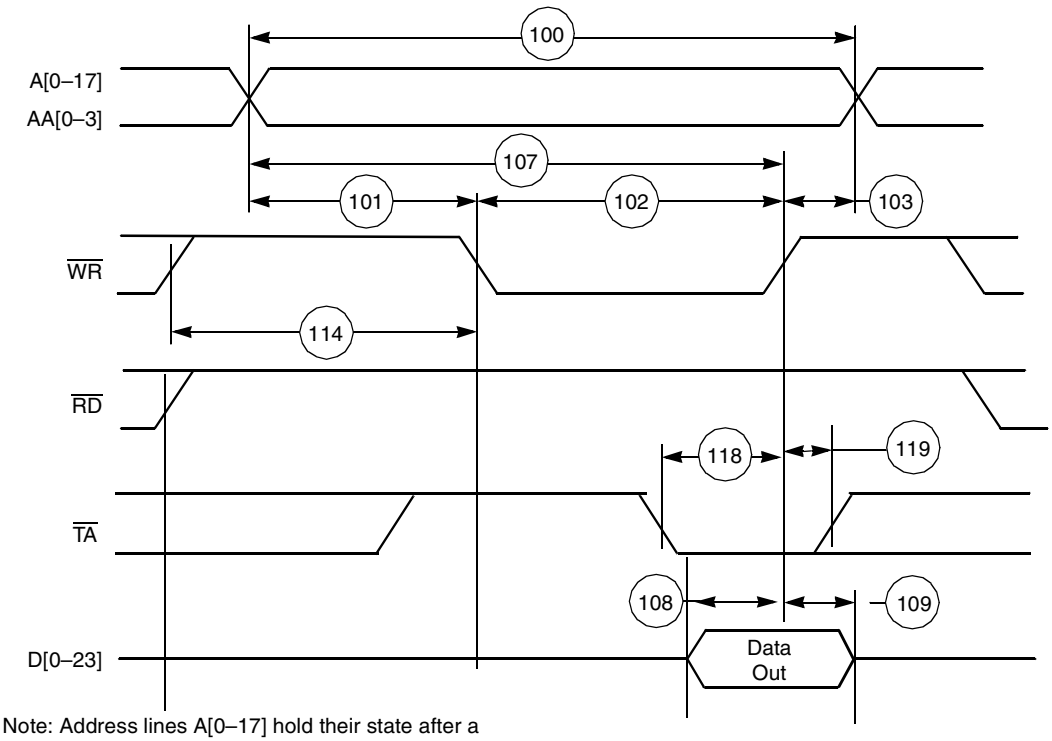
Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled • Power on, internal oscillator • During STOP, XTAL disabled (PCTL Bit 16 = 0) • During STOP, XTAL enabled (PCTL Bit 16 = 1) • During normal operation	 $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$	 500.0 10.0 0.75 0.75 25.0 25.0	 — — — — — —	 ns µs ms ms ns ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5] • Minimum • Maximum	 $3.25 \times T_C + 2.0$ $20.25 \times T_C + 10$	 34.5 —	 — 212.5	 ns ns
11	Synchronous reset set-up time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 • Minimum • Maximum	 T_C	 5.9 —	 — 10.0	 ns ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output • Minimum • Maximum	 $3.25 \times T_C + 1.0$ $20.25 \times T_C + 1.0$	 33.5 —	 — 203.5	 ns ns
13	Mode select setup time		30.0	—	ns
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	 $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$	 44.5 74.5	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	105.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	$(WS + 3.75) \times T_C - 10.94$	—	Note 8	ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	$(WS + 3.25) \times T_C - 10.94$	—	Note 8	ns
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8] • DRAM for all WS • SRAM WS = 1 • SRAM WS = 2, 3 • SRAM WS ≥ 4	 $(WS + 3.5) \times T_C - 10.94$ $(WS + 3.5) \times T_C - 10.94$ $(WS + 3) \times T_C - 10.94$ $(WS + 2.5) \times T_C - 10.94$	 — — — —	 Note 8 Note 8 Note 8 Note 8	 ns ns ns ns
22	Synchronous interrupt set-up time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to the CLKOUT Transition 2		5.9	T_C	ns
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state • Minimum • Maximum	 $8.25 \times T_C + 1.0$ $24.75 \times T_C + 5.0$	 83.5 —	 — 252.5	 ns ns



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-12. SRAM Read Access



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-13. SRAM Write Access

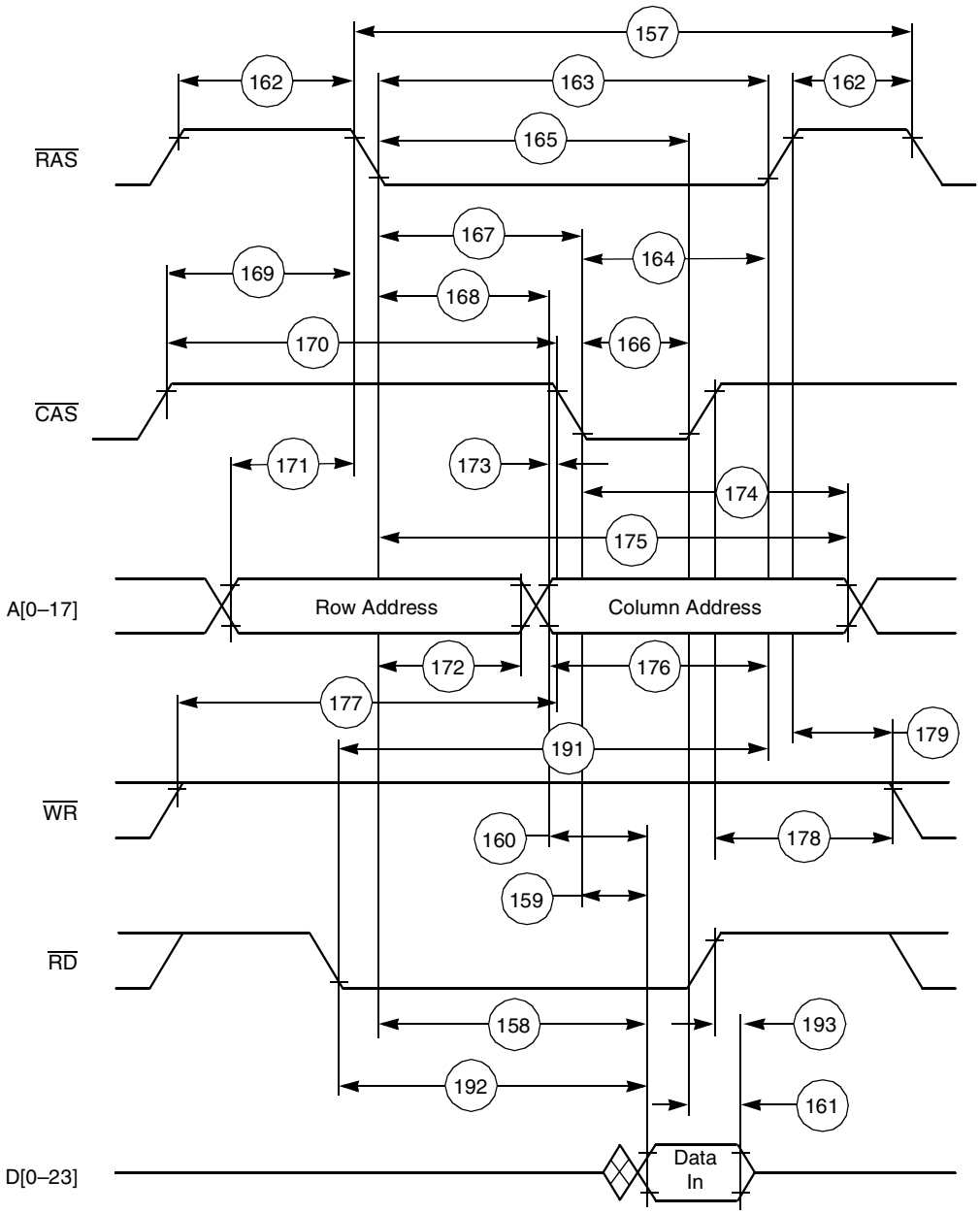


Figure 2-18. DRAM Out-of-Page Read Access

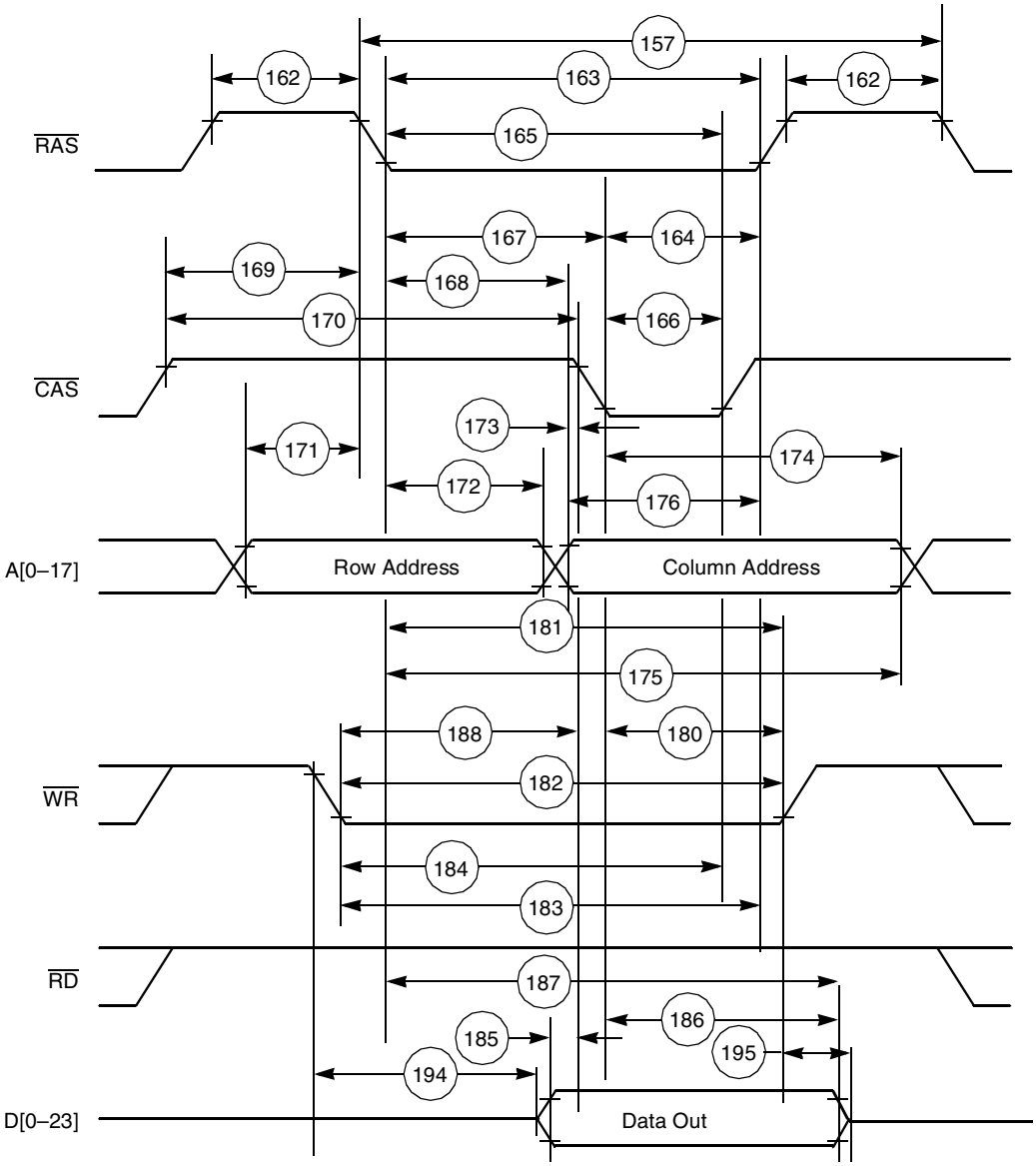


Figure 2-19. DRAM Out-of-Page Write Access

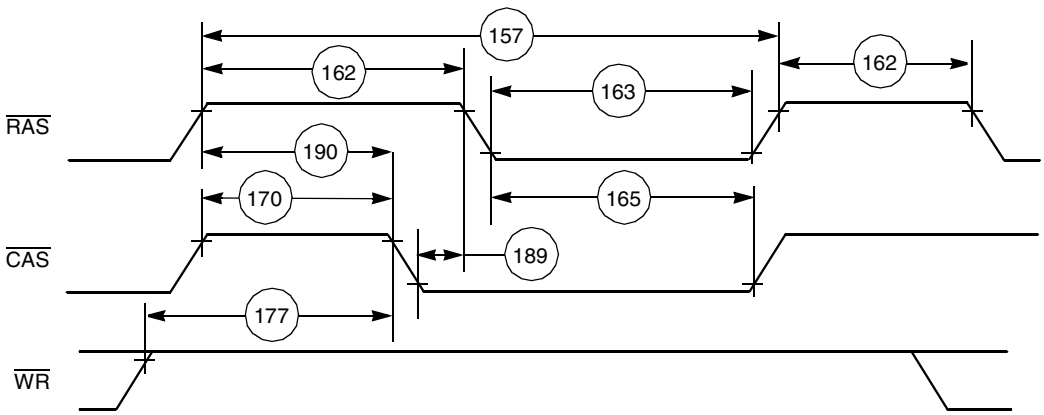


Figure 2-20. DRAM Refresh Access

2.5.5.4 Arbitration Timings

Table 2-14. Arbitration Bus Timings[1]

No.	Characteristics	Expression[2]	100 MHz		Unit
			Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion/deassertion[3]		0.0	4.0	ns
213	$\overline{BG}$ asserted/deasserted to CLKOUT high (setup)		4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted/asserted (hold)		0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input set-up)		4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)		0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)		0.0	4.0	ns
218	CLKOUT high to $\overline{BB}$ deassertion (output)		0.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)		—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	2.5	—	ns
221	CLKOUT high to address and controls high impedance	$0.75 \times T_C$	—	7.5	ns
222	CLKOUT high to AA active	$0.25 \times T_C$	2.5	—	ns
223	CLKOUT high to AA deassertion	maximum: $0.25 \times T_C + 4.0$	2.0	6.5	ns
224	CLKOUT high to AA high impedance	$0.75 \times T_C$	—	7.5	ns

Notes:
1. Synchronous bus arbitration is not recommended. Use Asynchronous mode whenever possible.
2. An expression is used to compute the maximum or minimum value listed, as appropriate. For timing 223, the minimum is an absolute value.
3. T212 is valid for Address Trace mode when the ATE bit in the Operating Mode Register is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.

2.5.5.5 Asynchronous Bus Arbitration Timings

Table 2-15. Asynchronous Bus Timings[1, 2]

No.	Characteristics	Expression[3]	100 MHz[4]		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion[5]	2.5 × Tc + 5	—	30	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion[5]	2 × Tc + 5	25	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
2. If Asynchronous Arbitration mode is active, none of the timings in **Table 2-14** is required.
3. An expression is used to compute the maximum or minimum value listed, as appropriate.
4. Asynchronous Arbitration mode is recommended for operation at 100 MHz.
5. In order to guarantee timings 250, and 251, BG inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in **Figure 2-26**.

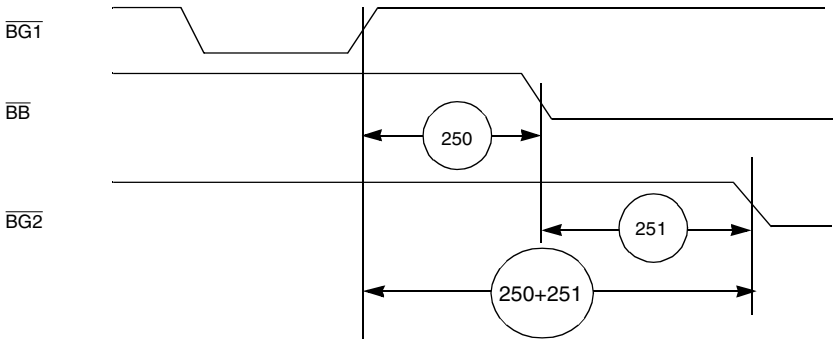


Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

2.5.8 ESSI0/ESSI1 Timing

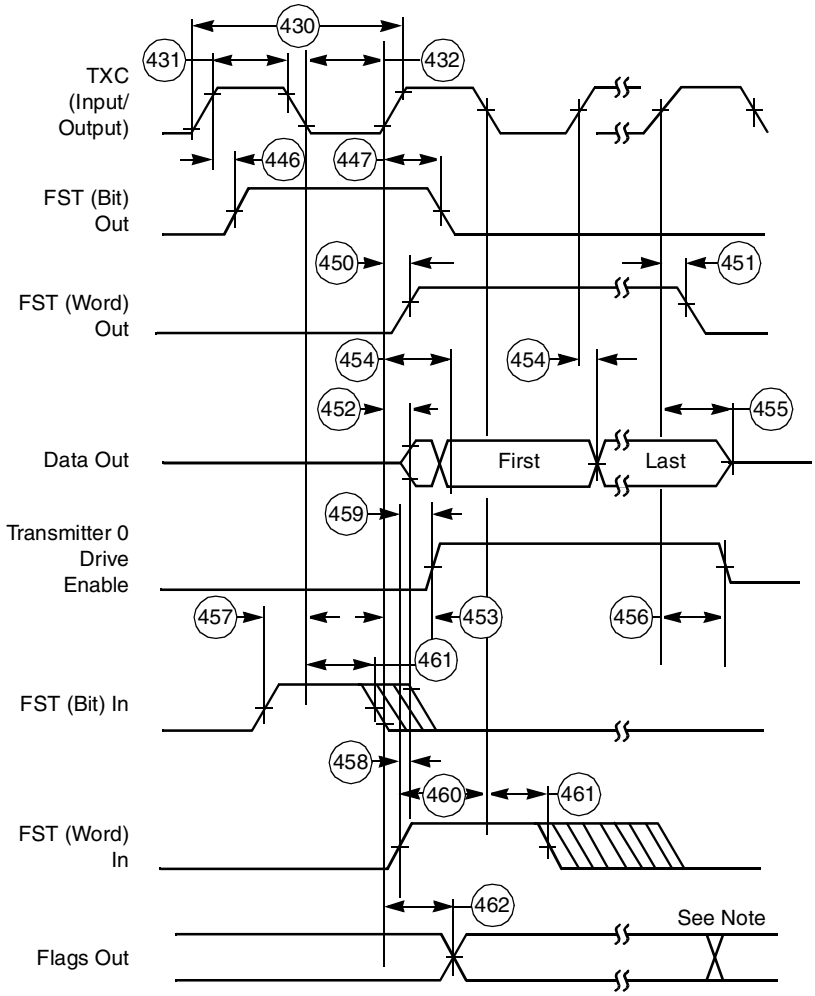
Table 2-18. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	30.0 40.0	— —	x ck i ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C$ - 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C$ –10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in set-up time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr)[7] high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl)[7] high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input set-up before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (word-length) low			— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	x ck i ck	ns

Table 2-18. ESSI Timings (Continued)

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Condition[5]	Unit
				Min	Max		
453	TXC rising edge to transmitter 0 drive enable assertion			— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid			— —	20.0[8] 10.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[3]			— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to Transmitter 0 drive enable deassertion[3]			— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) set-up time before TXC falling edge[2]			2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance			—	27.0	—	ns
459	FST input (wl) to Transmitter 0 drive enable assertion			—	31.0	—	ns
460	FST input (wl) set-up time before TXC falling edge			2.5 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge			4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge			— —	32.0 18.0	x ck i ck	ns

Notes:
1. For the internal clock, the external clock cycle is defined by Icyc (see Timing 7) and the ESSI Control Register.
2. The word-length-relative frame sync signal waveform operates the same way as the bit-length frame sync signal waveform, but spreads from one serial clock before the first bit clock (same as the Bit Length Frame Sync signal) until the one before last bit clock of the first word in the frame.
3. Periodically sampled and not 100 percent tested
4. V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF
5. TXC (SCK Pin) = transmit clock
   RXC (SC0 or SCK pin) = receive clock
   FST (SC2 pin) = transmit frame sync
   FSR (SC1 or SC2 pin) receive frame sync
6. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, Asynchronous mode
   (asynchronous implies that TXC and RXC are two different clocks)
   i ck s = Internal Clock, Synchronous mode
   (synchronous implies that TXC and RXC are the same clock)
7. bl = bit length; wl = word length; wr = word length relative.
8. If the DSP core writes to the transmit register during the last cycle before causing an underrun error, the delay is 20 ns + (0.5 × T_C).
9. An expression is used to compute the number listed as the minimum or maximum value as appropriate.



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-38. ESSI Transmitter Timing

2.5.12 OnCE Module Timing

Table 2-22. OnCE Module Timing

No.	Characteristics	Expression	Min	Max	Unit
500	TCK frequency of operation	Max 22.0 MHz	0.0	22.0	MHz
514	$\overline{DE}$ assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	20.0	—	ns
515	Response time when DSP56303 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	67.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 5.0$	25.0	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$, $V_{CC} = 1.8\ V \pm 0.1\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$.				

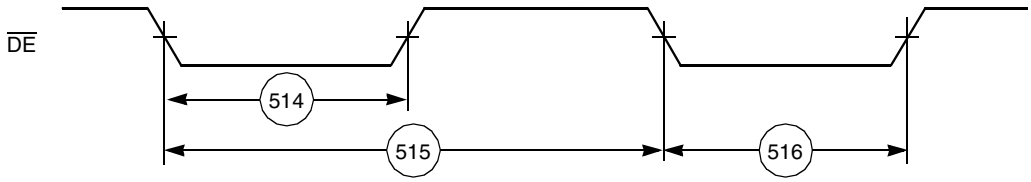


Figure 2-48. OnCE—Debug Request

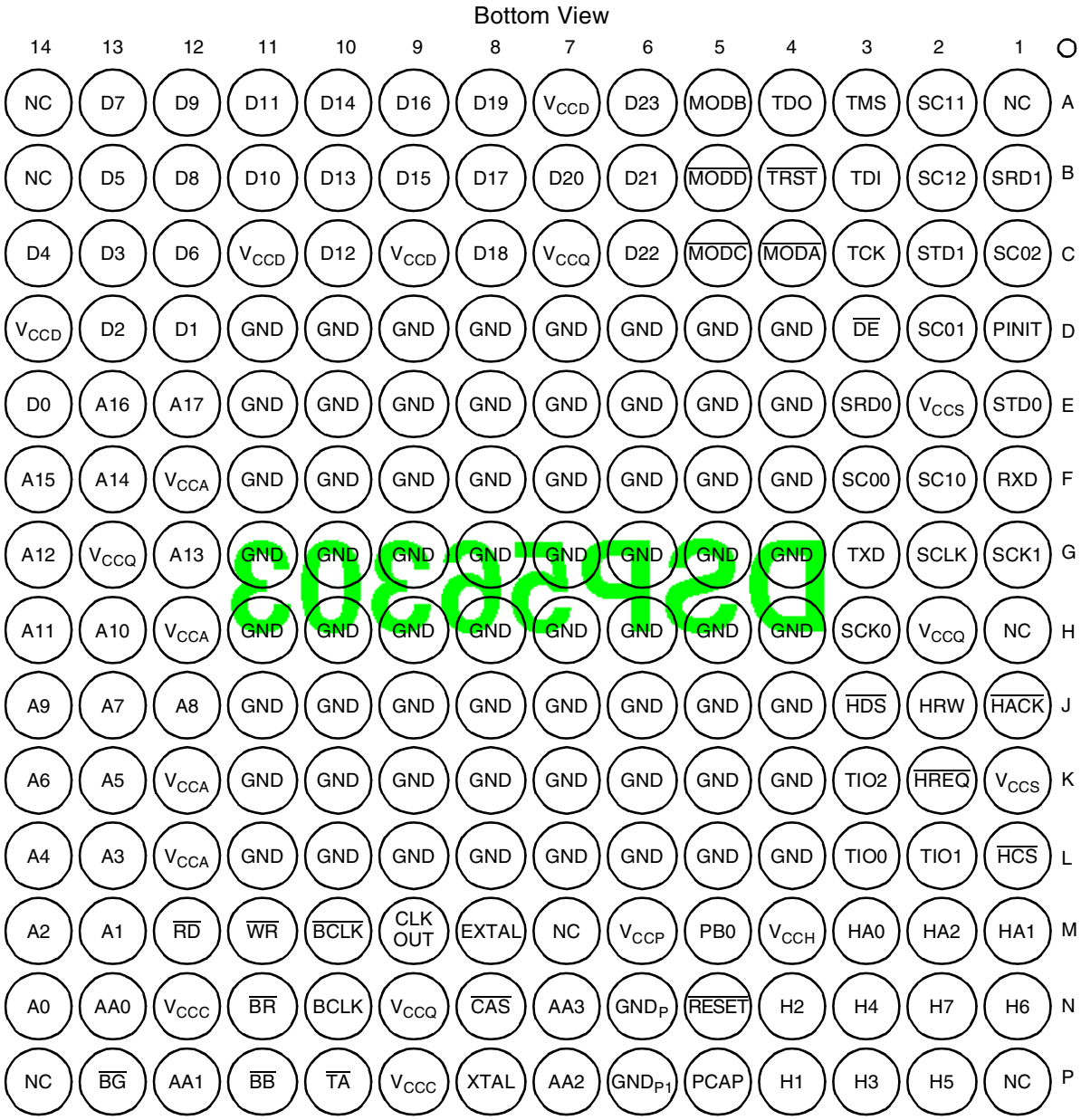


Figure 3-5. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	Not Connected (NC), reserved	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQ}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	F8	GND	J9	H4	N3
GND	F9	GND	J10	H5	P2
GND	F10	GND	J11	H6	N1
GND	F11	GND	K4	H7	N2
GND	G4	GND	K5	HA0	M3
GND	G5	GND	K6	HA1	M1
GND	G6	GND	K7	HA10	L1
GND	G7	GND	K8	HA2	M2
GND	G8	GND	K9	HA8	M1
GND	G9	GND	K10	HA9	M2
GND	G10	GND	K11	$\overline{\text{HACK}}$/HACK	J1
GND	G11	GND	L4	HAD0	M5
GND	H4	GND	L5	HAD1	P4
GND	H5	GND	L6	HAD2	N4
GND	H6	GND	L7	HAD3	P3
GND	H7	GND	L8	HAD4	N3
GND	H8	GND	L9	HAD5	P2
GND	H9	GND	L10	HAD6	N1
GND	H10	GND	L11	HAD7	N2
GND	H11	GND_P	N6	$\overline{\text{HAS}}$/HAS	M3
GND	J4	GND_{P1}	P6	$\overline{\text{HCS}}$/HCS	L1
GND	J5	H0	M5	$\overline{\text{HDS}}$/HDS	J3
GND	J6	H1	P4	$\overline{\text{HRD}}$/HRD	J2
GND	J7	H2	N4	$\overline{\text{HREQ}}$/HREQ	K2
GND	J8	H3	P3	$\overline{\text{HRRQ}}$/HRRQ	J1

- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.
- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{\text{RESET}}$ must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of $\overline{\text{RESET}}$.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $I = C \times V \times f$

Where:

C	=	node/pin capacitance
V	=	voltage swing
f	=	frequency of node/pin toggle

Example 4-1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.

Power Consumption Benchmark A

The following benchmark program evaluates DSP56303 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;************************************************************************
;************************************************************************
;*                                                                      *
;*                    CHECKS   Typical Power Consumption                *
;*                                                                      *
;************************************************************************

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0; INTERNAL X-data memory starting address
INT_YDAT  EQU $0; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "intequ.asm"

        list

        org     P:START
;
        movep #$0243FF,x:M_BCR ;; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
        movep   #$0d0000,x:M_PCTL      ; XTAL disable
                                       ; PLL enable
                                       ; CLKOUT disable
;
; Load the program
;
        move    #INT_PROG,r0
        move    #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,p:(r0)+
        nop
PLOAD_LOOP
;
; Load the X-data
;
        move    #INT_XDAT,r0
        move    #XDAT_START,r1
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
```

```
M_DI EQU 12                          ; Data Input
M_DO EQU 13                          ; Data Output
M_PCE EQU  15                        ; Prescaled Clock Enable
M_TOF EQU 20                         ; Timer Overflow Flag
M_TCF EQU 21                         ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000                    ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22

;      Timer Control Bits
M_TC0 EQU 4                          ; Timer Control 0
M_TC1 EQU 5                          ; Timer Control 1
M_TC2 EQU 6                          ; Timer Control 2
M_TC3 EQU 7                          ; Timer Control 3


;------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4                    ; DMA Status Register
M_DOR0 EQU $FFFFF3                   ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2                   ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1                   ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0                   ; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF                   ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE                   ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED                   ; DMA0 Counter
M_DCR0 EQU $FFFFEC                   ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB                   ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA                   ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9                   ; DMA1 Counter
M_DCR1 EQU $FFFFE8                   ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7                   ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6                   ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5                   ; DMA2 Counter
M_DCR2 EQU $FFFFE4                   ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3                   ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2                   ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1                   ; DMA3 Counter
M_DCR3 EQU $FFFFE0                   ; DMA3 Control Register
```

```
;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF                  ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE                  ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD                  ; DMA4 Counter
M_DCR4 EQU $FFFFDC                  ; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB                  ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA                  ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9                  ; DMA5 Counter
M_DCR5 EQU $FFFFD8                  ; DMA5 Control Register

;       DMA Control Register

M_DSS EQU $3                        ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0                        ; DMA Source Memory space 0
M_DSS1 EQU 1                        ; DMA Source Memory space 1
M_DDS EQU $C                        ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2                        ; DMA Destination Memory Space 0
M_DDS1 EQU 3                        ; DMA Destination Memory Space 1
M_DAM EQU $3f0                      ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0  EQU 4                       ; DMA Address Mode 0
M_DAM1  EQU 5                       ; DMA Address Mode 1
M_DAM2  EQU 6                       ; DMA Address Mode 2
M_DAM3  EQU 7                       ; DMA Address Mode 3
M_DAM4  EQU 8                       ; DMA Address Mode 4
M_DAM5  EQU 9                       ; DMA Address Mode 5
M_D3D EQU 10                        ; DMA Three Dimensional Mode
M_DRS EQU $F800                     ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16                       ; DMA Continuous Mode
M_DPR EQU $60000                    ; DMA Channel Priority
M_DPR0 EQU 17                       ; DMA Channel Priority Level (low)
M_DPR1 EQU 18                       ; DMA Channel Priority Level (high)
M_DTM EQU $380000                   ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19                       ; DMA Transfer Mode 0
M_DTM1 EQU 20                       ; DMA Transfer Mode 1
M_DTM2 EQU 21                       ; DMA Transfer Mode 2
M_DIE EQU 22                        ; DMA Interrupt Enable bit
M_DE EQU 23                         ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F                       ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0                        ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1                        ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2                        ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3                        ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4                        ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5                        ; DMA Channel Transfer Done Status 5
M_DACT EQU  8                       ; DMA Active State
M_DCH EQU  $E00                     ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU  9                       ; DMA Active Channel 0
M_DCH1 EQU  10                      ; DMA Active Channel 1
M_DCH2 EQU  11                      ; DMA Active Channel 2

;---------------------------------------------------------------------------
```