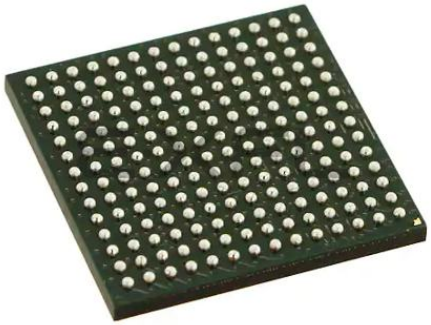

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56303vl100b1

Table of Contents

Data Sheet Conventions

OVERBAR	Indicates a signal that is active when pulled low (For example, the RESET pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	PIN	True	Asserted	V_{IL}/V_{OL}
	PIN	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Target Applications

Examples include:

- Multi-line voice/data/fax processing
- Video conferencing
- Audio applications
- Control

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56303 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56303 Documentation

Name	Description	Order Number
DSP56303 User's Manual	Detailed functional description of the DSP56303 memory configuration, operation, and register programming	DSP56303UM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56303 product website

1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Type	State During Reset	State During Stop or Wait	Signal Description
D[0–23]	Input/ Output	Ignored Input	Last state: *Input*: Ignored *Output*: Tri-stated	**Data Bus**—When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tri-stated.

1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
AA[0–3]	Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals.
$\overline{\text{RAS}}$[0–3]	Output		**Row Address Strobe**—When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated.
$\overline{\text{TA}}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56303 is the bus master and there is no external bus activity, or the DSP56303 is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. To use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion; otherwise, improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously depending on the setting of the TAS bit in the Operating Mode Register. $\overline{\text{TA}}$ functionality cannot be used during DRAM type accesses; otherwise improper operation may result.
$\overline{\text{BR}}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Asserted when the DSP requests bus mastership. $\overline{\text{BR}}$ is deasserted when the DSP no longer needs the bus. $\overline{\text{BR}}$ may be asserted or deasserted independently of whether the DSP56303 is a bus master or a bus slave. Bus “parking” allows $\overline{\text{BR}}$ to be deasserted even though the DSP56303 is the bus master. (See the description of bus “parking” in the $\overline{\text{BB}}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{\text{BR}}$ to be asserted under software control even though the DSP does not need the bus. $\overline{\text{BR}}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{\text{BR}}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{\text{BR}}$ is deasserted and the arbitration is reset to the bus slave state.

1.8 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the serial peripheral interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PC0	Input or Output		**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.
SRD0	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received.
PC4	Input or Output		**Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.

1.10 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

2.3 Thermal Characteristics

Table 2-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	MAP-BGA[3] Value	MAP-BGA[4] Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	56	57	28	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	11	15	—	°C/W
Thermal characterization parameter	Ψ_{JT}	7	8	—	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per JEDEC Specification JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values. See note 1 for test board conditions.
4. These are simulated values. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

2.4 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 0.8 × V_{CC}	 — — —	 V_{CC} 5.25 V_{CC}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 0.2 × V_{CC}	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7] • CMOS (I_{OH} = –10 µA)[5]	V_{OH}	 2.4 V_{CC} – 0.01	 — —	 — —	 V V
Output low voltage • TTL (I_{OL} = 1.6 mA, open-drain pins I_{OL} = 6.7 mA)[5,7] • CMOS (I_{OL} = 10 µA)[5]	V_{OL}	 — —	 — —	 0.4 0.01	 V V
Internal supply current[2]: • In Normal mode • In Wait mode[3] • In Stop mode[4]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 127 7.5 100	 — — —	 mA mA µA
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Table 2-3. DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit

Notes:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
2. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 100°C.
3. In order to obtain these results, all inputs must be terminated (that is, not allowed to float).
4. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
5. Periodically sampled and not 100 percent tested.
6. V_{CC} = 3.3 V ±0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CC} and the maximum V_{ILX} should be no higher than 0.1 × V_{CC}.

2.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.5.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—

2.5.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled • Power on, internal oscillator • During STOP, XTAL disabled (PCTL Bit 16 = 0) • During STOP, XTAL enabled (PCTL Bit 16 = 1) • During normal operation	 $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$	 500.0 10.0 0.75 0.75 25.0 25.0	 — — — — — —	 ns µs ms ms ns ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5] • Minimum • Maximum	 $3.25 \times T_C + 2.0$ $20.25 \times T_C + 10$	 34.5 —	 — 212.5	 ns ns
11	Synchronous reset set-up time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 • Minimum • Maximum	 T_C	 5.9 —	 — 10.0	 ns ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output • Minimum • Maximum	 $3.25 \times T_C + 1.0$ $20.25 \times T_C + 1.0$	 33.5 —	 — 203.5	 ns ns
13	Mode select setup time		30.0	—	ns
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	 $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$	 44.5 74.5	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	105.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	$(WS + 3.75) \times T_C - 10.94$	—	Note 8	ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	$(WS + 3.25) \times T_C - 10.94$	—	Note 8	ns
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8] • DRAM for all WS • SRAM WS = 1 • SRAM WS = 2, 3 • SRAM WS ≥ 4	 $(WS + 3.5) \times T_C - 10.94$ $(WS + 3.5) \times T_C - 10.94$ $(WS + 3) \times T_C - 10.94$ $(WS + 2.5) \times T_C - 10.94$	 — — — —	 Note 8 Note 8 Note 8 Note 8	 ns ns ns ns
22	Synchronous interrupt set-up time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to the CLKOUT Transition 2		5.9	T_C	ns
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state • Minimum • Maximum	 $8.25 \times T_C + 1.0$ $24.75 \times T_C + 5.0$	 83.5 —	 — 252.5	 ns ns

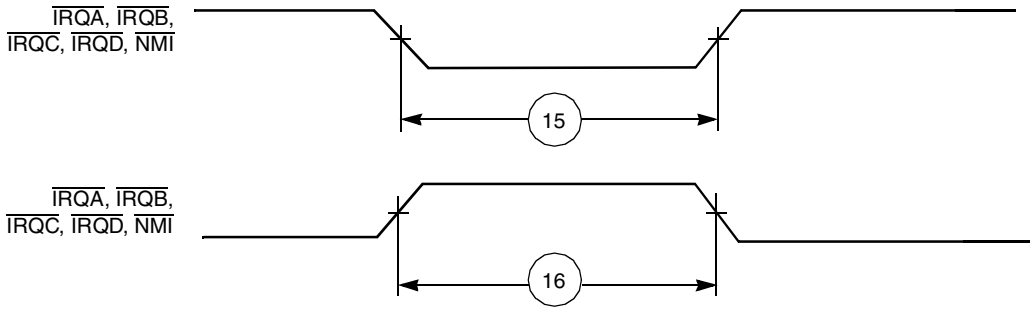

Figure 2-6. External Interrupt Timing (Negative Edge-Triggered)

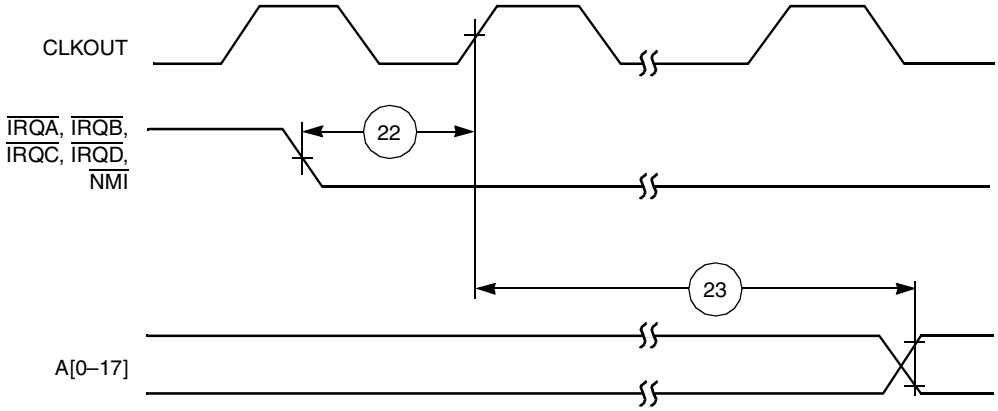

Figure 2-7. Synchronous Interrupt from Wait State Timing

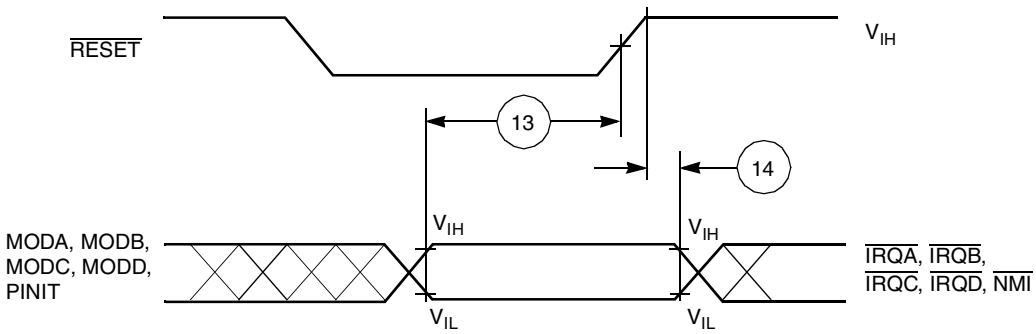

Figure 2-8. Operating Mode Select Timing

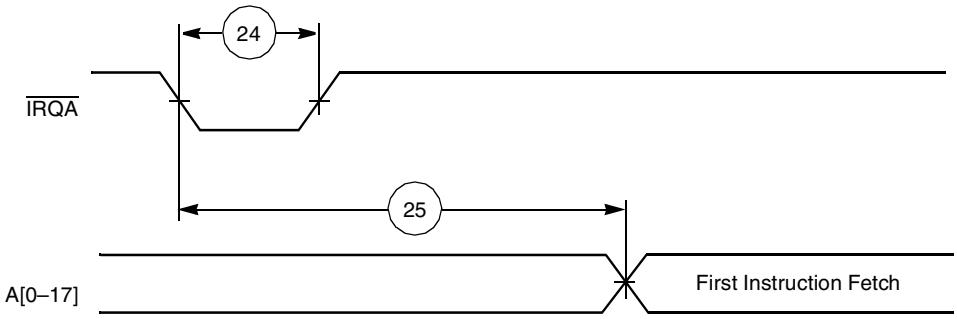

Figure 2-9. Recovery from Stop State Using $\overline{\text{IRQA}}$

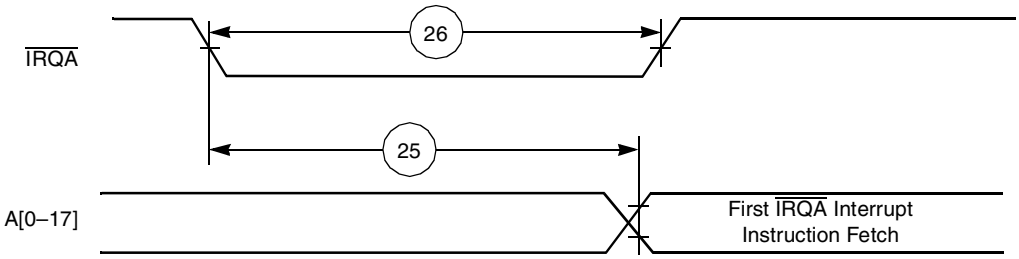

Figure 2-10. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

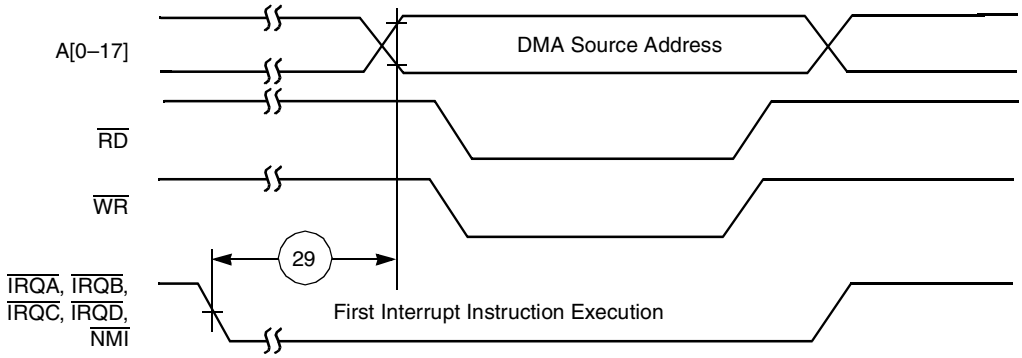

Figure 2-11. External Memory Access (DMA Source) Timing

Table 2-8. SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	100 MHz		Unit
				Min	Max	
111	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C + 0.2$ [1 ≤WS ≤3]	—	2.7	ns
			$1.25 \times TC + 0.2$ [4 ≤WS ≤7]	—	12.7	ns
			$2.25 \times T_C + 0.2$ [WS > 8]	—	22.7	ns
112	Previous $\overline{RD}$ deassertion to data active (write)	—	$1.25 \times T_C - 4.0$ [1 ≤WS ≤3]	8.5	—	ns
			$2.25 \times T_C - 4.0$ [4 ≤WS ≤7]	18.5	—	ns
			$3.25 \times T_C - 4.0$ [WS > 8]	28.5	—	ns
113	$\overline{RD}$ deassertion time	—	$0.75 \times T_C - 4.0$ [1 ≤WS ≤3]	3.5	—	ns
			$1.75 \times T_C - 4.0$ [4 ≤WS ≤7]	13.5	—	ns
			$2.75 \times T_C - 4.0$ [WS ≥ 8]	23.5	—	ns
114	$\overline{WR}$ deassertion time	—	$0.5 \times T_C - 4.0$ [WS = 1]	1.0	—	ns
			$T_C - 4.0$ [2 ≤WS ≤3]	6.0	—	ns
			$2.5 \times T_C - 4.0$ [4 ≤WS ≤7]	21.0	—	ns
			$3.5 \times T_C - 4.0$ [WS ≥ 8]	31.0	—	ns
115	Address valid to $\overline{RD}$ assertion	—	$0.5 \times T_C - 4.0$	1.0	—	ns
116	$\overline{RD}$ assertion pulse width	—	$(WS + 0.25) \times T_C - 4.0$	8.5	—	ns
117	$\overline{RD}$ deassertion to address not valid	—	$0.25 \times T_C - 2.0$ [1 ≤WS ≤3]	0.5	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤WS ≤7]	10.5	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	20.5	—	ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[4]	—	$0.25 \times T_C + 2.0$	4.5	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion	—	—	0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR. An expression is used to compute the number listed as the minimum or maximum value, as appropriate.
2. Timings 100, 107 are guaranteed by design, not tested.
3. All timings for 100 MHz are measured from 0.5 × Vcc to 0.5 × Vcc.
4. Timing 118 is relative to the deassertion edge of $\overline{RD}$ or $\overline{WR}$ even if $\overline{TA}$ remains asserted.
5. V_{CC} = 3.3 V ±0.3 V; T_J = –40°C to +100°C, C_L = 50 pF

Table 2-9. DRAM Page Mode Timings, Three Wait States[1,2,3]

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$4 \times T_C$	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$3.5 \times T_C$	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 5.7$	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 5.7$	—	24.3	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00, 01—not applicable • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 — $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — 41.5 61.5	 — — —	 — ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 4.0$	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.5$	0.5	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 5.7$	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. The asynchronous delays specified in the expressions are valid for the DSP56303.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences). An expression is used to compute the number listed as the minimum or maximum value listed, as appropriate.
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

2.5.9 Timer Timing

Table 2-19. Timer Timing[1]

No.	Characteristics	Expression[2]	100 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	22.0	—	ns
481	TIO High	$2 \times T_C + 2.0$	22.0	—	ns
482	Timer set-up time from TIO (Input) assertion to CLKOUT rising edge		9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	$10.25 \times T_C + 1.0$	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 5.5 —	 — 24.8	 ns ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 5.5 —	 — 24.8	 ns ns

Notes: 1. V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF.
2. An expression is used to compute the number listed as the minimum or maximum value as appropriate.

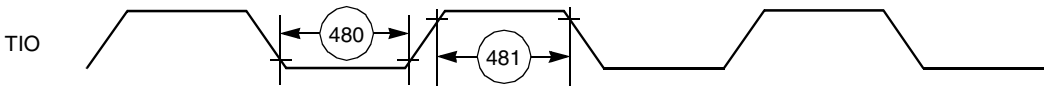

Figure 2-40. TIO Timer Event Input Restrictions

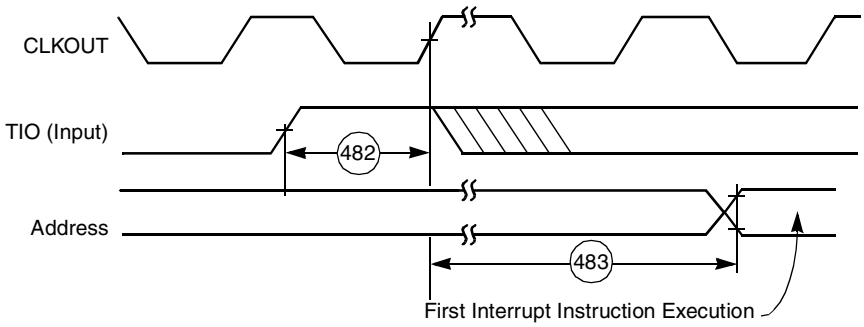

Figure 2-41. Timer Interrupt Generation

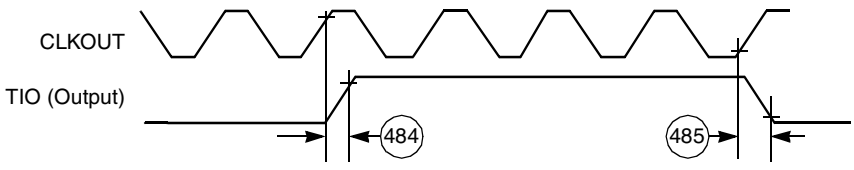

Figure 2-42. External Pulse Generation

2.5.12 OnCE Module Timing

Table 2-22. OnCE Module Timing

No.	Characteristics	Expression	Min	Max	Unit
500	TCK frequency of operation	Max 22.0 MHz	0.0	22.0	MHz
514	$\overline{DE}$ assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	20.0	—	ns
515	Response time when DSP56303 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	67.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 5.0$	25.0	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$, $V_{CC} = 1.8\ V \pm 0.1\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$.				

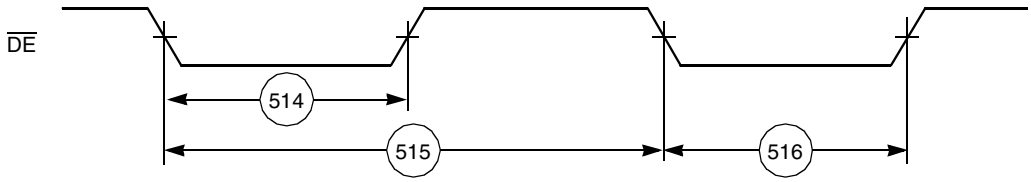

Figure 2-48. OnCE—Debug Request

Table 3-1. DSP56303 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	SRD1 or PD4	26	GND_S	51	AA2/$\overline{RAS2}$
2	STD1 or PD5	27	TIO2	52	$\overline{CAS}$
3	SC02 or PC2	28	TIO1	53	XTAL
4	SC01 or PC1	29	TIO0	54	GND_Q
5	$\overline{DE}$	30	$\overline{HCS}$/HCS, HA10, or PB13	55	EXTAL
6	PINIT/$\overline{NMI}$	31	HA2, HA9, or PB10	56	V_{CCQ}
7	SRD0 or PC4	32	HA1, HA8, or PB9	57	V_{CCC}
8	V_{CCS}	33	HA0, $\overline{HAS}$/HAS, or PB8	58	GND_C
9	GND_S	34	H7, HAD7, or PB7	59	CLKOUT
10	STD0 or PC5	35	H6, HAD6, or PB6	60	BCLK
11	SC10 or PD0	36	H5, HAD5, or PB5	61	$\overline{BCLK}$
12	SC00 or PC0	37	H4, HAD4, or PB4	62	$\overline{TA}$
13	RXD or PE0	38	V_{CCH}	63	$\overline{BR}$
14	TXD or PE1	39	GND_H	64	$\overline{BB}$
15	SCLK or PE2	40	H3, HAD3, or PB3	65	V_{CCC}
16	SCK1 or PD3	41	H2, HAD2, or PB2	66	GND_C
17	SCK0 or PC3	42	H1, HAD1, or PB1	67	$\overline{WR}$
18	V_{CCQ}	43	H0, HAD0, or PB0	68	$\overline{RD}$
19	GND_Q	44	$\overline{RESET}$	69	AA1/$\overline{RAS1}$
20	Not Connected (NC), reserved	45	V_{CCP}	70	AA0/$\overline{RAS0}$
21	$\overline{HDS}$/HDS, $\overline{HWR}$/HWR, or PB12	46	PCAP	71	$\overline{BG}$
22	HRW, $\overline{HRD}$/HRD, or PB11	47	GND_P	72	A0
23	$\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, or PB15	48	GND_{P1}	73	A1
24	$\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, or PB14	49	Not Connected (NC), reserved	74	V_{CCA}
25	V_{CCS}	50	AA3/$\overline{RAS3}$	75	GND_A

Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
H1	42	$\overline{\text{HRD}}$/HRD	22	PB2	41
H2	41	$\overline{\text{HREQ}}$/HREQ	24	PB3	40
H3	40	$\overline{\text{HRRQ}}$/HRRQ	23	PB4	37
H4	37	HRW	22	PB5	36
H5	36	$\overline{\text{HTRQ}}$/HTRQ	24	PB6	35
H6	35	$\overline{\text{HWR}}$/HWR	21	PB7	34
H7	34	$\overline{\text{IRQA}}$	137	PB8	33
HA0	33	$\overline{\text{IRQB}}$	136	PB9	32
HA1	32	$\overline{\text{IRQC}}$	135	PC0	12
HA10	30	$\overline{\text{IRQD}}$	134	PC1	4
HA2	31	MODA	137	PC2	3
HA8	32	MODB	136	PC3	17
HA9	31	MODC	135	PC4	7
$\overline{\text{HACK}}$/HACK	23	MODD	134	PC5	10
HAD0	43	NC	20	PCAP	46
HAD1	42	NMI	6	PD0	11
HAD2	41	NC	49	PD1	144
HAD3	40	PB0	43	PD2	143
HAD4	37	PB1	42	PD3	16
HAD5	36	PB10	31	PD4	1
HAD6	35	PB11	22	PD5	2
HAD7	34	PB12	21	PE0	13
$\overline{\text{HAS}}$/HAS	33	PB13	30	PE1	14
$\overline{\text{HCS}}$/HCS	30	PB14	24	PE2	15
$\overline{\text{HDS}}$/HDS	21	PB15	23	PINIT	6

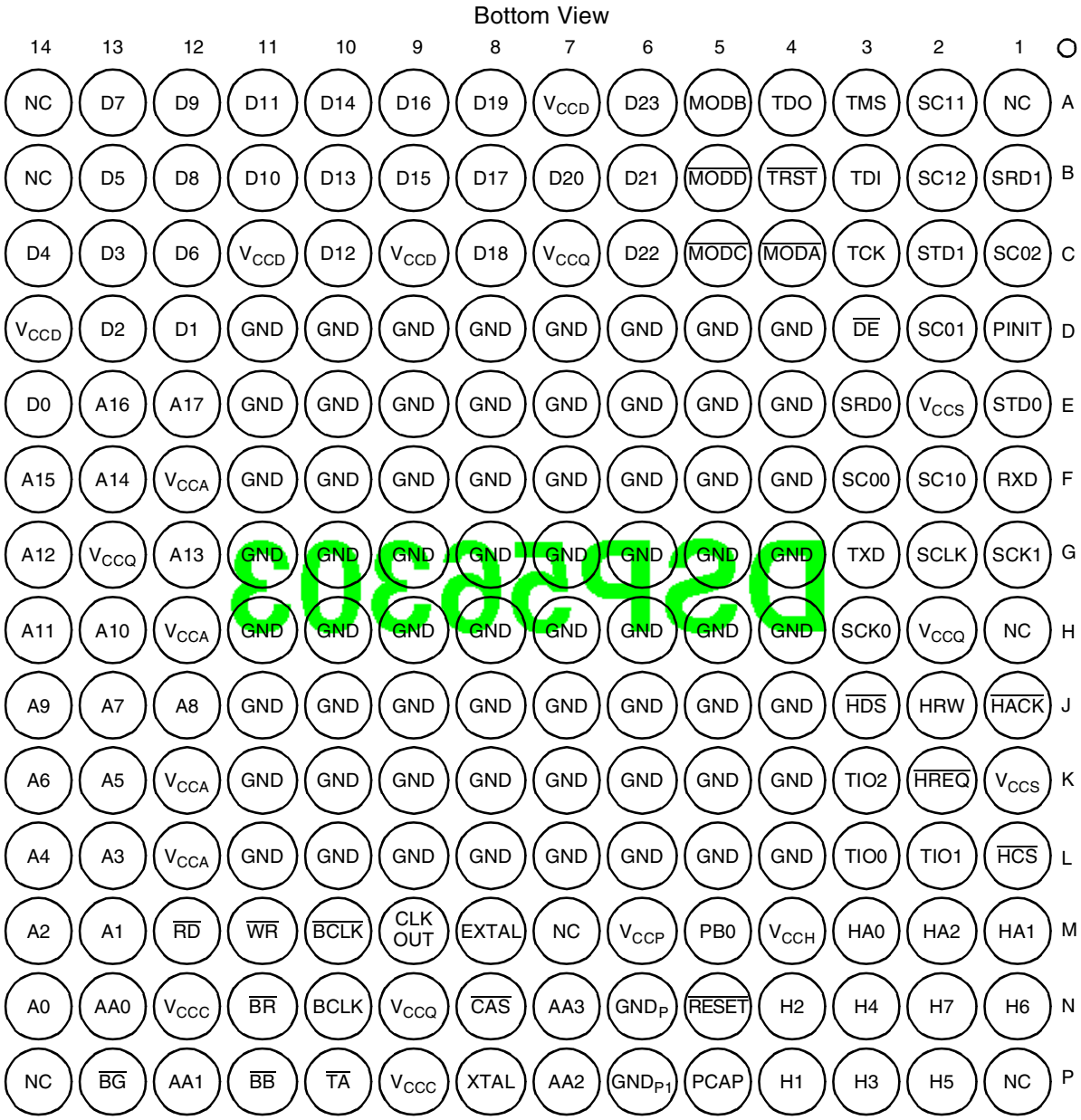

Figure 3-5. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	F8	GND	J9	H4	N3
GND	F9	GND	J10	H5	P2
GND	F10	GND	J11	H6	N1
GND	F11	GND	K4	H7	N2
GND	G4	GND	K5	HA0	M3
GND	G5	GND	K6	HA1	M1
GND	G6	GND	K7	HA10	L1
GND	G7	GND	K8	HA2	M2
GND	G8	GND	K9	HA8	M1
GND	G9	GND	K10	HA9	M2
GND	G10	GND	K11	$\overline{\text{HACK}}$/HACK	J1
GND	G11	GND	L4	HAD0	M5
GND	H4	GND	L5	HAD1	P4
GND	H5	GND	L6	HAD2	N4
GND	H6	GND	L7	HAD3	P3
GND	H7	GND	L8	HAD4	N3
GND	H8	GND	L9	HAD5	P2
GND	H9	GND	L10	HAD6	N1
GND	H10	GND	L11	HAD7	N2
GND	H11	GND_P	N6	$\overline{\text{HAS}}$/HAS	M3
GND	J4	GND_{P1}	P6	$\overline{\text{HCS}}$/HCS	L1
GND	J5	H0	M5	$\overline{\text{HDS}}$/HDS	J3
GND	J6	H1	P4	$\overline{\text{HRD}}$/HRD	J2
GND	J7	H2	N4	$\overline{\text{HREQ}}$/HREQ	K2
GND	J8	H3	P3	$\overline{\text{HRRQ}}$/HRRQ	J1

```
M_BRP EQU 23                        ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3                        ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2                        ; Address Attribute Pin Polarity
M_BPEN EQU 3                        ; Program Space Enable
M_BXEN EQU 4                        ; X Data Space Enable
M_BYEN EQU 5                        ; Y Data Space Enable
M_BAM EQU 6                         ; Address Muxing
M_BPAC EQU 7                        ; Packing Enable
M_BNC EQU $F00                      ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000                   ; Address to Compare Bits Mask (BAC0-BAC11)


;       control and status bits in SR

M_CP EQU $c00000                    ; mask for CORE-DMA priority bits in SR
M_CA EQU 0                          ; Carry
M_V EQU 1                           ; Overflow
M_Z EQU 2                           ; Zero
M_N EQU 3                           ; Negative
M_U EQU 4                           ; Unnormalized
M_E EQU 5                           ; Extension
M_L EQU 6                           ; Limit
M_S EQU 7                           ; Scaling Bit
M_I0 EQU 8                          ; Interupt Mask Bit 0
M_I1 EQU 9                          ; Interupt Mask Bit 1
M_S0 EQU 10                         ; Scaling Mode Bit 0
M_S1 EQU 11                         ; Scaling Mode Bit 1
M_SC EQU 13                         ; Sixteen_Bit Compatibility
M_DM EQU 14                         ; Double Precision Multiply
M_LF EQU 15                         ; DO-Loop Flag
M_FV EQU 16                         ; DO-Forever Flag
M_SA EQU 17                         ; Sixteen-Bit Arithmetic
M_CE EQU 19                         ; Instruction Cache Enable
M_SM EQU 20                         ; Arithmetic Saturation
M_RM EQU 21                         ; Rounding Mode
M_CP0 EQU 22                        ; bit 0 of priority bits in SR
M_CP1 EQU 23                        ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU $300                      ; mask for CORE-DMA priority bits in OMR
M_MA    equ0                        ; Operating Mode A
M_MB   equ1                         ; Operating Mode B
M_MC    equ2                        ; Operating Mode C
M_MD    equ3                        ; Operating Mode D
M_EBD EQU 4                         ; External Bus Disable bit in OMR
M_SD EQU 6                          ; Stop Delay
M_MS EQU 7                          ; Memory Switch bit in OMR
M_CDP0 EQU 8                        ; bit 0 of priority bits in OMR
M_CDP1 EQU 9                        ; bit 1 of priority bits in OMR
M_BEN   EQU 10                      ; Burst Enable
M_TAS  EQU 11                       ; TA Synchronize Select
M_BRT  EQU 12                       ; Bus Release Timing
M_ATE EQU 15                        ; Address Tracing Enable bit in OMR.
M_XYS EQU 16                        ; Stack Extension space select bit in OMR.
M_EUN EQU 17                        ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18                        ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19                        ; Extended WRaP flag in OMR.
```

```
I_TIM1OF EQU I_VEC+$2A              ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C               ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E              ; TIMER 2 overflow

;------------------------------------------------------------------------
; ESSI Interrupts
;------------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30               ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32              ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34              ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36               ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38              ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A              ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40               ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42              ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44              ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46               ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48              ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A              ; ESSI1 Transmit last slot

;------------------------------------------------------------------------
; SCI Interrupts
;------------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50               ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52              ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54               ; SCI Transmit Data
I_SCIIL EQU I_VEC+$56               ; SCI Idle Line
I_SCITM EQU I_VEC+$58               ; SCI Timer

;------------------------------------------------------------------------
; HOST Interrupts
;------------------------------------------------------------------------
I_HRDF EQU I_VEC+$60                ; Host Receive Data Full
I_HTDE EQU I_VEC+$62                ; Host Transmit Data Empty
I_HC EQU I_VEC+$64                  ; Default Host Command
;------------------------------------------------------------------------
; INTERRUPT ENDING ADDRESS
;------------------------------------------------------------------------
I_INTEND EQU I_VEC+$FF              ; last address of interrupt vector space
```