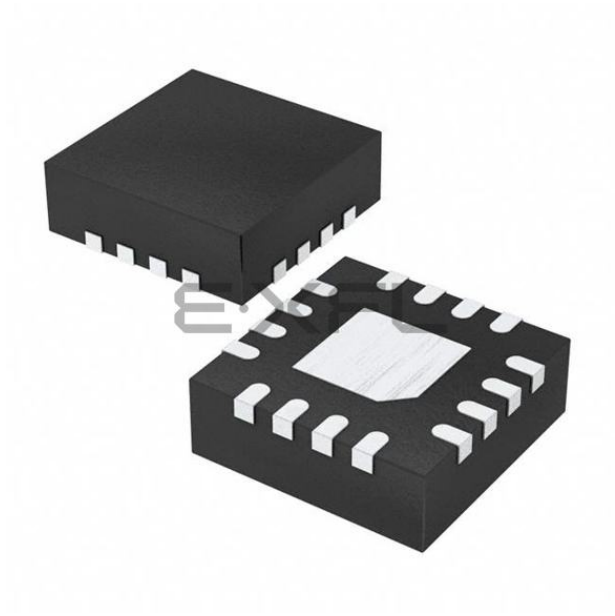

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Supplier Device Package	16-QFN (4x4)
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PIN ALLOCATION TABLES

TABLE 3: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1614)

I/O	14-Pin PDIP, SOIC, TSSOP	16-Pin UQFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	CLC	EUSART	SMT	Angular Timer	MSSP	PWM	High Current I/O	Interrupt	Pull-up	Basic
RA0	13	12	AN0	DAC1OUT1	C1IN+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	T0CKI(1)	—	CWG1IN(1)	ZCD1IN	—	—	—	—	—	—	—	INT IOC	Y	—
RA3	4	3	—	—	—	T6IN(1)	—	—	—	—	—	SMTWIN2(1)	—	—	—	—	IOC	Y	$\overline{MCLR}$/VPP
RA4	3	2	AN3	—	—	T1G(1)	—	—	—	—	—	SMTSIG1(1)	—	—	—	—	IOC	Y	CLKOUT
RA5	2	1	—	—	—	T1CKI(1) T2IN(1)	—	—	—	—	—	SMTWIN1(1)	—	—	—	—	IOC	Y	CLKIN
RC0	10	9	AN4	—	C2IN+	T5CKI(1)	—	—	—	—	—	—	—	SCK(1,3)	—	—	IOC	Y	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	T4IN(1)	—	—	—	—	—	SMTSIG2(1)	—	SDI(1)	—	—	IOC	Y	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	T5G(1)	CCP2(1)	—	—	CLCIN0(1)	—	—	ATCC1(1)	$\overline{SS}$(1)	—	—	IOC	Y	—
RC4	6	5	—	—	—	T3G(1)	—	—	—	CLCIN1(1)	CK(1)	—	ATCC2(1)	—	—	HIC4	IOC	Y	—
RC5	5	4	—	—	—	T3CKI(1)	CCP1(1)	—	—	—	RX(1,3)	—	ATIN(1) ATCC3(1)	—	—	HIC5	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	—	CCP1	CWG1A	ZCD1OUT	CLC1OUT	DT(3)	—	—	SDO	PWM3OUT	—	—	—	—
	—	—	—	—	C2OUT	—	CCP2	CWG1B	—	CLC2OUT	CK	—	—	SCK(3)	PWM4OUT	—	—	—	—
	—	—	—	—	—	—	—	CWG1C	—	—	TX	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	CWG1D	—	—	—	—	—	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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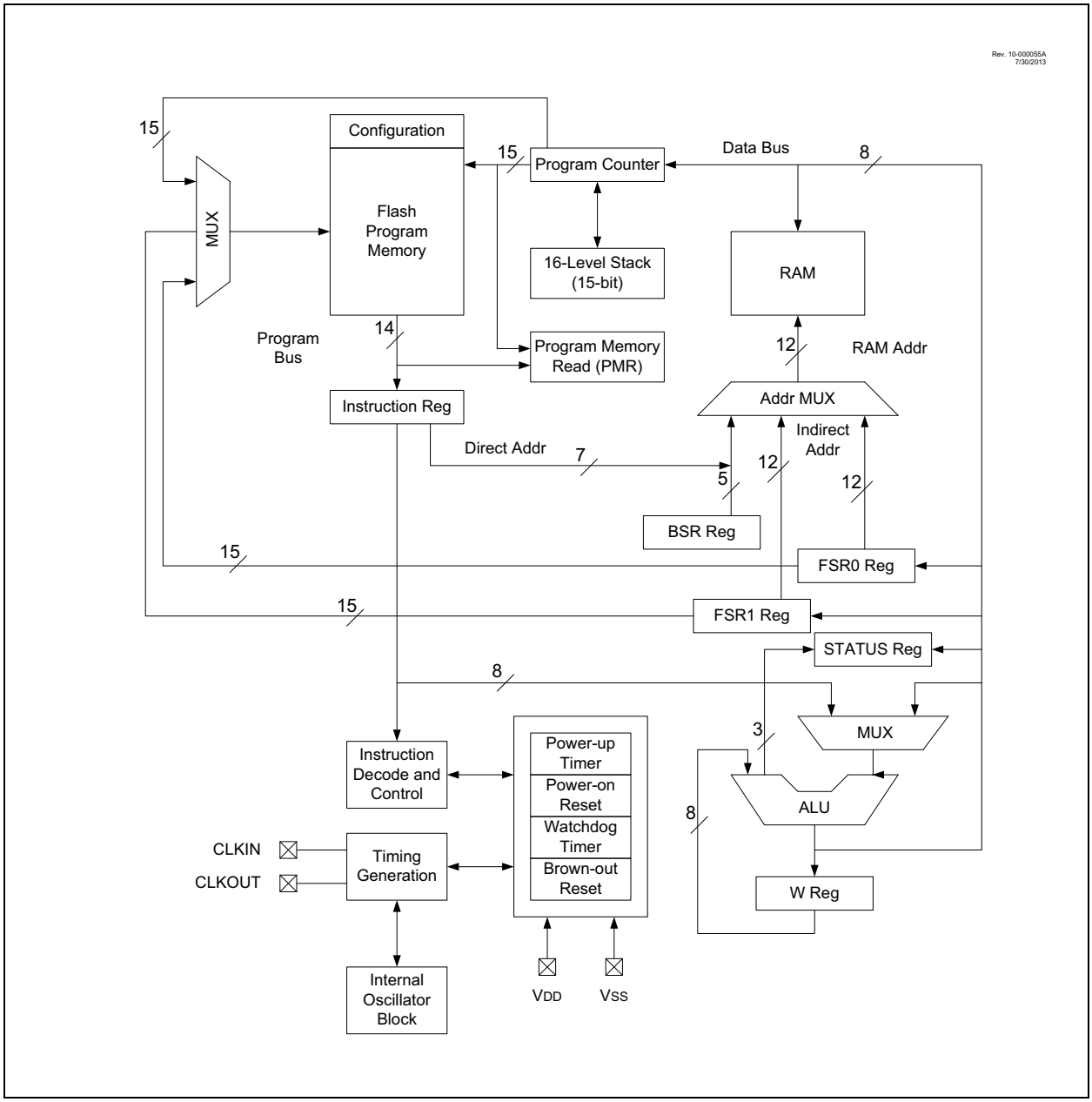
2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 34.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
- 1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
- 0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
- 1 = After power-up or by the `CLRWDT` instruction
- 0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
- 1 = The result of an arithmetic or logic operation is zero
- 0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
- 1 = A carry-out from the 4th low-order bit of the result occurred
- 0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
- 1 = A carry-out from the Most Significant bit of the result occurred
- 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

TABLE 3-2: PIC16(L)F1614 MEMORY MAP, BANK 0-7

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-1)	080h	Core Registers (Table 3-1)	100h	Core Registers (Table 3-1)	180h	Core Registers (Table 3-1)	200h	Core Registers (Table 3-1)	280h	Core Registers (Table 3-1)	300h	Core Registers (Table 3-1)	380h	Core Registers (Table 3-1)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	—	08Dh	—	10Dh	—	18Dh	—	20Dh	—	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PIR1	090h	PIE1	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR2	091h	PIE2	111h	CM1CON0	191h	PMADRL	211h	SSP1BUF	291h	CCP1RL	311h	—	391h	IOCAP
012h	PIR3	092h	PIE3	112h	CM1CON1	192h	PMADRH	212h	SSP1ADD	292h	CCP1RH	312h	—	392h	IOCAN
013h	PIR4	093h	PIE4	113h	CM2CON0	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	PIR5	094h	PIE5	114h	CM2CON1	194h	PMDATH	214h	SSP1STAT	294h	CCP1CAP	314h	—	394h	—
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	SSP1CON	295h	—	315h	—	395h	—
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSP1CON2	296h	—	316h	—	396h	—
017h	TMR1H	097h	—	117h	FVRCON	197h	VREGCON	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	—	218h	—	298h	CCP2RL	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RC1REG	219h	—	299h	CCP2RH	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TX1REG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	SP1BRGL	21Bh	—	29Bh	CCP2CAP	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	ZCD1CON	19Ch	SP1BRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	T2HLT	09Dh	ADCON0	11Dh	—	19Dh	RC1STA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	T2CLKCON	09Eh	ADCON1	11Eh	—	19Eh	TX1STA	21Eh	—	29Eh	CCPTMRS	31Eh	—	39Eh	—
01Fh	T2RST	09Fh	ADCON2	11Fh	—	19Fh	BAUD1CON	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 16 Bytes	3A0h	Unimplemented Read as '0'
												32Fh			
												330h	Unimplemented Read as '0'		
		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
		0F0h	Common RAM (Accesses 70h – 7Fh)	170h	Common RAM (Accesses 70h – 7Fh)	1F0h	Common RAM (Accesses 70h – 7Fh)	270h	Common RAM (Accesses 70h – 7Fh)	2F0h	Common RAM (Accesses 70h – 7Fh)	370h	Accesses 70h – 7Fh	3F0h	Common RAM (Accesses 70h – 7Fh)
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

4.6 Device ID and Revision ID

The 14-bit Device ID word is located at 8006h and the 14-bit Revision ID is located at 8005h. These locations are read-only and cannot be erased or modified. See **Section 10.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

4.7 Register Definitions: Device ID

REGISTER 4-4: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R
DEV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit		
'1' = Bit is set	'0' = Bit is cleared	

bit 13-0 **DEV<13:0>:** Device ID bits

Device	DEVID<13:0> Values
PIC16F1614	11 0000 0111 1000 (3078h)
PIC16LF1614	11 0000 0111 1010 (307Ah)
PIC16F1618	11 0000 0111 1001 (3079h)
PIC16LF1618	11 0000 0111 1011 (307Bh)

REGISTER 4-5: REVID: REVISION ID REGISTER

R	R	R	R	R	R
REV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
REV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit		
'1' = Bit is set	'0' = Bit is cleared	

bit 13-0 **REV<13:0>:** Revision ID bits

7.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIE1, PIE2 and PIE3 registers)

The INTCON, PIR1, PIR2 and PIR3 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See **"Section7.5 "Automatic Context Saving"."**)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

Note 1:	Individual interrupt flag bits are set, regardless of the state of any other enable bits.
2:	All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

7.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is three or four instruction cycles. For asynchronous interrupts, the latency is three to five instruction cycles, depending on when the interrupt occurs. See Figure 7-2 and Figure 7-3 for more details.

EXAMPLE 10-3: WRITING TO FLASH PROGRAM MEMORY (32 WRITE LATCHES)

```
; This write routine assumes the following:
; 1. 64 bytes of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
;    stored in little endian format
; 3. A valid starting address (the Least Significant bits = 00000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)
;
        BCF         INTCON,GIE     ; Disable ints so required sequences will execute properly
        BANKSEL     PMADRH         ; Bank 3
        MOVF        ADDRH,W        ; Load initial address
        MOVWF       PMADRH         ;
        MOVF        ADDRL,W        ;
        MOVWF       PMADRL         ;
        MOVLW       LOW DATA_ADDR  ; Load initial data address
        MOVWF       FSR0L          ;
        MOVLW       HIGH DATA_ADDR ; Load initial data address
        MOVWF       FSR0H          ;
        BCF         PMCON1,CFGS    ; Not configuration space
        BSF         PMCON1,WREN    ; Enable writes
        BSF         PMCON1,LWLO    ; Only Load Write Latches
LOOP
        MOVIW       FSR0++         ; Load first data byte into lower
        MOVWF       PMDATL         ;
        MOVIW       FSR0++         ; Load second data byte into upper
        MOVWF       PMDATH         ;

        MOVF        PMADRL,W       ; Check if lower bits of address are '00000'
        XORLW       0x1F           ; Check if we're on the last of 32 addresses
        ANDLW       0x1F           ;
        BTFSC       STATUS,Z       ; Exit if last of 32 words,
        GOTO        START_WRITE    ;

  Required Sequence
        MOVLW       55h            ; Start of required write sequence:
        MOVWF       PMCON2         ; Write 55h
        MOVLW       AAh            ;
        MOVWF       PMCON2         ; Write AAh
        BSF         PMCON1,WR      ; Set WR bit to begin write
        NOP                        ; NOP instructions are forced as processor
                                   ; loads program memory write latches
        NOP                        ;

        INCF        PMADRL,F       ; Still loading latches Increment address
        GOTO        LOOP           ; Write next latches

START_WRITE
        BCF         PMCON1,LWLO    ; No more loading latches - Actually start Flash program
                                   ; memory write

  Required Sequence
        MOVLW       55h            ; Start of required write sequence:
        MOVWF       PMCON2         ; Write 55h
        MOVLW       AAh            ;
        MOVWF       PMCON2         ; Write AAh
        BSF         PMCON1,WR      ; Set WR bit to begin write
        NOP                        ; NOP instructions are forced as processor writes
                                   ; all the program memory write latches simultaneously
        NOP                        ; to program memory.
                                   ; After NOPs, the processor
                                   ; stalls until the self-write process in complete
                                   ; after write processor continues with 3rd instruction
        BCF         PMCON1,WREN    ; Disable writes
        BSF         INTCON,GIE     ; Enable interrupts
```

REGISTER 12-23: SLRCONC: PORTC SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRC7(1)	SLRC6(1)	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRC<7:0>:** PORTC Slew Rate Enable bits(1)
For RC<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

Note 1: SLRC<7:6> on PIC16(L)F1618 only.

REGISTER 12-24: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
INLVLC7(1)	INLVLC6(1)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLC<7:0>:** PORTC Input Level Select bits(1)
For RC<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

Note 1: INLVLC<7:6> on PIC16(L)F1618 only.

14.0 INTERRUPT-ON-CHANGE

The PORTA, PORTB[(1)] and PORTC pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 14-1 is a block diagram of the IOC module.

Note 1: PORTB available on PIC16(L)F1618 only.

14.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

14.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

14.3 Interrupt Flags

The IOCAFx, IOCBFx and IOCCFx bits located in the IOCAF, IOCBF and IOCCF registers, respectively, are status flags that correspond to the interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx, IOCBFx and IOCCFx bits.

14.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx, IOCBFx and IOCCFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 14-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW   0xff
XORWF   IOCAF, W
ANDWF   IOCAF, F
```

14.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

TABLE 15-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)

Peripheral	Conditions	Description
HFINTOSC	FOSC<2:0> = 010 and IRCF<3:0> = 000x	INTOSC is active and device is not in Sleep.
BOR	BOREN<1:0> = 11	BOR always enabled.
	BOREN<1:0> = 10 and BORFS = 1	BOR disabled in Sleep mode, BOR Fast Start enabled.
	BOREN<1:0> = 01 and BORFS = 1	BOR under software control, BOR Fast Start enabled.
LDO	All PIC16F1614/8 devices, when VREGPM = 1 and not in Sleep	The device runs off of the Low-Power Regulator when in Sleep mode.

25.1.2.8 Asynchronous Reception Set-up

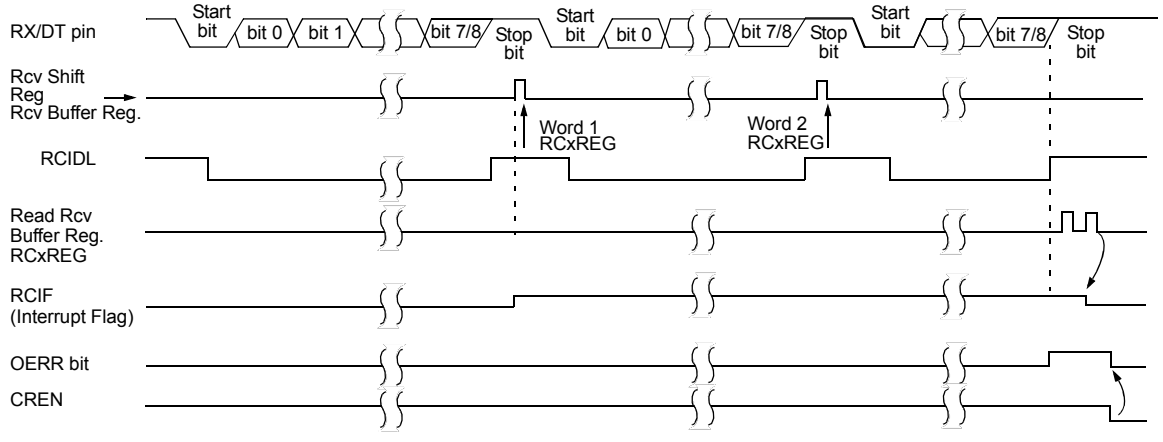
1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 25.4 "EUSART Baud Rate Generator (BRG)"**).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
8. Read the RCxSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

25.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 25.4 "EUSART Baud Rate Generator (BRG)"**).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. Enable 9-bit reception by setting the RX9 bit.
6. Enable address detection by setting the ADDEN bit.
7. Enable reception by setting the CREN bit.
8. The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
9. Read the RCxSTA register to get the error flags. The ninth data bit will always be set.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register. Software determines if this is the device's address.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

FIGURE 25-5: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCxREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

28.9 CWG Steering Mode

In Steering mode (MODE = 00x), the CWG allows any combination of the CWGxx pins to be the modulated signal. The same signal can be simultaneously available on multiple pins, or a fixed-value output can be presented.

When the respective STRx bit of CWGxOCON0 is '0', the corresponding pin is held at the level defined. When the respective STRx bit of CWGxOCON0 is '1', the pin is driven by the input data signal. The user can assign the input data signal to one, two, three, or all four output pins.

The POLx bits of the CWGxCON1 register control the signal polarity only when STRx = 1.

The CWG auto-shutdown operation also applies in Steering modes as described in **Section 28.10 "Auto-Shutdown"**. An auto-shutdown event will only affect pins that have STRx = 1.

28.9.1 STEERING SYNCHRONIZATION

Changing the MODE bits allows for two modes of steering, synchronous and asynchronous.

When MODE = 000, the steering event is asynchronous and will happen at the end of the instruction that writes to STRx (that is, immediately). In this case, the output signal at the output pin may be an incomplete waveform. This can be useful for immediately removing a signal from the pin.

When MODE = 001, the steering update is synchronous and occurs at the beginning of the next rising edge of the input data signal. In this case, steering the output on/off will always produce a complete waveform.

Figure 28-10 and Figure 28-11 illustrate the timing of asynchronous and synchronous steering, respectively.

FIGURE 28-10: EXAMPLE OF STEERING EVENT AT END OF INSTRUCTION (MODE<2:0> = 000)

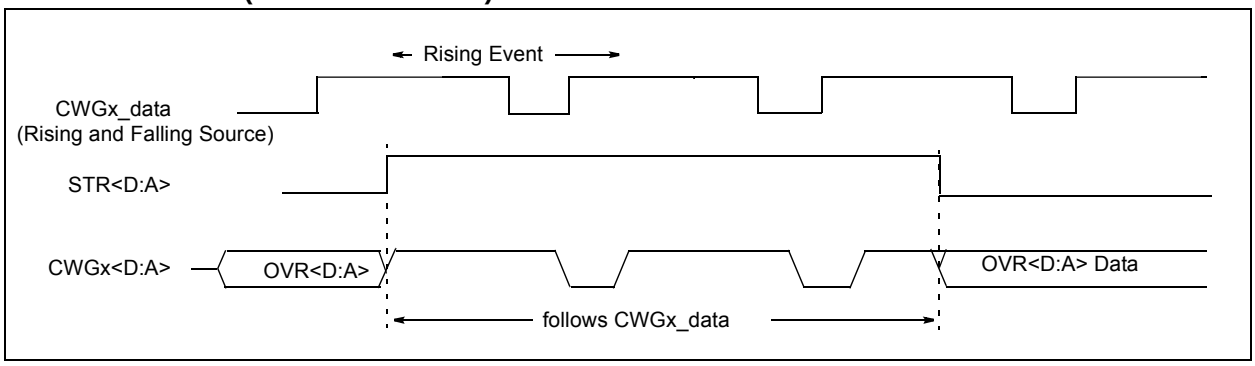
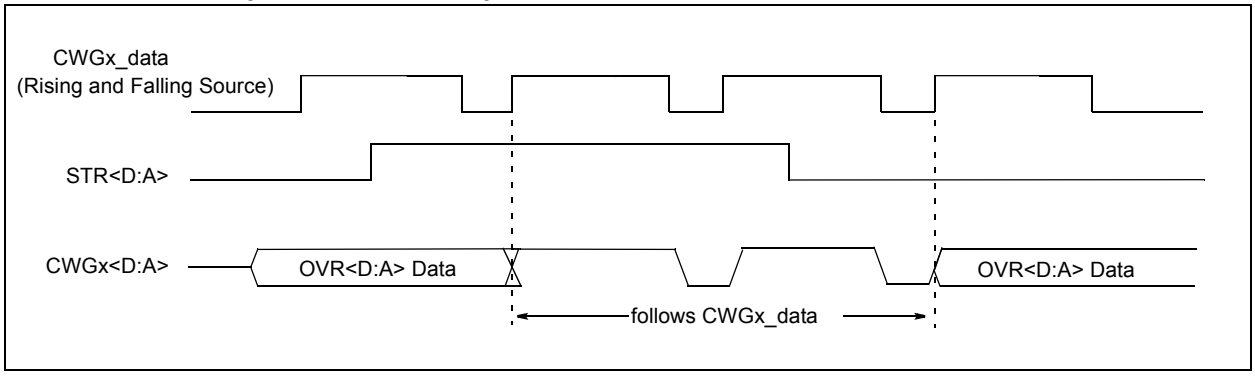


FIGURE 28-11: EXAMPLE OF STEERING EVENT AT BEGINNING OF INSTRUCTION (MODE<2:0> = 001)



REGISTER 28-2: CWGxCON1: CWGx CONTROL REGISTER 1

U-0	U-0	R-x	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IN	—	POLD	POLC	POLB	POLA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **IN:** CWG Input Value

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **POLD:** CWGxD Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 2 **POLC:** CWGxC Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 1 **POLB:** CWGxB Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 0 **POLA:** CWGxA Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

REGISTER 28-3: CWGxDBR: CWGx RISING DEAD-BAND COUNTER REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	DBR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DBR<5:0>:** Rising Event Dead-Band Value for Counter bits

REGISTER 28-4: CWGxDBF: CWGx FALLING DEAD-BAND COUNTER REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	DBF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DBF<5:0>:** Falling Event Dead-Band Value for Counter bits

REGISTER 30-9: SMTxTMRL: SMT TIMER REGISTER – LOW BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SMTxTMR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxTMR<7:0>**: Significant bits of the SMT Counter – Low Byte

REGISTER 30-10: SMTxTMRH: SMT TIMER REGISTER – HIGH BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SMTxTMR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxTMR<15:8>**: Significant bits of the SMT Counter – High Byte

REGISTER 30-11: SMTxTMRU: SMT TIMER REGISTER – UPPER BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SMTxTMR<23:16>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxTMR<23:16>**: Significant bits of the SMT Counter – Upper Byte

TABLE 30-3: SUMMARY OF REGISTERS ASSOCIATED WITH SMTx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PIE4	SCANIE	CRCIE	SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE	101
PIR4	SCANIF	CRCIF	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF	106
SMT1CLK	—	—	—	—	—	CSEL<2:0>			438
SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		435
SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				436
SMT1CPRH	SMT1CPR<15:8>								444
SMT1CPRL	SMT1CPR<7:0>								444
SMT1CPRU	SMT1CPR<23:16>								444
SMT1CPWH	SMT1CPW<15:8>								445
SMT1CPWL	SMT1CPW<7:0>								445
SMT1CPWU	SMT1CPW<23:16>								445
SMT1PRH	SMT1PR<15:8>								446
SMT1PRL	SMT1PR<7:0>								446
SMT1PRU	SMT1PR<23:16>								446
SMT1SIG	—	—	—	SSEL<4:0>					441
SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	437
SMT1TMRH	SMT1TMR<15:8>								443
SMT1TMRL	SMT1TMR<7:0>								443
SMT1TMRU	SMT1TMR<23:16>								443
SMT1WIN	—	—	—	WSEL<4:0>					439
SMT2CLK	—	—	—	—	—	CSEL<2:0>			438
SMT2CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT2PS<1:0>		435
SMT2CON1	SMT2GO	REPEAT	—	—	MODE<3:0>				436
SMT2CPRH	SMT2CPR<15:8>								444
SMT2CPRL	SMT2CPR<7:0>								444
SMT2CPRU	SMT2CPR<23:16>								444
SMT2CPWH	SMT2CPW<15:8>								445
SMT2CPWL	SMT2CPW<7:0>								445
SMT2CPWU	SMT2CPW<23:16>								445
SMT2PRH	SMT2PR<15:8>								446
SMT2PRL	SMT2PR<7:0>								446
SMT2PRU	SMT2PR<23:16>								446
SMT2SIG	—	—	—	—	—	SSEL<2:0>			441
SMT2STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	437
SMT2TMRH	SMT2TMR<15:8>								443
SMT2TMRL	SMT2TMR<7:0>								443
SMT2TMRU	SMT2TMR<23:16>								443
SMT2WIN	—	—	—	WSEL<4:0>					438

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for SMTx module.

31.7 Interrupts

The angular timer and its capture/compare features can generate multiple interrupt conditions. To accommodate all of these interrupt sources, the module is provided with its own interrupt logic structure, similar to that of the micro controller. Angular timer interrupts are enabled by the ATxIE0 register (Register 31-13) and their respective flags are located in the ATxIR0 register (Register 31-14). The capture/compare interrupts are enabled by the ATxIE1 register (Register 31-15) with flags in the ATxIR1 register (Register 31-16). All sources are funneled into a single Angular Timer Interrupt Flag bit, ATxIF of the PIR5 register (Register 7-11). This means that upon a triggered interrupt, the ATxIR0 and ATxIR1 register bits will indicate the source of the triggered interrupt. It also means that in order for specific interrupts to generate a microcontroller interrupt, both the ATxIE bit of the PIE register and the desired enable bit in either ATxIE0 or ATxIE1 must be set.

Note:	Due to the nature of the angular timer interrupts, the ATxIF flag bit of the PIR5 register is read-only.

31.7.1 ANGULAR TIMER PERIOD INTERRUPT

This interrupt is triggered when the AT module detects a period event. In Single-Pulse mode, a period event occurs on every input signal edge. In Multi-Pulse mode, a period event occurs on the input signal edge following a missed pulse. The period interrupt generation matches with the pulses on the period clock output of the timer. It is enabled by the ATPERIE bit of the ATxIE0 register and the status is indicated by the PERIF bit of the ATxIR0 register.

31.7.2 ANGULAR TIMER PHASE CLOCK INTERRUPT

This interrupt is triggered on each pulse of the phase clock output of the timer. It is enabled by the ATPHIE bit of the ATxIE0 register and the status is indicated by the PHSIF bit of the ATxIR0 register.

31.7.3 ANGULAR TIMER MISSING PULSE INTERRUPT

This interrupt is triggered upon the output of a missing pulse detection signal. Refer to **Section 31.2.3 “Missing Pulse Detection”** for more information. This interrupt is enabled by the ATMISSIE bit of the ATxIE0 register and its status is indicated by the ATMISSIF bit of the ATxIR0 register.

31.7.4 ANGULAR TIMER CAPTURE/COMPARE INTERRUPTS

Capture and compare interrupts are triggered by the capture/compare functions of the module. If configured for Capture mode, the interrupt will trigger after the capture signal has successfully latched the value of the phase counter into the capture registers. If configured for Compare mode, the interrupt will trigger when a match is detected between the value placed in the compare register and the value of the phase counter. These interrupts are controlled by the CC1IE, CC2IE, and CC3IE bits of the ATxIE1 register, respectively, and are similarly indicated by the CC1IF, CC2IF, and CC3IF bits of the ATxIR1 register.

Note: Unless otherwise noted, VIN = 5V, FOSC = 500 kHz, CIN = 0.1 µF, TA = 25°C.

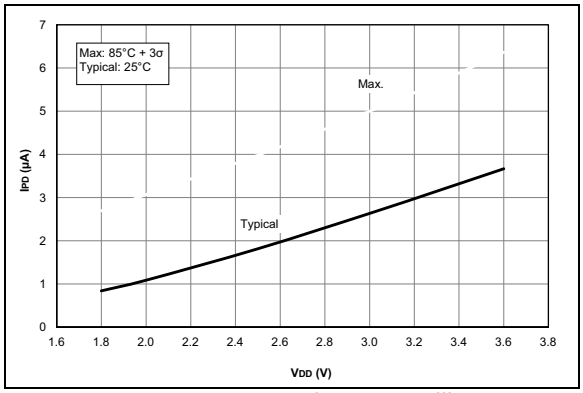


FIGURE 36-31: *IPD, Timer1 Oscillator, FOSC = 32 kHz, PIC16LF1614/8 Only.*

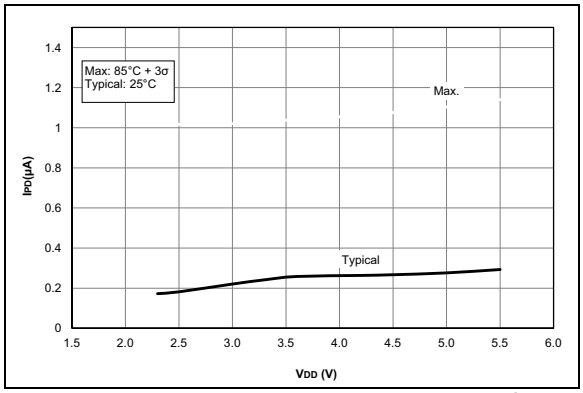


FIGURE 36-34: *IPD, ADC Non-Converting, PIC16F1614/8 Only.*

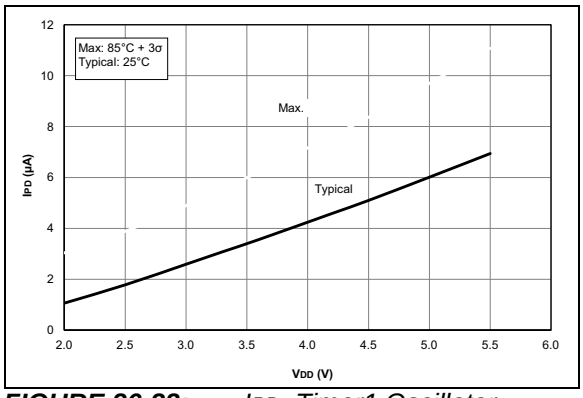


FIGURE 36-32: *IPD, Timer1 Oscillator, FOSC = 32 kHz, PIC16F1614/8 Only.*

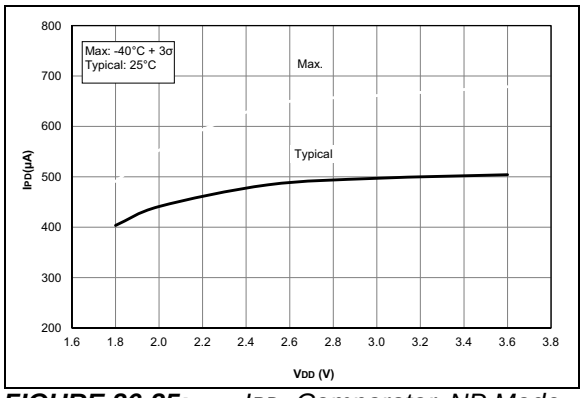


FIGURE 36-35: *IPD, Comparator, NP Mode (CxSP = 1), PIC16LF1614/8 Only.*

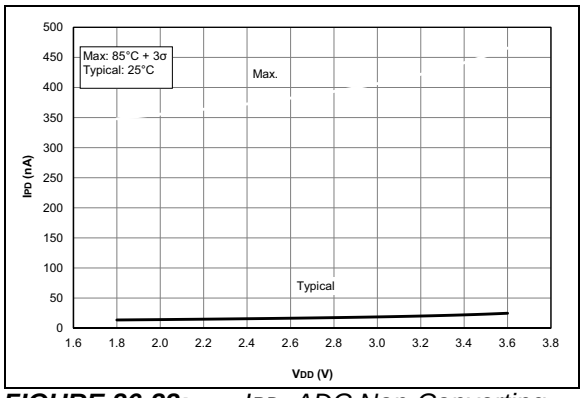


FIGURE 36-33: *IPD, ADC Non-Converting, PIC16LF1614/8 Only.*

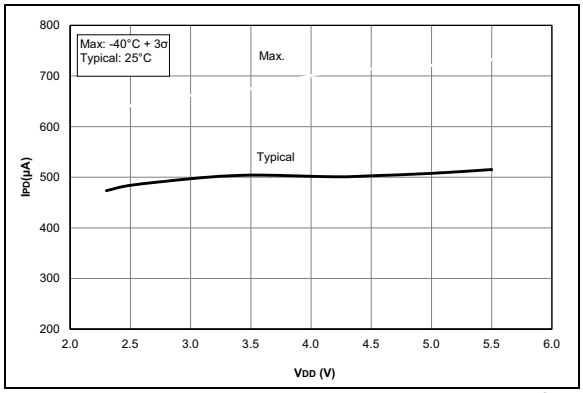
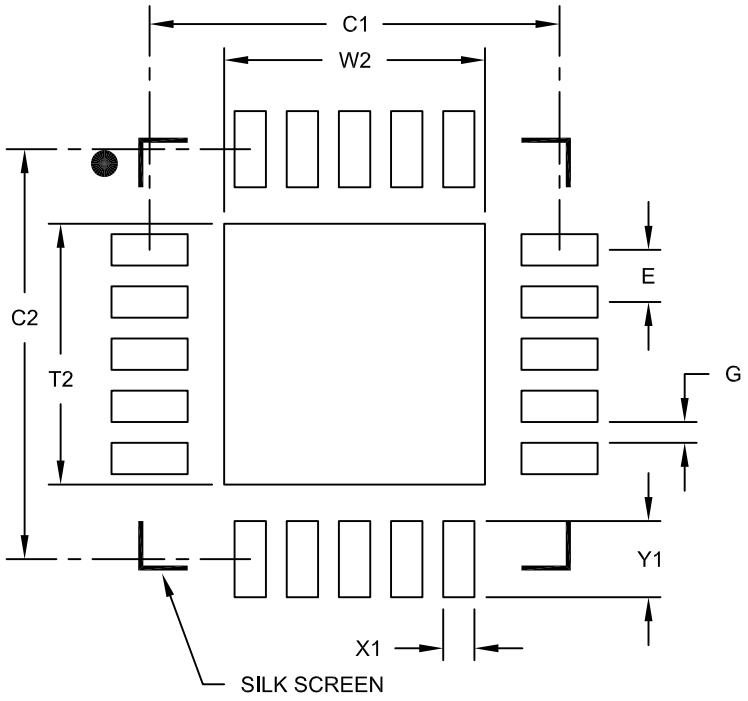


FIGURE 36-36: *IPD, Comparator, NP Mode (CxSP = 1), PIC16F1614/8 Only.*

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A