What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1618-e-so

3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The `MOVIW` instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The `HIGH` operator will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
  DW DATA0             ;First constant
  DW DATA1             ;Second constant
  DW DATA2
  DW DATA3
my_function
  ;… LOTS OF CODE…
  MOVLW   DATA_INDEX
  ADDLW   LOW constants
  MOVWF   FSR1L
  MOVLW   HIGH constants;MSb sets
                        automatically
  MOVWF   FSR1H
  BTFSC   STATUS, C    ;carry from ADDLW?
  INCF    FSR1h, f     ;yes
  MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

TABLE 3-14: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Banks 29											
E8Ch to E8Fh	—	Unimplemented								—	—
E90h	RA0PPS	—	—	—	RA0PPS<4:0>					`---0 0000`	`---0 0000`
E91h	RA1PPS	—	—	—	RA1PPS<4:0>					`---0 0000`	`---0 0000`
E92h	RA2PPS	—	—	—	RA2PPS<4:0>					`---0 0000`	`---0 0000`
E93h	—	Unimplemented								—	—
E94h	RA4PPS	—	—	—	RA4PPS<4:0>					`---0 0000`	`---0 0000`
E95h	RA5PPS	—	—	—	RA5PPS<4:0>					`---0 0000`	`---0 0000`
E96h to E9Bh	—	Unimplemented								—	—
E9Ch	RB4PPS(4)	—	—	—	RB4PPS<4:0>					`---0 0000`	`---0 0000`
E9Dh	RB5PPS(4)	—	—	—	RB5PPS<4:0>					`---0 0000`	`---0 0000`
E9Eh	RB6PPS(4)	—	—	—	RB6PPS<4:0>					`---0 0000`	`---0 0000`
E9Fh	RB7PPS(4)	—	—	—	RB7PPS<4:0>					`---0 0000`	`---0 0000`
EA0h	RC0PPS	—	—	—	RC0PPS<4:0>					`---0 0000`	`---0 0000`
EA1h	RC1PPS	—	—	—	RC1PPS<4:0>					`---0 0000`	`---0 0000`
EA2h	RC2PPS	—	—	—	RC2PPS<4:0>					`---0 0000`	`---0 0000`
EA3h	RC3PPS	—	—	—	RC3PPS<4:0>					`---0 0000`	`---0 0000`
EA4h	RC4PPS	—	—	—	RC4PPS<4:0>					`---0 0000`	`---0 0000`
EA5h	RC5PPS	—	—	—	RC5PPS<4:0>					`---0 0000`	`---0 0000`
EA6h	RC6PPS(4)	—	—	—	RC6PPS<4:0>					`---0 0000`	`---0 0000`
EA7h	RC7PPS(4)	—	—	—	RC7PPS<4:0>					`---0 0000`	`---0 0000`
EA8h to EEFh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: PIC16F1614/8 only.

2: Unimplemented, read as '1'.

3: PIC16(L)F1614 only.

4: PIC16(L)F1618 only.

TABLE 3-14: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 31											
F8Ch — FE3h	—	Unimplemented								—	—
FE4h	STATUS_SHAD	—	—	—	—	—	Z_SHAD	DC_SHAD	C_SHAD	`---- -xxx`	`---- -uuu`
FE5h	WREG_SHAD	Working Register Shadow								`xxxx xxxx`	`uuuu uuuu`
FE6h	BSR_SHAD	—	—	—	Bank Select Register Shadow					`---x xxxx`	`---u uuuu`
FE7h	PCLATH_SHAD	—	Program Counter Latch High Register Shadow							`-xxx xxxx`	`uuuu uuuu`
FE8h	FSR0L_SHAD	Indirect Data Memory Address 0 Low Pointer Shadow								`xxxx xxxx`	`uuuu uuuu`
FE9h	FSR0H_SHAD	Indirect Data Memory Address 0 High Pointer Shadow								`xxxx xxxx`	`uuuu uuuu`
FEAh	FSR1L_SHAD	Indirect Data Memory Address 1 Low Pointer Shadow								`xxxx xxxx`	`uuuu uuuu`
FEBh	FSR1H_SHAD	Indirect Data Memory Address 1 High Pointer Shadow								`xxxx xxxx`	`uuuu uuuu`
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack Pointer					`---1 1111`	`---1 1111`
FEEh	TOSL	Top-of-Stack Low byte								`xxxx xxxx`	`uuuu uuuu`
FEFh	TOSH	—	Top-of-Stack High byte							`-xxx xxxx`	`-uuu uuuu`

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as ‘0’.

Note 1: PIC16F1614/8 only.

2: Unimplemented, read as ‘1’.

3: PIC16(L)F1614 only.

4: PIC16(L)F1618 only.

REGISTER 4-3: CONFIG3: CONFIGURATION WORD 3

R/P-0	R/P-0	R/P-1	R/P-1	R/P-1	R/P-1
WDTCCS<2:0>			WDTCWS<2:0>		
bit 13					bit 8

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	WDTE<1:0>		WDTCPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	-n = Value when blank or after Bulk Erase

bit 13-11 **WDTCCS<2:0>:** WDT Configuration Clock Select bits

111 =Software Control; WDT clock selected by CS<2:0>
110 =Reserved
•
•
•
010 =Reserved
001 =WDT reference clock is MFINTOSC, 31.25 kHz (default value)
000 =WDT reference clock is LFINTOSC, 31.00 kHz output

bit 10-8 **WDTCWS<2:0>:** WDT Configuration Window Select bits.

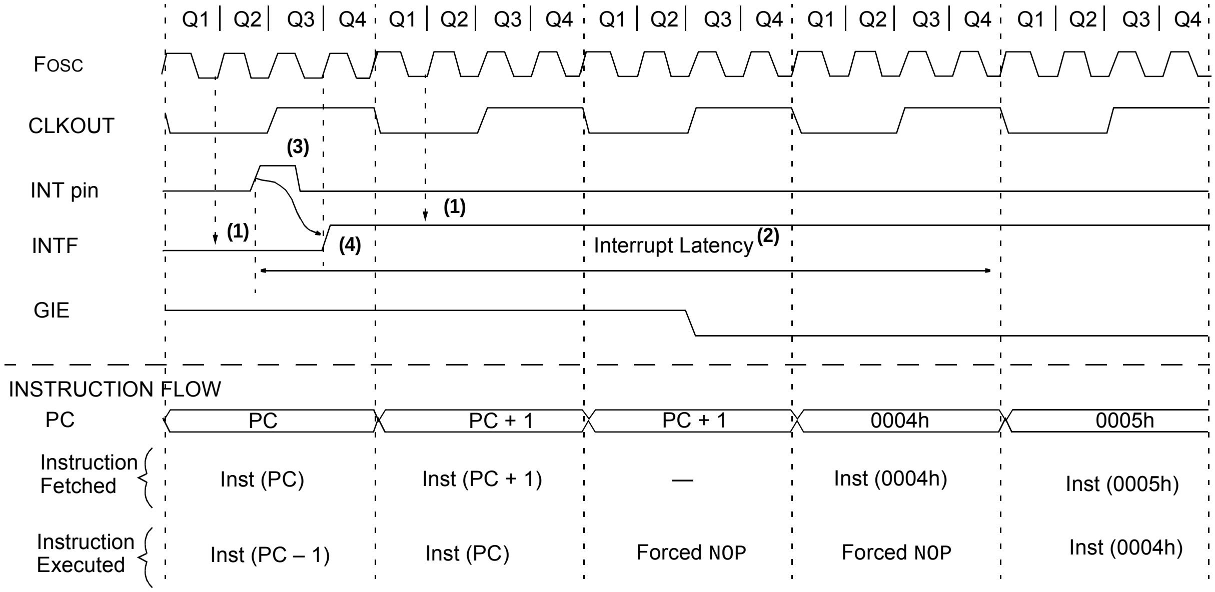
WDTCWS <2:0>	WINDOW at POR			Software control of WINDOW?	Keyed access required?	
	Value	Window delay Percent of time	Window opening Percent of time			
111	111	n/a	100	Yes	No	Default fuse = 111
110	111	n/a	100	No	Yes	
101	101	25	75			
100	100	37.5	62.5			
011	011	50	50			
010	010	62.5	37.5			
001	001	75	25			
000	000	87.5	12.5[1]			

bit 7 **Unimplemented:** Read as ‘1’

bit 6-5 **WDTE<1:0>:** Watchdog Timer Enable bits

11 =WDT enabled in all modes, the SEN bit in the WDTCON0 register is ignored
10 =WDT enabled while running and disabled in Sleep
01 =WDT controlled by the SEN bit in the WDTCON0 register
00 = WDT disabled

FIGURE 7-3: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: For minimum width of INT pulse, refer to AC specifications in **Section35.0 “Electrical Specifications”**.

4: INTF is enabled to be set any time during the Q4-Q1 cycles.

10.0 FLASH PROGRAM MEMORY CONTROL

The Flash program memory is readable and writable during normal operation over the full VDD range. Program memory is indirectly addressed using Special Function Registers (SFRs). The SFRs used to access program memory are:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When accessing the program memory, the PMDATH:PMDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the PMADRH:PMADRL register pair forms a 2-byte word that holds the 15-bit address of the program memory location being read.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

The Flash program memory can be protected in two ways; by code protection ($\overline{\text{CP}}$ bit in Configuration Words) and write protection (WRT<1:0> bits in Configuration Words).

Code protection ($\overline{\text{CP}}$ = `0`)**(1)**, disables access, reading and writing, to the Flash program memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a Bulk Erase to the device, clearing all Flash program memory, Configuration bits and User IDs.

Write protection prohibits self-write and erase to a portion or all of the Flash program memory, as defined by the bits WRT<1:0>. Write protection does not affect a device programmers ability to read, write or erase the device.

Note 1: Code protection of the entire Flash program memory array is enabled by clearing the $\overline{\text{CP}}$ bit of Configuration Words.

10.1 PMADRL and PMADRH Registers

The PMADRH:PMADRL register pair can address up to a maximum of 16K words of program memory. When selecting a program address value, the MSB of the address is written to the PMADRH register and the LSB is written to the PMADRL register.

10.1.1 PMCON1 AND PMCON2 REGISTERS

PMCON1 is the control register for Flash program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared by hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

The PMCON2 register is a write-only register. Attempting to read the PMCON2 register will return all ‘`0`’s.

To enable writes to the program memory, a specific pattern (the unlock sequence), must be written to the PMCON2 register. The required unlock sequence prevents inadvertent writes to the program memory write latches and Flash program memory.

10.2 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum size that can be erased by user software.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the PMDATH:PMDATL register pair.

Note: If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, new data and retained data can be written into the write latches to reprogram the row of Flash program memory. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations.

See Table 10-1 for Erase Row size and the number of write latches for Flash program memory.

TABLE 10-1: FLASH MEMORY ORGANIZATION BY DEVICE

Device	Row Erase (words)	Write Latches (words)
PIC16(L)F1614	32	32
PIC16(L)F1618		

REGISTER 12-7: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	SLRA5	SLRA4	—	SLRA2	SLRA1	SLRA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **SLRA<5:4>:** PORTA Slew Rate Enable bits
For RA<5:4> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SLRA<2:0>:** PORTA Slew Rate Enable bits
For RA<2:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-8: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **INLVLA<5:0>:** PORTA Input Level Select bits
For RA<5:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

REGISTER 12-13: WPUB: WEAK PULL-UP PORTB REGISTER(1),(2)

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **WPUB<7:4>**: Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

bit 3-0 **Unimplemented:** Read as ‘0’

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 12-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

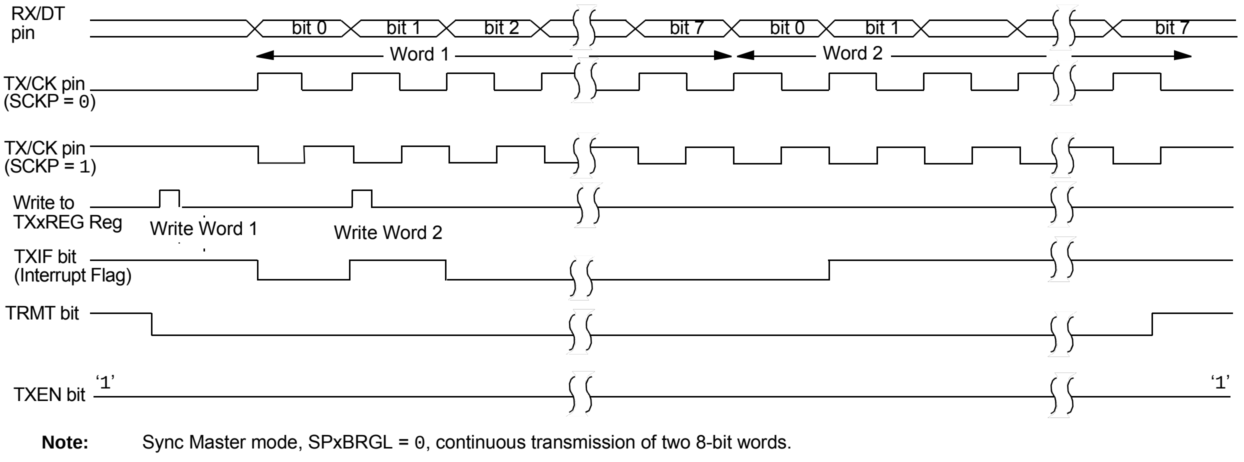
R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
ODB7	ODB6	ODB5	ODB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **ODB<7:4>**: PORTB Open-Drain Enable bits
For RB<7:4> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

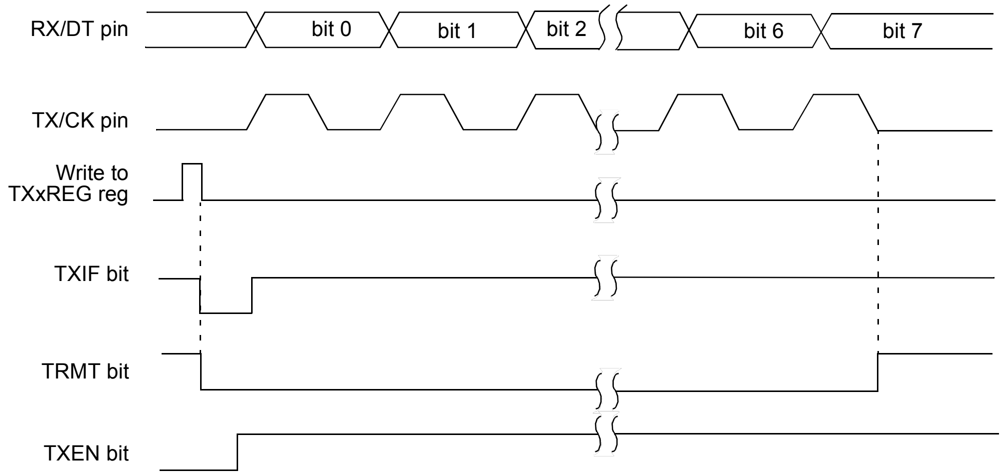
bit 3-0 **Unimplemented:** Read as ‘0’

FIGURE 25-10: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPxBRGL = 0, continuous transmission of two 8-bit words.

FIGURE 25-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



REGISTER 26-2: CCPTMRS: PWM TIMER SELECTION CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
P4TSEL<1:0>		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **P4TSEL<1:0>:** PWM4 Timer Selection bits

11 = Reserved
10 = PWM4 is based off Timer6 in PWM mode
01 = PWM4 is based off Timer4 in PWM mode
00 = PWM4 is based off Timer2 in PWM mode

bit 5-4 **P3TSEL<1:0>:** PWM3 Timer Selection bits

11 = Reserved
10 = PWM3 is based off Timer6 in PWM mode
01 = PWM3 is based off Timer4 in PWM mode
00 = PWM3 is based off Timer2 in PWM mode

bit 3-2 **C2TSEL<1:0>:** CCP2 (PWM2) Timer Selection bits

11 = Reserved
10 = CCP2 is based off Timer6 in PWM mode
01 = CCP2 is based off Timer4 in PWM mode
00 = CCP2 is based off Timer2 in PWM mode

bit 1-0 **C1TSEL<1:0>:** CCP1 (PWM1) Timer Selection bits

11 = Reserved
10 = CCP1 is based off Timer6 in PWM mode
01 = CCP1 is based off Timer4 in PWM mode
00 = CCP1 is based off Timer2 in PWM mode

REGISTER 28-2: CWGxCON1: CWGx CONTROL REGISTER 1

U-0	U-0	R-x	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IN	—	POLD	POLC	POLB	POLA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **IN:** CWG Input Value

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **POLD:** CWGxD Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 2 **POLC:** CWGxC Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 1 **POLB:** CWGxB Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 0 **POLA:** CWGxA Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

REGISTER 28-7: CWGxOCON0: CWGx STEERING CONTROL REGISTER[1]

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OVRD	OVRC	OVRB	OVRA	STRD[2]	STRC[2]	STRB[2]	STRA[2]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **OVRD:** Steering Data D bit

bit 6 **OVRC:** Steering Data C bit

bit 5 **OVRB:** Steering Data B bit

bit 4 **OVRA:** Steering Data A bit

bit 3 **STRD:** Steering Enable D bit[2]
1 = CWGxD output has the CWGx_data waveform with polarity control from POLD bit
0 = CWGxD output is assigned the value of OVRD bit

bit 2 **STRC:** Steering Enable C bit[2]
1 = CWGxC output has the CWGx_data waveform with polarity control from POLC bit
0 = CWGxC output is assigned the value of OVRC bit

bit 1 **STRB:** Steering Enable B bit[2]
1 = CWGxB output has the CWGx_data waveform with polarity control from POLB bit
0 = CWGxB output is assigned the value of OVRB bit

bit 0 **STRA:** Steering Enable A bit[2]
1 = CWGxA output has the CWGx_data waveform with polarity control from POLA bit
0 = CWGxA output is assigned the value of OVRA bit

Note 1: The bits in this register apply only when MODE<2:0> = 00x.

2: This bit is effectively double-buffered when MODE<2:0> = 001.

31.2.5 VALID BIT

Several values used by the AT module must be calculated from external signals. As such, these values may be inaccurate for a period of time after the angular timer starts up. Because of this, the module will not output signals or trigger interrupts for a period of time after the module is enabled, or under certain other conditions that might jeopardize accurate output values. This output inhibition is indicated by the read-only VALID bit of the ATxCON1 being clear.

The following cases will clear the VALID bit in hardware:

- Any write to ATxRES register pair
- Phase counter overflow (ATxPHS register pair) clocked beyond 0x3FF)
- In-Circuit Debugger halt
- EN = 0
- ATxPER register pair = 0
- Device Reset

As long as the VALID bit is cleared, the following occurs:

- Period clock is not output and associated interrupts do not trigger.
- Missed pulse is not output and associated interrupts do not trigger.
- Phase clock is not output and associated interrupts do not trigger.
- Phase counter does not increment.
- Capture logic does not function and associated interrupts do not trigger.
- Compare logic does not function and associated interrupts do not trigger.
- Every ATxsig edge latches the period counter into the ATxPER register pair, regardless of mode.

In single-pulse modes, the VALID bit becomes set upon the 3rd active input edge of the signal that latches the ATxPER register pair. In multi-pulse modes, a missing pulse trigger is also required, ensuring that at least one full revolution of the input has occurred.

An example of the VALID bit in Single-Pulse mode is shown in Figure 31-6.

31.2.6 DETERMINING ACCURACY

The ATxRES register pair determines the resolution of the period measurement and, by extension, the maximum value that the phase counter reaches at the end of each input signal period. The interim value, ATxPER, used to derive the phase counter is, by nature of the circuitry, an integer. The ratio of the integer value obtained by the circuit and the calculated floating point value is the inherent error of the measurement. When ATxRES is small then integer rounding results in large errors. Factors that contribute to large errors include:

- Large values for ATxRES
- Relatively low ATxclk frequency
- Relatively high ATxsig input frequency

The actual error can be determined with Equation 31-7.

EQUATION 31-7:

$$period = \frac{F(ATxclk)}{F(ATxsig) \bullet (ATxRES + 1)}$$

$$error\% = 100 \bullet \left(\frac{period - int(period + 1)}{period}\right)$$

31.3 Input and Clock Selection

The input clock for the AT module can come from either the FOSC system clock or the 16 MHz HFINTOSC, and is chosen by the CS0 bit of the ATxCLK register. In addition, the clock is run through a prescaler that can be /1, /2, /4, or /8, which is configured by the PS<1:0> bits of the ATxCON0 register. This prescaled clock is then used for all clock operations of the Angular Timer, and as such, should be used for all of the equations demonstrated above determining the Angular Timer's behavior.

The input signal for the AT module can come from a variety of sources. The source is selected by the SSEL bits of the ATxSIG register (Register 31-4).

31.4 Module Outputs

31.4.1 ANGLE/PHASE CLOCK OUTPUT

The angle/phase clock signal (ATx_phsclk) can be used by the CLC as an input signal to combinational logic. The polarity of this signal is configured by the PHP bit of the ATxCON1 register.

31.4.2 PERIOD CLOCK OUTPUT

The period clock signal (ATx_perclk) can be used as an input clock for the Timer2/4/6 and Signal Measurement module, as well as an input signal to the CLC for combinational logic. The polarity of this signal is configured by the PRP bit of the ATxCON1 register (Register 31-2).

31.4.3 MISSED PULSE OUTPUT

The missed pulse signal (ATx_missedpulse) can be used by the CLC as an input signal to combinational logic. The polarity of this signal is configured by the MPP bit of the ATxCON1 register.

REGISTER 31-7: ATxMISSH: ANGULAR TIMER MISSING PULSE DELAY HIGH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MISS<15:8>[(1)]							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-0 **MISS<15:8>[(1)]:** Most Significant bits (2’s complement) of ATxMISS. ATxMISS defines the period counter value at which the missing pulse output becomes valid, based on the difference between the current counter value and the latched-in value of ATxPER.

Note 1: ATxMISSH is held until ATxMISSL is written. Proper writes of ATxMISS should write to ATxMISSH first, then ATxMISSL to ensure the value is properly written.

REGISTER 31-8: ATxMISSL: ANGULAR TIMER MISSING PULSE DELAY LOW REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MISS<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-0 **MISS<7:0>:** Least Significant bits (2’s complement) of ATxMISS. ATxMISS defines the period counter value at which the missing pulse output becomes valid, based on the difference between the current counter value and the latched-in value of ATxPER.

REGISTER 31-19: ATxERRH: ANGULAR TIMER SET POINT ERROR VALUE HIGH REGISTER

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
ERR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-0 **ERR<15:8>:** Most Significant bits of ATxERR. ATxERR is the error of the measured period value compared to the threshold setting, defined as ATxPER-ATxSTPTP.

REGISTER 31-20: ATxERRL: ANGULAR TIMER SET POINT ERROR VALUE LOW REGISTER

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
ERR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-0 **ERR<7:0>:** Least Significant bits of ATxERR. ATxERR is the error of the measured period value compared to the threshold setting, defined as ATxPER-ATxSTPTP.

XORLW	**Exclusive OR literal with W**
Syntax:	[*label*] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF	**Exclusive OR W with f**
Syntax:	[*label*] XORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) → (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

Note: Unless otherwise noted, VIN = 5V, FOSC = 500 kHz, CIN = 0.1 μF, TA = 25°C.

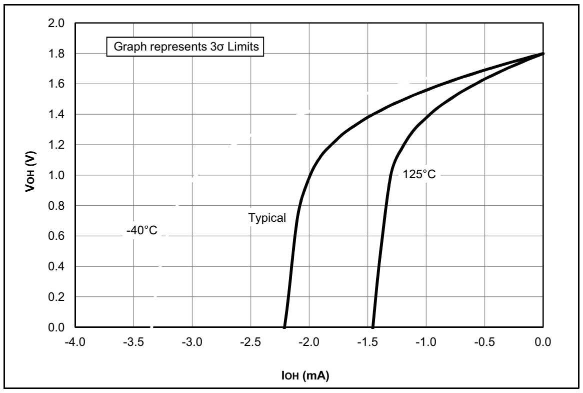


FIGURE 36-43: *VOH vs. IOH Over Temperature, VDD = 1.8V, PIC16LF1614/8 Only.*

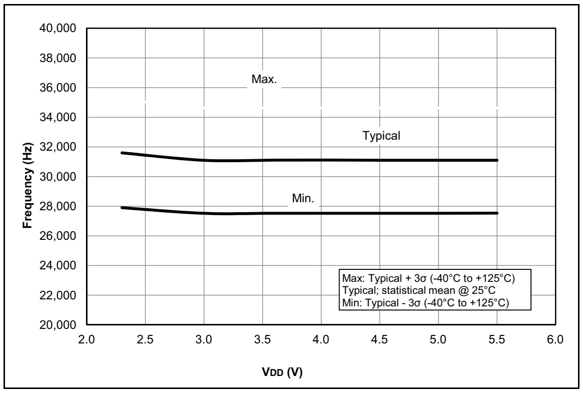


FIGURE 36-46: *LFINTOSC Frequency, PIC16F1614/8 Only.*

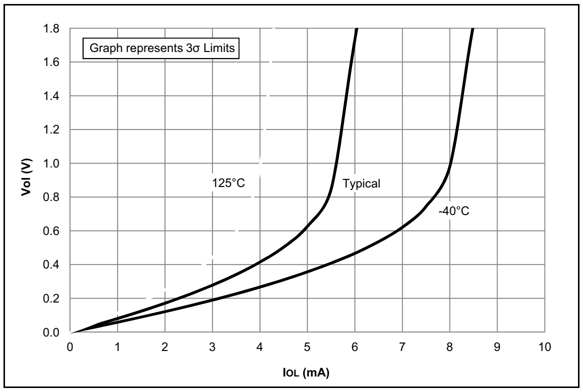


FIGURE 36-44: *VOL vs. IOL Over Temperature, VDD = 1.8V, PIC16LF1614/8 Only.*

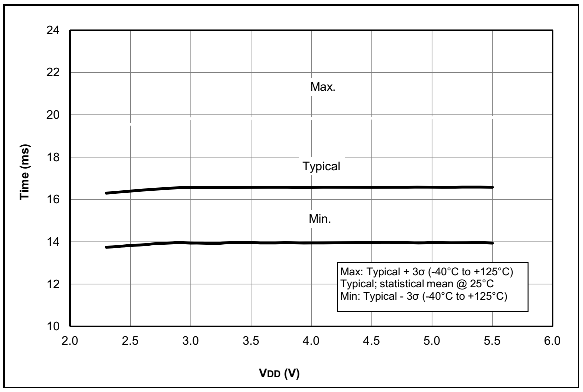


FIGURE 36-47: *WDT Time-Out Period, PIC16F1614/8 Only.*

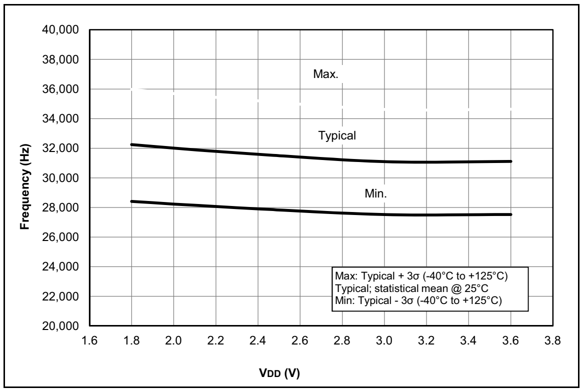


FIGURE 36-45: *LFINTOSC Frequency, PIC16LF1614/8 Only.*

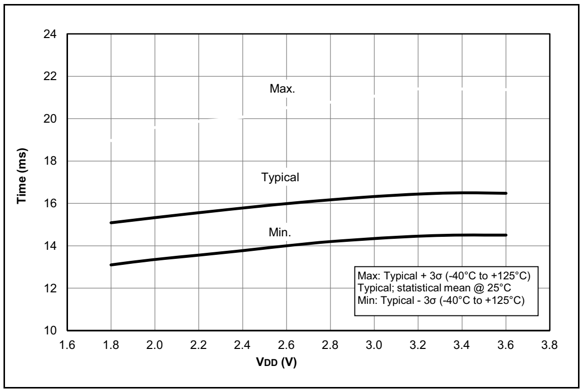


FIGURE 36-48: *WDT Time-Out Period, PIC16LF1614/8 Only.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 500 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

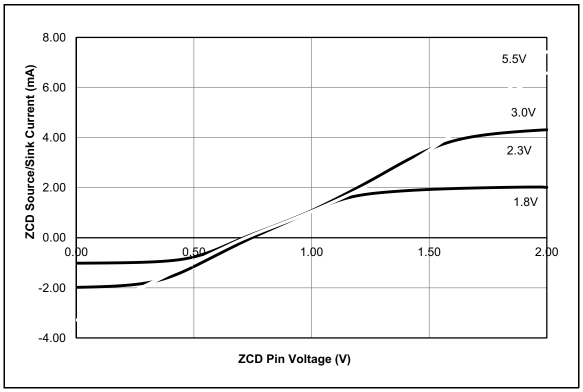


FIGURE 36-103: *ZCD Pin Current over ZCD Pin Voltage, Typical Measured Values from -40°C to 125°C.*

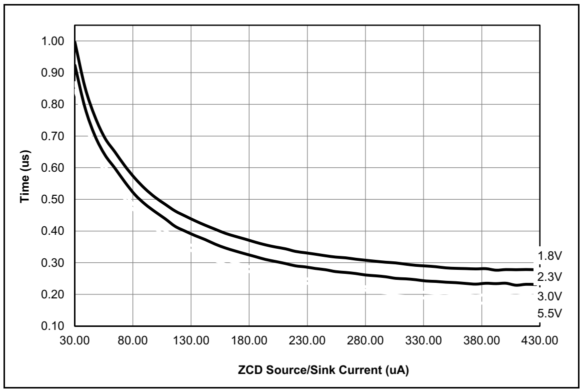
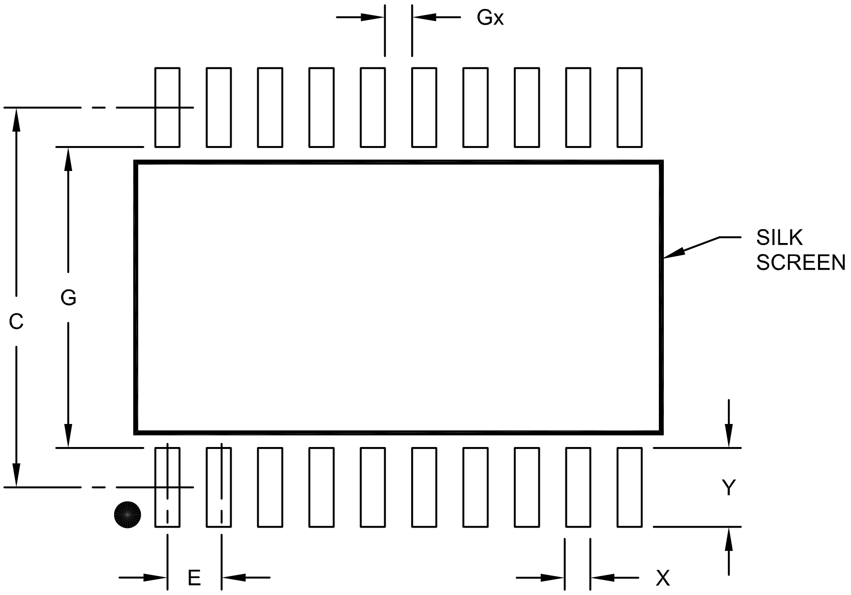


FIGURE 36-104: *ZCD Pin Response Timer over Current, Typical Measured Values from -40°C to 125°C.*

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X20)	X			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

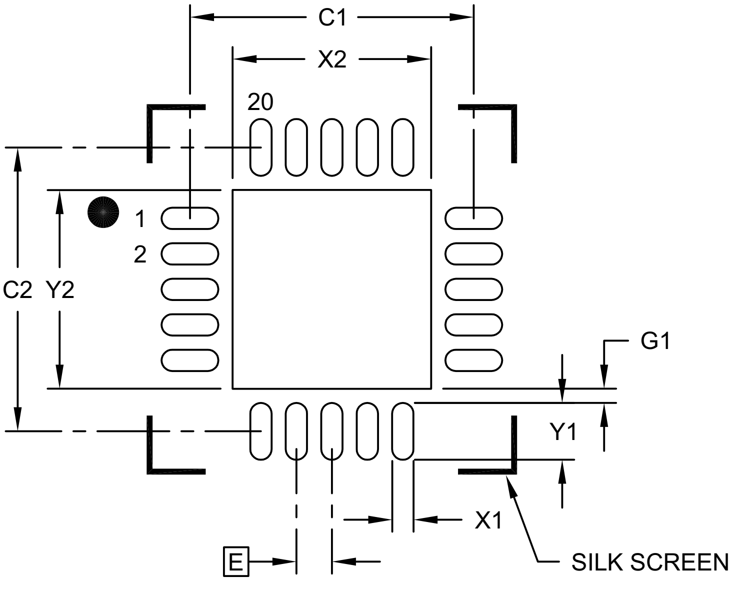
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2255A