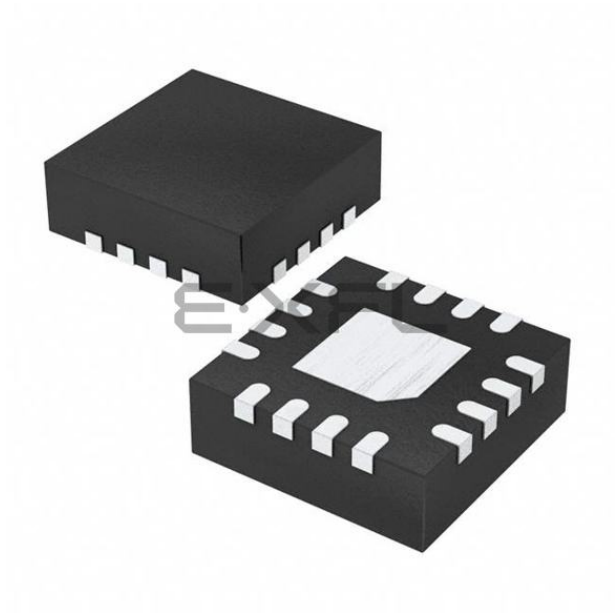

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1614t-i-ml

20-pin QFN, UQFN

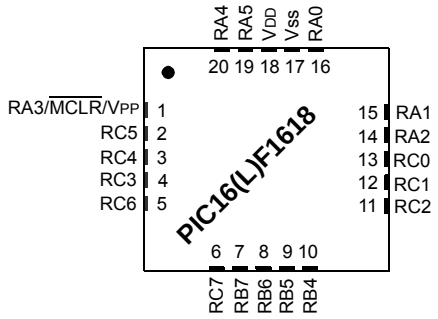


TABLE 1-3: PIC16(L)F1618 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB6/SCK(1, 3)	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	SCK	ST	CMOS	SPI clock.
RB7/CK(1)	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	CK	ST	CMOS	USART synchronous clock.
RC0/AN4/C2IN+/T5CKI(1)	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	AN4	AN	—	ADC Channel input.
	C2IN+	AN	—	Comparator positive input.
	T5CKI	TTL/ST	—	Timer5 clock input.
RC1/AN5/C1IN1-/C2IN1-/ T4IN(1)/CLCIN(2)/SMTSIG2(1)	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	AN5	AN	—	ADC Channel input.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
	T4IN	TTL/ST	—	Timer4 input.
	CLCIN2	ST	—	Configurable Logic Cell source input.
	SMTSIG2	TTL/ST	—	SMT2 signal input.
RC2/AN6/C1IN2-/C2IN2-	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	AN6	AN	—	ADC Channel input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
RC3/AN7/C1IN3-/C2IN3-/T5G(1)/ CCP2(1)/CLCIN0(1)/ATCC(1)	RC3	TTL/ST	—	General purpose input with IOC and WPU.
	AN7	AN	—	ADC Channel input.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.
	T5G	ST	—	Timer5 Gate input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	CLCIN0	ST	—	Configurable Logic Cell source input.
	ATCC	ST	—	Angular Timer Capture/Compare input.
RC4/T3G(1)/CLCIN1(1)/HIC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	T3G	ST	—	Timer3 Gate input.
	CLCIN1	ST	—	Configurable Logic Cell source input.
	HIC4	TTL	CMOS	High Current I/O.
RC5/T3CKI(1)/CCP2(1)/ATIN(1)/ HIC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	T3CKI	TTL/ST	—	Timer3 clock input.
	CCP2	TTL/ST	CMOS/OD	Capture/Compare/PWM2.
	ATIN	TTL/ST	—	Angular Timer clock input.
	HIC5	TTL	CMOS	High Current I/O.

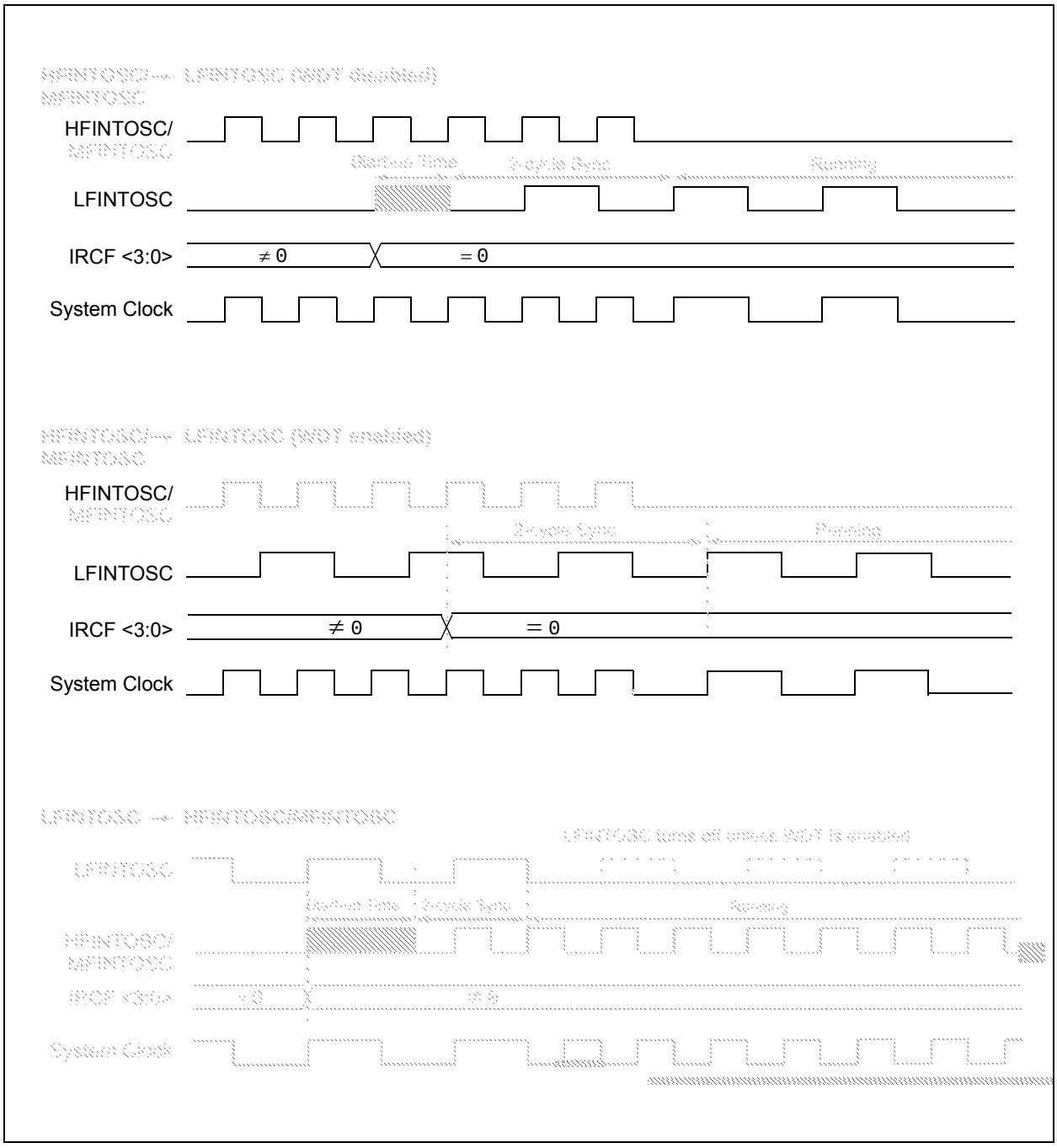
Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels; HV = High Voltage; XTAL = Crystal

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-1.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

FIGURE 5-3: INTERNAL OSCILLATOR SWITCH TIMING



6.1 Power-On Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

6.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms time-out on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTE bit in Configuration Words.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

6.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 6-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Words.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 6-2 for more information.

TABLE 6-1: BOR OPERATING MODES

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Instruction Execution upon: Release of POR or Wake-up from Sleep
11	X	X	Active	Waits for BOR ready(1) (BORRDY = 1)
10	X	Awake	Active	Waits for BOR ready (BORRDY = 1)
		Sleep	Disabled	
01	1	X	Active	Waits for BOR ready(1) (BORRDY = 1)
	0	X	Disabled	Begins immediately (BORRDY = x)
00	X	X	Disabled	

Note 1: In these specific cases, "release of POR" and "wake-up from Sleep," there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

6.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

6.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Words are programmed to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

6.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

REGISTER 7-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SCANIE	CRCIE	SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **SCANIE**: Scanner Interrupt Enable bit
1 = Enables the scanner interrupt
0 = Disables the scanner interrupt

bit 6 **CRCIE**: CRC Interrupt Enable bit
1 = Enables the CRC interrupt
0 = Disables the CRC interrupt

bit 5 **SMT2PWAIE**: SMT2 Pulse Width Acquisition Interrupt Enable bit
1 = Enables the SMT2 acquisition interrupt
0 = Disables the SMT2 acquisition interrupt

bit 4 **SMT2PRAIE**: SMT2 Period Acquisition Interrupt Enable bit
1 = Enables the SMT2 acquisition interrupt
0 = Disables the SMT2 acquisition interrupt

bit 3 **SMT2IE**: SMT2 Match Interrupt Enable bit
1 = Enables the SMT2 period match interrupt
0 = Disables the SMT2 period match interrupt

bit 2 **SMT1PWAIE**: SMT1 Pulse Width Acquisition Interrupt Enable bit
1 = Enables the SMT1 acquisition interrupt
0 = Disables the SMT1 acquisition interrupt

bit 1 **SMT1PRAIE**: SMT1 Period Acquisition Interrupt Enable bit
1 = Enables the SMT1 acquisition interrupt
0 = Disables the SMT1 acquisition interrupt

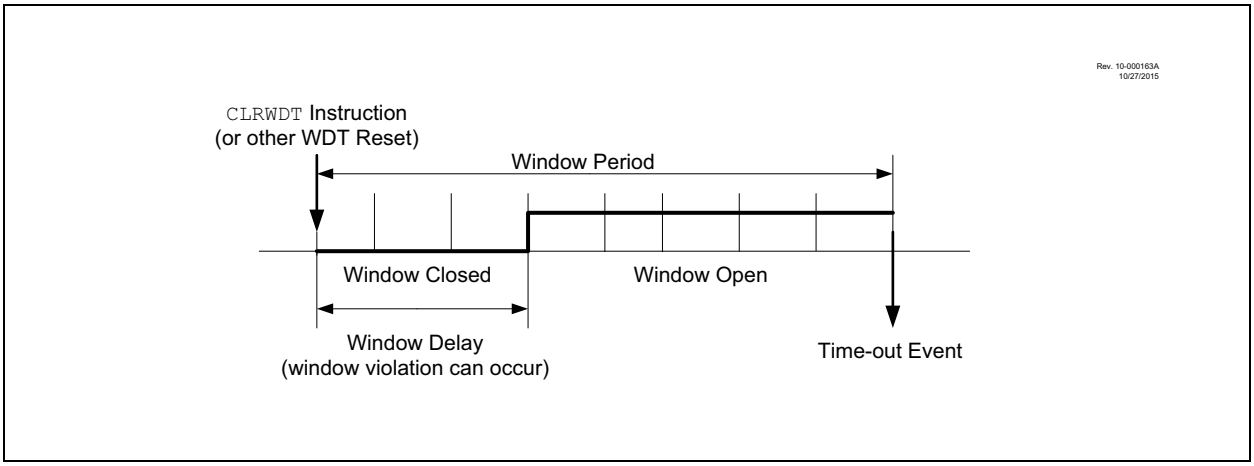
bit 0 **SMT1IE**: SMT1 Match Interrupt Enable bit
1 = Enables the SMT1 period match interrupt
0 = Disables the SMT1 period match interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

TABLE 9-2: WDT CLEARING CONDITIONS

Conditions	WDT
WDTE<1:0> = 00	Cleared
WDTE<1:0> = 01 and SEN = 0	
WDTE<1:0> = 10 and enter Sleep	
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Change INTOSC divider (IRCF bits)	Unaffected

FIGURE 9-2: WINDOW PERIOD AND DELAY



REGISTER 9-3: WDTPSL: WDT PRESCALE SELECT LOW BYTE REGISTER (READ ONLY)

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
PSCNT<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PSCNT<7:0>**: Prescale Select Low Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 9-4: WDTPSH: WDT PRESCALE SELECT HIGH BYTE REGISTER (READ ONLY)

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
PSCNT<15:8>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PSCNT<15:8>**: Prescale Select High Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 9-5: WDTTMR: WDT TIMER REGISTER (READ ONLY)

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
WDTTMR<3:0>					STATE	PSCNT<17:16>(1)	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-3 **WDTTMR<4:0>**: Watchdog Timer Value

bit 2 **STATE**: WDT Armed Status bit
1 = WDT is armed
0 = WDT is not armed

bit 1-0 **PSCNT<17:16>**: Prescale Select Upper Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

21.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 3-bit prescaler (independent of Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow
- TMR0 can be used to gate Timer1

Figure 21-1 is a block diagram of the Timer0 module.

21.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

21.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-bit Timer mode is selected by clearing the TMR0CS bit of the OPTION_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

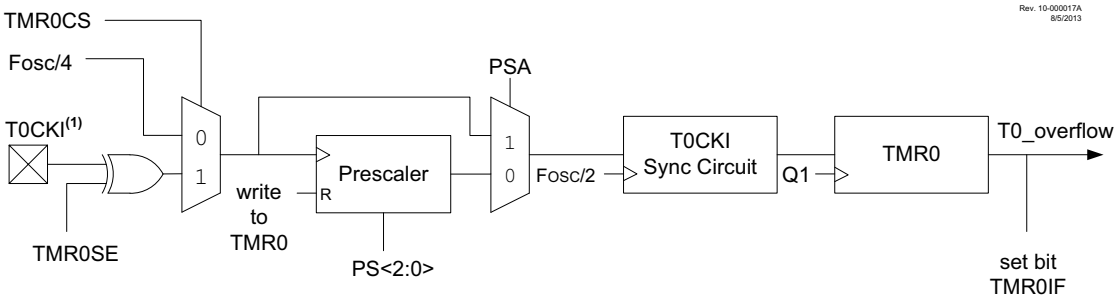
21.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin.

8-Bit Counter mode using the T0CKI pin is selected by setting the TMR0CS bit in the OPTION_REG register to '1'.

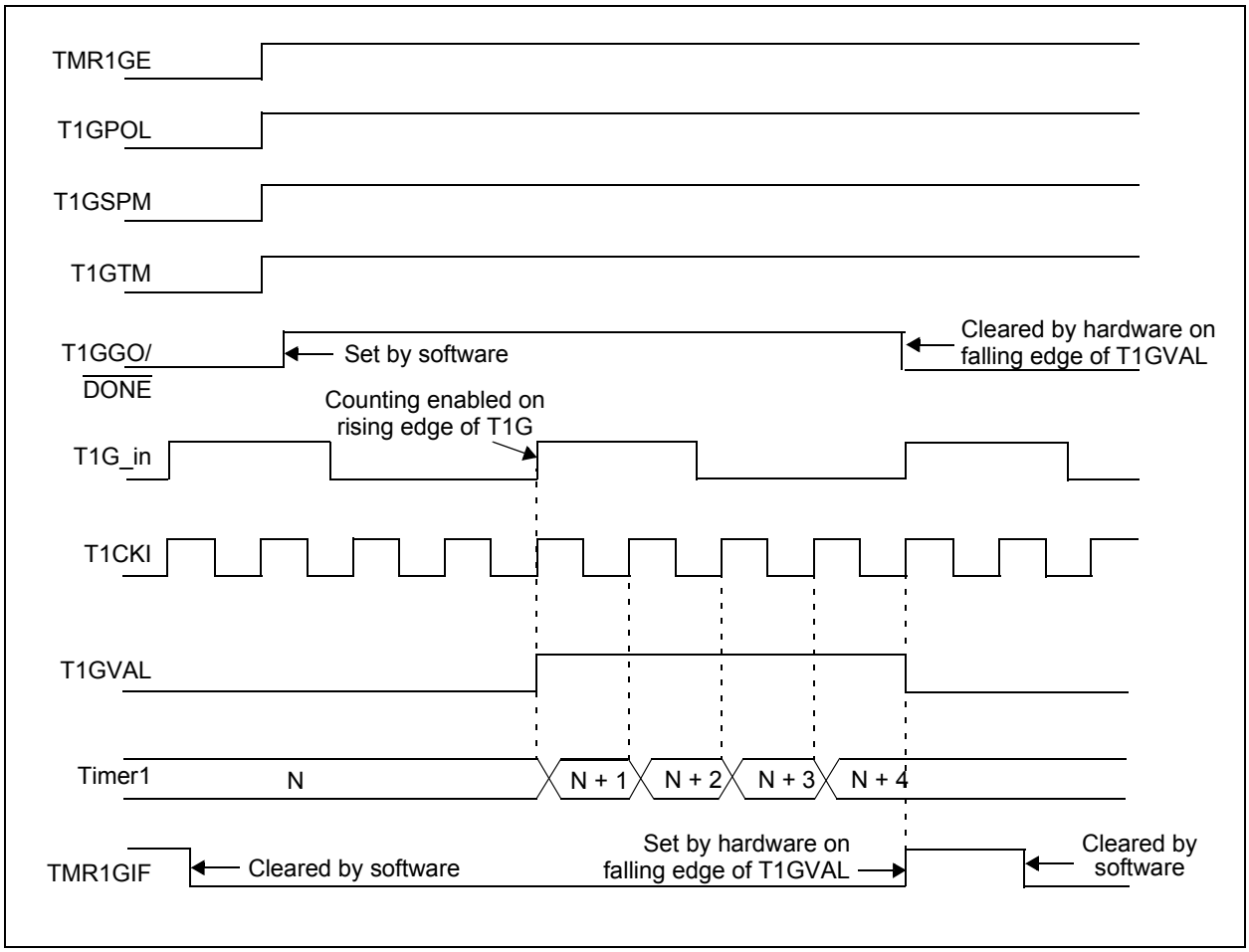
The rising or falling transition of the incrementing edge for either input source is determined by the TMR0SE bit in the OPTION_REG register.

FIGURE 21-1: TIMER0 BLOCK DIAGRAM



Note 1: The T0CKI prescale output frequency should not exceed FOSC/8.

FIGURE 22-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



22.8 Register Definitions: Timer1 Control

REGISTER 22-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	U-0	R/W-0/u	U-0	R/W-0/u
TMR1CS<1:0>		T1CKPS<1:0>		—	$\overline{\text{T1SYNC}}$	—	TMR1ON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **TMR1CS<1:0>:** Timer1 Clock Source Select bits
- 11 =LFINTOSC
- 10 =T1CKI
- 01 =FOSC
- 00 =FOSC/4

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
- 11 =1:8 Prescale value
- 10 =1:4 Prescale value
- 01 =1:2 Prescale value
- 00 =1:1 Prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 Synchronization Control bit
- 1 = Do not synchronize asynchronous clock input
- 0 = Synchronize asynchronous clock input with system clock (FOSC)

bit 1 **Unimplemented:** Read as '0'

bit 0 **TMR1ON:** Timer1 On bit
- 1 = Enables Timer1
- 0 = Stops Timer1 and clears Timer1 gate flip-flop

24.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

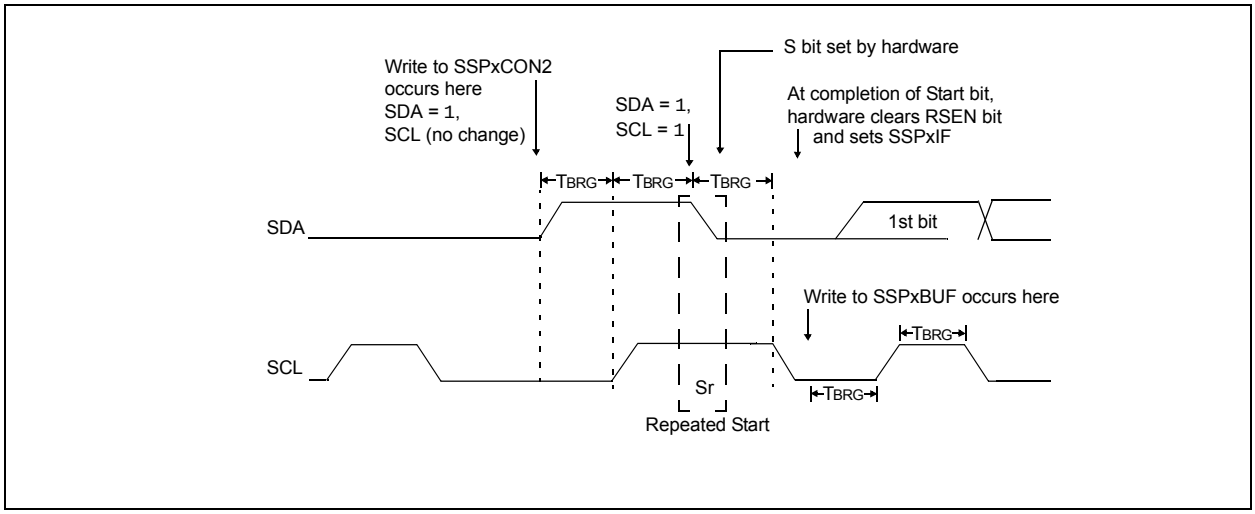
A Repeated Start condition (Figure 24-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 24-27: REPEATED START CONDITION WAVEFORM



24.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out (Case 1).

b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high (Case 2).

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to zero. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 24-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 24-39).

FIGURE 24-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

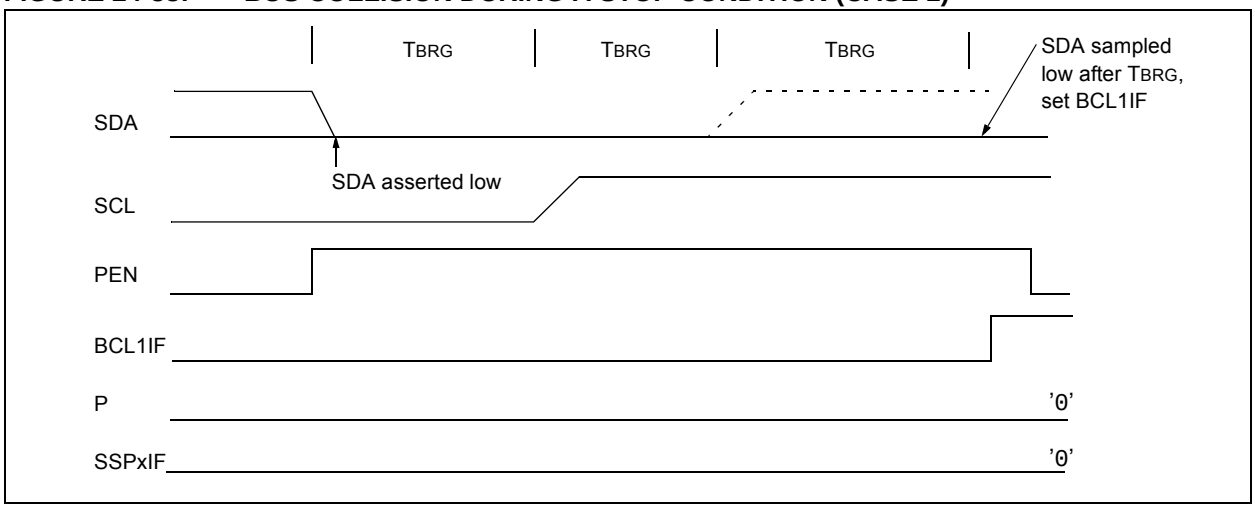
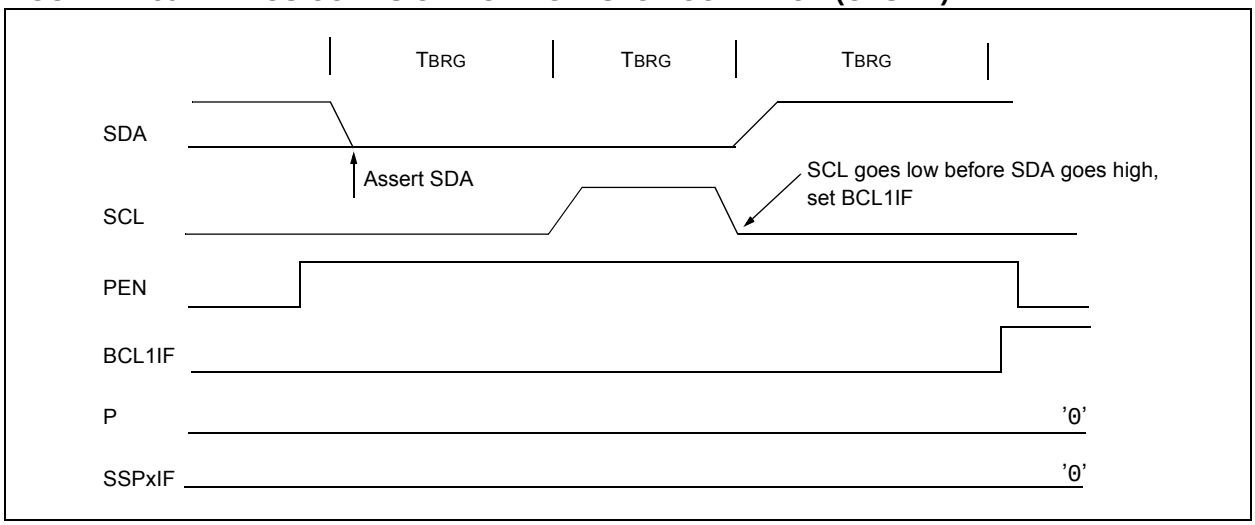


FIGURE 24-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



28.1.2 PUSH-PULL MODE

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 28-2. This alternation creates the push-pull effect required for driving some transformer-based power supply designs.

The push-pull sequencer is reset whenever EN = 0 or if an auto-shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWGxA.

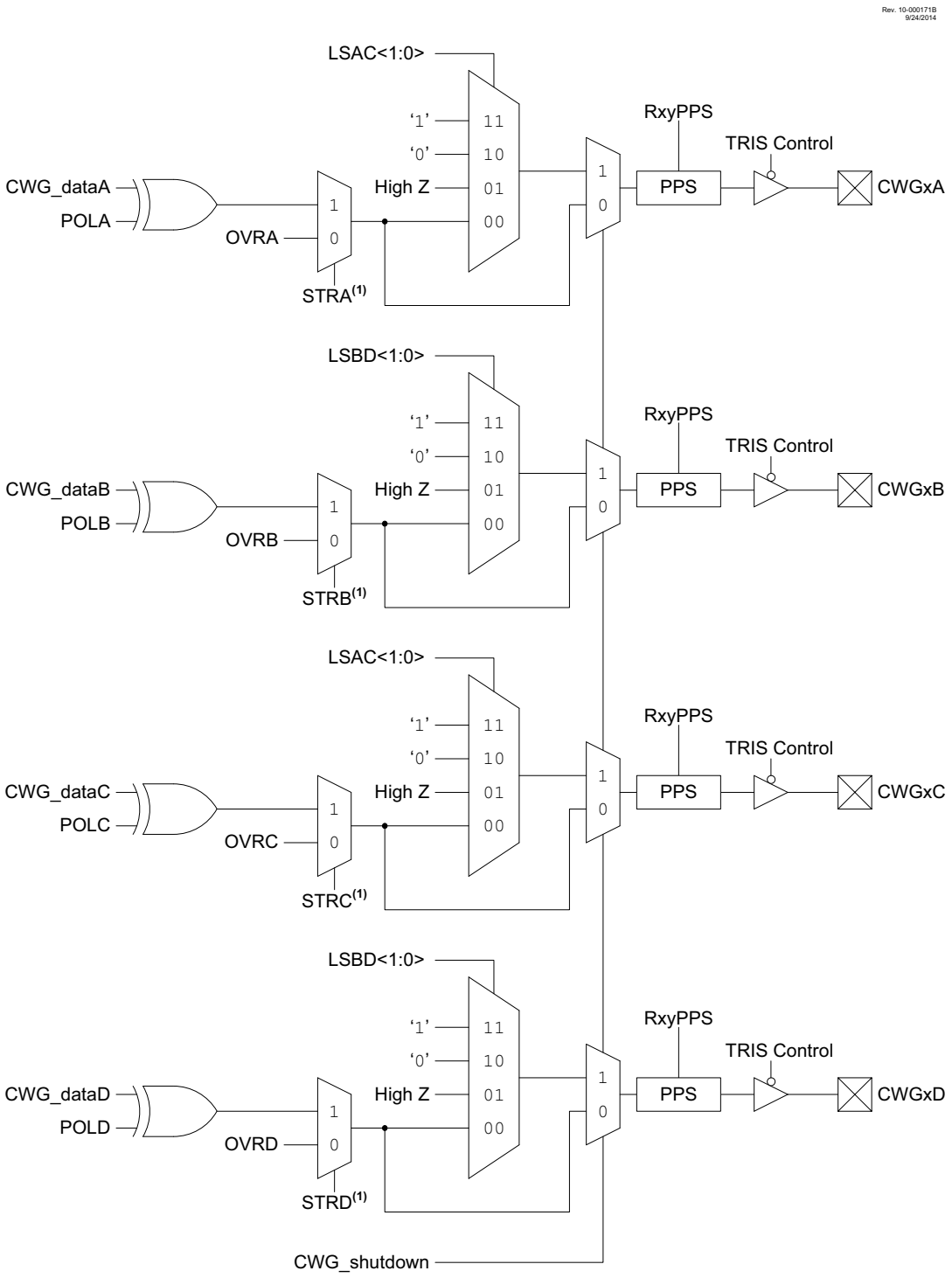
The unused outputs CWGxC and CWGxD drive copies of CWGxA and CWGxB, respectively, but with polarity controlled by the POLC and POLD bits of the CWGxCON1 register, respectively.

28.1.3 FULL-BRIDGE MODES

In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth is modulated by the input data signal. In Forward Full-Bridge mode, CWGxA is driven to its active state, CWGxB and CWGxC are driven to their inactive state, and CWGxD is modulated by the input signal. In Reverse Full-Bridge mode, CWGxC is driven to its active state, CWGxA and CWGxD are driven to their inactive states, and CWGxB is modulated by the input signal. In Full-Bridge mode, the dead-band period is used when there is a switch from forward to reverse or vice-versa. This dead-band control is described in **Section 28.5 “Dead-Band Control”**, with additional details in **Section 28.6 “Rising Edge and Reverse Dead Band”** and **Section 28.7 “Falling Edge and Forward Dead Band”**.

The mode selection may be toggled between forward and reverse by toggling the MODE<0> bit of the CWGxCON0 while keeping MODE<2:1> static, without disabling the CWG module.

FIGURE 28-5: CWG OUTPUT BLOCK DIAGRAM



Note 1: STRx is held to 1 in all modes other than Output Steering Mode.

30.8 Register Definitions: SMT Control

Long bit name prefixes for the Signal Measurement Timer peripherals are shown in Table 30-2. Refer to **Section 1.1 "Register and Bit Naming Conventions"** for more information.

TABLE 30-2:

Peripheral	Bit Name Prefix
SMT1	SMT1
SMT2	SMT2

REGISTER 30-1: SMTxCON0: SMT CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN(1)	—	STP	WPOL	SPOL	CPOL	SMTxPS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** SMT Enable bit(1)
1 = SMT is enabled
0 = SMT is disabled; internal states are reset, clock requests are disabled

bit 6 **Unimplemented**: Read as '0'

bit 5 **STP:** SMT Counter Halt Enable bit
When SMTxTMR = SMTxPR:
1 = Counter remains SMTxPR; period match interrupt occurs when clocked
0 = Counter resets to 24'h000000; period match interrupt occurs when clocked

bit 4 **WPOL:** SMTxWIN Input Polarity Control bit
1 = SMTxWIN signal is active-low/falling edge enabled
0 = SMTxWIN signal is active-high/rising edge enabled

bit 3 **SPOL:** SMTxSIG Input Polarity Control bit
1 = SMTx_signal is active-low/falling edge enabled
0 = SMTx_signal is active-high/rising edge enabled

bit 2 **CPOL:** SMT Clock Input Polarity Control bit
1 = SMTxTMR increments on the falling edge of the selected clock signal
0 = SMTxTMR increments on the rising edge of the selected clock signal

bit 1-0 **SMTxPS<1:0>:** SMT Prescale Select bits
11 = Prescaler = 1:8
10 = Prescaler = 1:4
01 = Prescaler = 1:2
00 = Prescaler = 1:1

Note 1: Setting EN to '0' does not affect the register contents.

REGISTER 30-15: SMTxCPWL: SMT CAPTURED PULSE WIDTH REGISTER – LOW BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
SMTxCPW<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxCPW<7:0>**: Significant bits of the SMT PW Latch – Low Byte

REGISTER 30-16: SMTxCPWH: SMT CAPTURED PULSE WIDTH REGISTER – HIGH BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
SMTxCPW<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxCPW<15:8>**: Significant bits of the SMT PW Latch – High Byte

REGISTER 30-17: SMTxCPWU: SMT CAPTURED PULSE WIDTH REGISTER – UPPER BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
SMTxCPW<23:16>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxCPW<23:16>**: Significant bits of the SMT PW Latch – Upper Byte

31.2.5 VALID BIT

Several values used by the AT module must be calculated from external signals. As such, these values may be inaccurate for a period of time after the angular timer starts up. Because of this, the module will not output signals or trigger interrupts for a period of time after the module is enabled, or under certain other conditions that might jeopardize accurate output values. This output inhibition is indicated by the read-only VALID bit of the ATxCON1 being clear.

The following cases will clear the VALID bit in hardware:

- Any write to ATxRES register pair
- Phase counter overflow (ATxPHS register pair) clocked beyond 0x3FF)
- In-Circuit Debugger halt
- EN = 0
- ATxPER register pair = 0
- Device Reset

As long as the VALID bit is cleared, the following occurs:

- Period clock is not output and associated interrupts do not trigger.
- Missed pulse is not output and associated interrupts do not trigger.
- Phase clock is not output and associated interrupts do not trigger.
- Phase counter does not increment.
- Capture logic does not function and associated interrupts do not trigger.
- Compare logic does not function and associated interrupts do not trigger.
- Every ATxsig edge latches the period counter into the ATxPER register pair, regardless of mode.

In single-pulse modes, the VALID bit becomes set upon the 3rd active input edge of the signal that latches the ATxPER register pair. In multi-pulse modes, a missing pulse trigger is also required, ensuring that at least one full revolution of the input has occurred.

An example of the VALID bit in Single-Pulse mode is shown in Figure 31-6.

31.2.6 DETERMINING ACCURACY

The ATxRES register pair determines the resolution of the period measurement and, by extension, the maximum value that the phase counter reaches at the end of each input signal period. The interim value, ATxPER, used to derive the phase counter is, by nature of the circuitry, an integer. The ratio of the integer value obtained by the circuit and the calculated floating point value is the inherent error of the measurement. When ATxRES is small then integer rounding results in large errors. Factors that contribute to large errors include:

- Large values for ATxRES
- Relatively low ATxclk frequency
- Relatively high ATxsig input frequency

The actual error can be determined with Equation 31-7.

EQUATION 31-7:

$$period = \frac{F(ATxclk)}{F(ATxsig) \bullet (ATxRES + 1)}$$

$$error\% = 100 \bullet \left(\frac{period - int(period + 1)}{period}\right)$$

31.3 Input and Clock Selection

The input clock for the AT module can come from either the FOSC system clock or the 16 MHz HFINTOSC, and is chosen by the CS0 bit of the ATxCLK register. In addition, the clock is run through a prescaler that can be /1, /2, /4, or /8, which is configured by the PS<1:0> bits of the ATxCON0 register. This prescaled clock is then used for all clock operations of the Angular Timer, and as such, should be used for all of the equations demonstrated above determining the Angular Timer's behavior.

The input signal for the AT module can come from a variety of sources. The source is selected by the SSEL bits of the ATxSIG register (Register 31-4).

31.4 Module Outputs

31.4.1 ANGLE/PHASE CLOCK OUTPUT

The angle/phase clock signal (ATx_phsclk) can be used by the CLC as an input signal to combinational logic. The polarity of this signal is configured by the PHP bit of the ATxCON1 register.

31.4.2 PERIOD CLOCK OUTPUT

The period clock signal (ATx_perclk) can be used as an input clock for the Timer2/4/6 and Signal Measurement module, as well as an input signal to the CLC for combinational logic. The polarity of this signal is configured by the PRP bit of the ATxCON1 register (Register 31-2).

31.4.3 MISSED PULSE OUTPUT

The missed pulse signal (ATx_missedpulse) can be used by the CLC as an input signal to combinational logic. The polarity of this signal is configured by the MPP bit of the ATxCON1 register.

TABLE 35-11: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
30	TMCL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	
31	TWDTLP	Low-Power Watchdog Timer Time-out Period	10	16	27	ms	VDD = 3.3V-5V, 1:16 Prescaler used
32	TOST	Oscillator Start-up Timer Period(1)	—	1024	—	TOSC	
33*	TPWRT	Power-up Timer Period	40	65	140	ms	$\overline{PWRTE}$ = 0
34*	TIOZ	I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	VBOR	Brown-out Reset Voltage(2)	2.55	2.70	2.85	V	BORV = 0
			2.35	2.45	2.58	V	BORV = 1 (PIC16F1614/8)
			1.80	1.90	2.05	V	BORV = 1 (PIC16LF1614/8)
36*	VHYST	Brown-out Reset Hysteresis	0	25	60	mV	-40°C ≤ TA ≤ +85°C
37*	TBORDC	Brown-out Reset DC Response Time	1	16	35	µs	VDD ≤ VBOR
38	VLPBOR	Low-Power Brown-Out Reset Voltage	1.8	2.1	2.5	V	LPBOR = 1

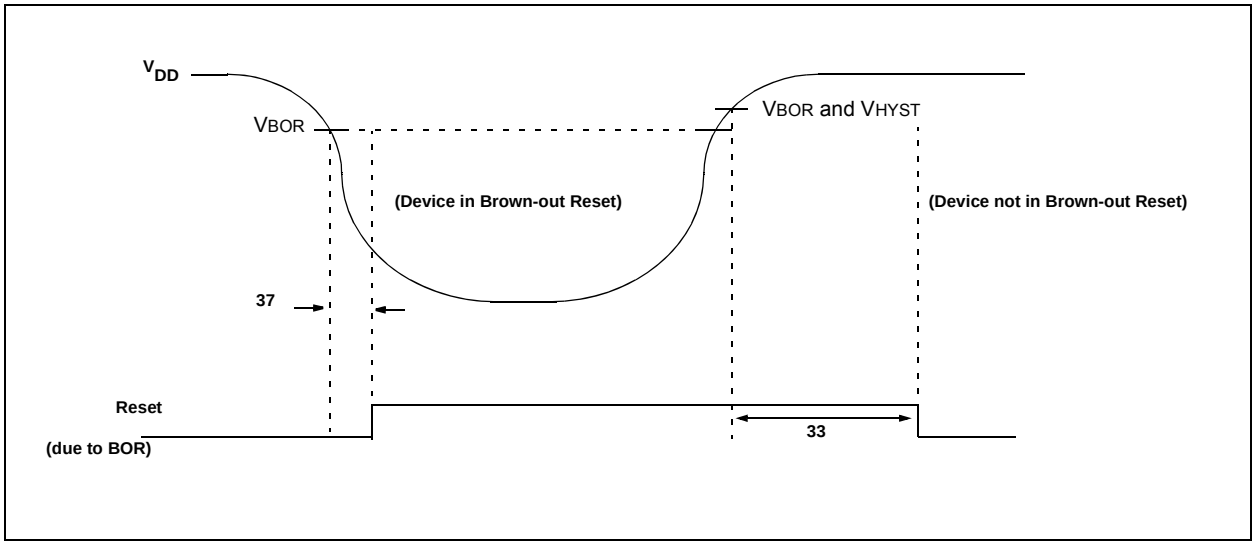
* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

2: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 35-9: BROWN-OUT RESET TIMING AND CHARACTERISTICS



36.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the L and LF devices.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum", "Max.", "Minimum" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 500 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

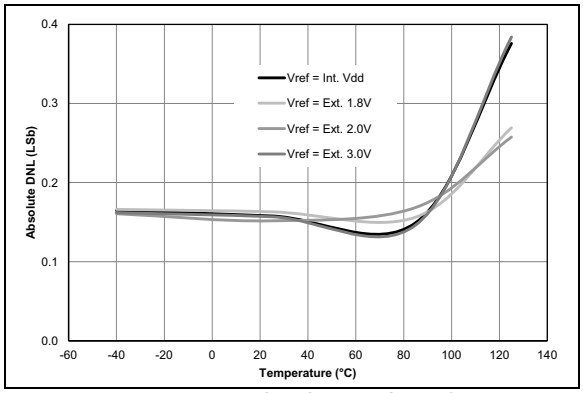


FIGURE 36-97: *Absolute Value of DAC DNL Error, V_{DD} = 3.0V, V_{REF} = V_{DD}.*

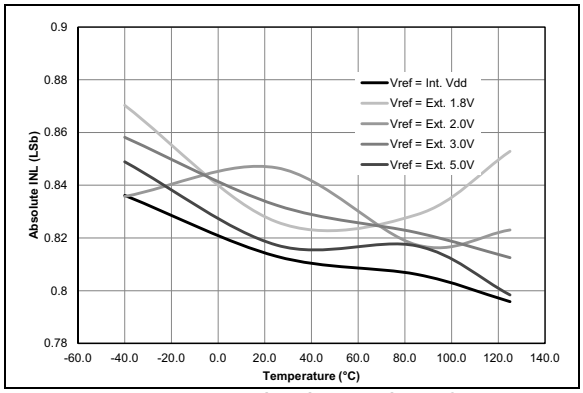


FIGURE 36-100: *Absolute Value of DAC INL Error, V_{DD} = 5.0V, V_{REF} = V_{DD}, PIC16F1614/8 Only.*

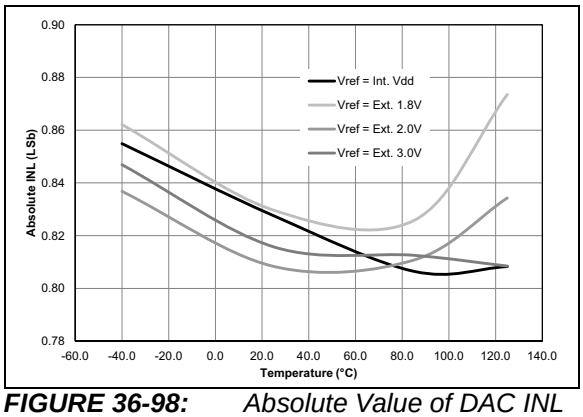


FIGURE 36-98: *Absolute Value of DAC INL Error, V_{DD} = 3.0V, V_{REF} = V_{DD}.*

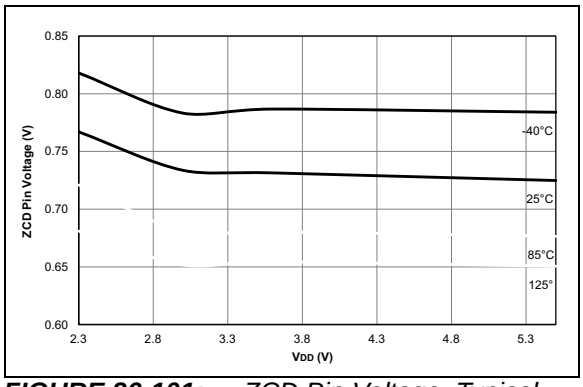


FIGURE 36-101: *ZCD Pin Voltage, Typical Measured Values.*

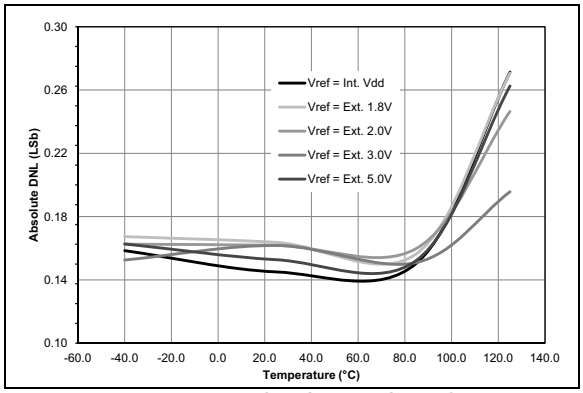


FIGURE 36-99: *Absolute Value of DAC DNL Error, V_{DD} = 5.0V, V_{REF} = V_{DD}, PIC16F1614/8 Only.*

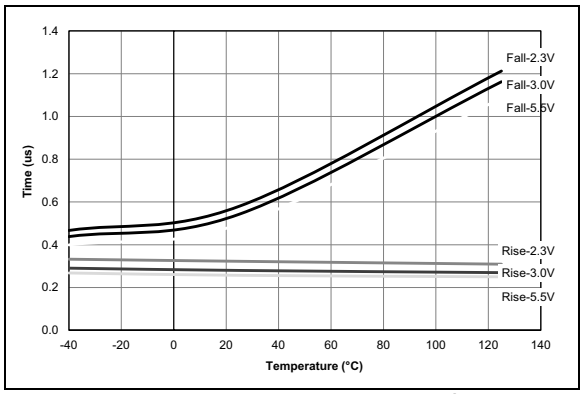


FIGURE 36-102: *ZCD Response Time over Voltage Typical Measured Values.*