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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1618-i-p

PIN ALLOCATION TABLES

TABLE 3: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1614)

I/O	14-Pin PDIP, SOIC, TSSOP	16-Pin UQFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	CLC	EUSART	SMT	Angular Timer	MSSP	PWM	High Current I/O	Interrupt	Pull-up	Basic
RA0	13	12	AN0	DAC1OUT1	C1IN+	—	—	—	—	—	—	—	—	—	—	—	IO	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	—	IO	Y	ICSPCLK
RA2	11	10	AN2	—	—	T0CKI ⁽¹⁾	—	CWG1IN ⁽¹⁾	ZCD1IN	—	—	—	—	—	—	—	INT IO	Y	—
RA3	4	3	—	—	—	T6IN ⁽¹⁾	—	—	—	—	—	SMTWIN2 ⁽¹⁾	—	—	—	—	IO	Y	MCLR/VPP
RA4	3	2	AN3	—	—	T1G ⁽¹⁾	—	—	—	—	—	SMTSIG1 ⁽¹⁾	—	—	—	—	IO	Y	CLKOUT
RA5	2	1	—	—	—	T1CKI ⁽¹⁾ T2IN ⁽¹⁾	—	—	—	—	—	SMTWIN1 ⁽¹⁾	—	—	—	—	IO	Y	CLKIN
RC0	10	9	AN4	—	C2IN+	T5CKI ⁽¹⁾	—	—	—	—	—	—	—	SCK ^(1,3)	—	—	IO	Y	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	T4IN ⁽¹⁾	—	—	—	—	—	SMTSIG2 ⁽¹⁾	—	SDI ⁽¹⁾	—	—	IO	Y	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IO	Y	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	T5G ⁽¹⁾	CCP2 ⁽¹⁾	—	—	CLCIN0 ⁽¹⁾	—	—	ATCC1 ⁽¹⁾	SS ⁽¹⁾	—	—	IO	Y	—
RC4	6	5	—	—	—	T3G ⁽¹⁾	—	—	—	CLCIN1 ⁽¹⁾	CK ⁽¹⁾	—	ATCC2 ⁽¹⁾	—	—	HIC4	IO	Y	—
RC5	5	4	—	—	—	T3CKI ⁽¹⁾	CCP1 ⁽¹⁾	—	—	—	RX ^(1,3)	—	ATIN ⁽¹⁾ ATCC3 ⁽¹⁾	—	—	HIC5	IO	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	—	—	—	C1OUT	—	CCP1	CWG1A	ZCD1OUT	CLC1OUT	DT ⁽³⁾	—	—	SDO	PWM3OUT	—	—	—	—
	—	—	—	—	C2OUT	—	CCP2	CWG1B	—	CLC2OUT	CK	—	—	SCK ⁽³⁾	PWM4OUT	—	—	—	—
	—	—	—	—	—	—	—	CWG1C	—	—	TX	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	CWG1D	—	—	—	—	—	—	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3-14: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 8											
40Ch	—	Unimplemented								—	—
40Dh	—	Unimplemented								—	—
40Eh	HIDRVC	—	—	HIDC5	HIDC4	—	—	—	—	--00 ----	--00 ----
40Fh to 412h	—	Unimplemented								—	—
413h	TMR4	Timer4 Module Register								0000 0000	0000 0000
414h	PR4	Timer4 Period Register								1111 1111	1111 1111
415h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>			0000 0000	0000 0000	
416h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>			0000 0000	0000 0000		
417h	T4CLKCON	—	—	—	—	CS<3:0>			---- 0000	---- 0000	
418h	T4RST	—	—	—	—	RSEL<3:0>			---- 0000	---- 0000	
419h	—	Unimplemented								—	—
41Ah	TMR6	Timer6 Module Register								0000 0000	0000 0000
41Bh	PR6	Timer6 Period Register								1111 1111	1111 1111
41Ch	T6CON	ON	CKPS<2:0>			OUTPS<3:0>			0000 0000	0000 0000	
41Dh	T6HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>			0000 0000	0000 0000		
41Eh	T6CLKCON	—	—	—	—	CS<3:0>			---- 0000	---- 0000	
41Fh	T6RST	—	—	—	—	RSEL<3:0>			---- 0000	---- 0000	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

- Note** 1: PIC16F1614/8 only.
 2: Unimplemented, read as '1'.
 3: PIC16(L)F1614 only.
 4: PIC16(L)F1618 only.

5.2.2.7 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4x PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. Either the 8 or 16 MHz internal oscillator settings can be used, with the 16 MHz being divided by two before being input into the PLL. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Words must be set to use the INTOSC source as the device system clock (FOSC<1:0> = 00).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<1:0> in Configuration Words (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to either the 16 MHz (IRCF<3:0> = 1111) or the 8 MHz HFINTOSC (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4x PLL, or the PLEN bit of the Configuration Words must be programmed to a '1'.

Note: When using the PLEN bit of the Configuration Words, the 4x PLL cannot be disabled by software and the 8/16 MHz HFINTOSC option will no longer be available.

The 4x PLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4x PLL with the internal oscillator.

5.2.2.8 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-3). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

1. IRCF<3:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. The new clock is now active.
6. The OSCSTAT register is updated as required.
7. Clock switch is complete.

See Figure 5-3 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 5-1.

Start-up delay specifications are located in the oscillator tables of **Section 35.0 "Electrical Specifications"**.

REGISTER 5-2: OSCSTAT: OSCILLATOR STATUS REGISTER

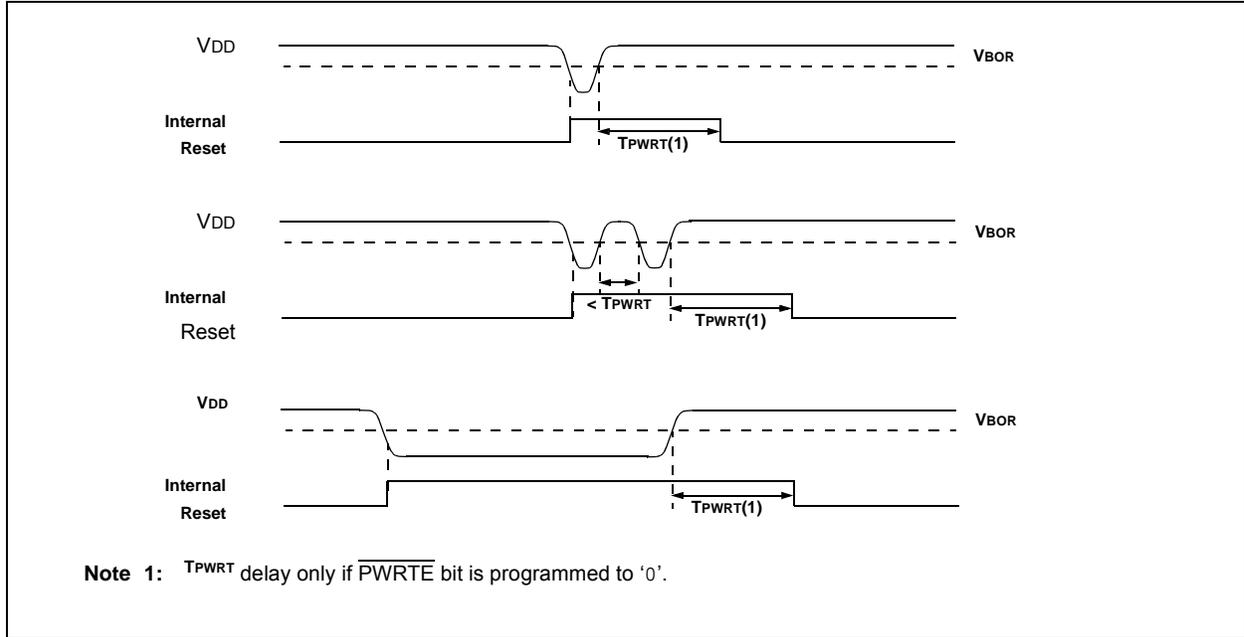
U-0	R-0/q	U-0	R-0/q	R-0/q	R-q/q	R-0/q	R-0/q
—	PLL R	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Conditional

bit 7	Unimplemented: Read as '0'
bit 6	PLL R: 4x PLL Ready bit 1 = 4x PLL is ready 0 = 4x PLL is not ready
bit 5	OSTS: Oscillator Start-Up Timer Status bit 1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Words 0 = Running from an internal oscillator (FOSC<2:0> = 100)
bit 4	HFIOFR: High-Frequency Internal Oscillator Ready bit 1 = HFINTOSC is ready 0 = HFINTOSC is not ready
bit 3	HFIOFL: High-Frequency Internal Oscillator Locked bit 1 = HFINTOSC is at least 2% accurate 0 = HFINTOSC is not 2% accurate
bit 2	MFIOFR: Medium-Frequency Internal Oscillator Ready bit 1 = MFINTOSC is ready 0 = MFINTOSC is not ready
bit 1	LFIOFR: Low-Frequency Internal Oscillator Ready bit 1 = LFINTOSC is ready 0 = LFINTOSC is not ready
bit 0	HFIOFS: High-Frequency Internal Oscillator Stable bit 1 = HFINTOSC is stable 0 = HFINTOSC is not stable

FIGURE 6-2: BROWN-OUT SITUATIONS



6.3 Register Definitions: BOR Control

REGISTER 6-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	R/W-0/u	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	BORFS	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-Out Reset Enable bit

If BOREN <1:0> in Configuration Words = 01:

- 1 = BOR Enabled
- 0 = BOR Disabled

If BOREN <1:0> in Configuration Words ≠ 01:

SBOREN is read/write, but has no effect on the BOR

bit 6 **BORFS:** Brown-Out Reset Fast Start bit⁽¹⁾

If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN <1:0> = 01 (Under software control):

- 1 = Band gap is forced on always (covers sleep/wake-up/operating cases)
- 0 = Band gap operates normally, and may turn off

If BOREN <1:0> = 11 (Always on) or BOREN <1:0> = 00 (Always off)

BORFS is Read/Write, but has no effect.

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-Out Reset Circuit Ready Status bit

- 1 = The Brown-out Reset circuit is active
- 0 = The Brown-out Reset circuit is inactive

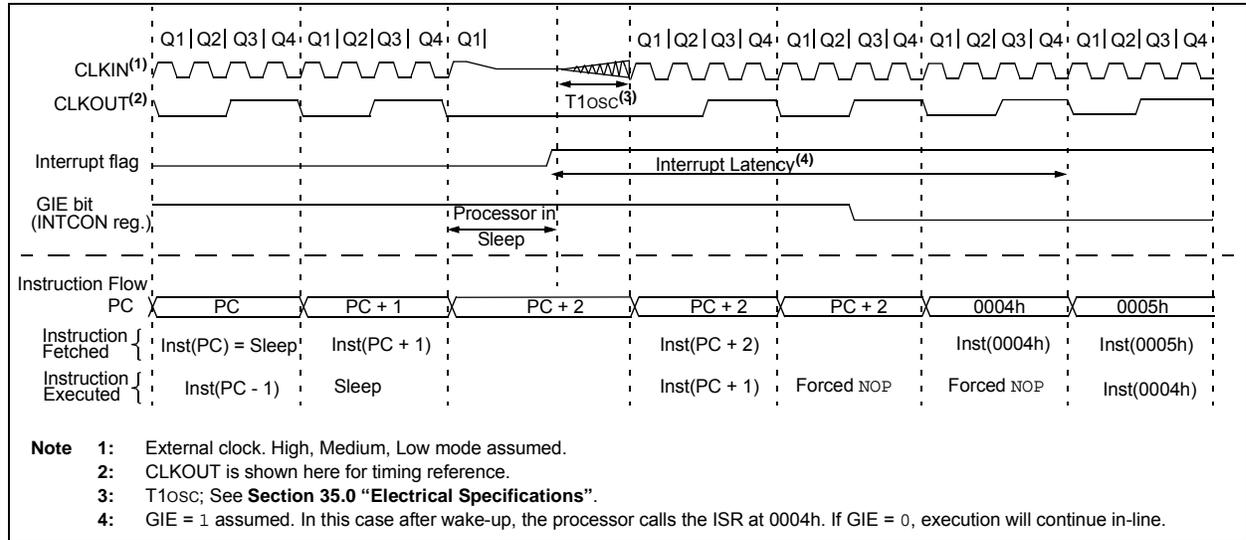
Note 1: BOREN <1:0> bits are located in Configuration Words.

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			222
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIE2	—	C2IE	C1IE	—	BCLIE	TMR6IE	TMR4IE	CCP2IE	99
PIE3	—	—	CWGIE	ZCDIE	—	—	CLC2IE	CLC1IE	100
PIE4	SCANIE	CRCIE	SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IF	101
PIE5	TMR3GIE	TMR3IE	TMR5GIE	TMR5IE	—	AT1IE	PID1EIE	PID1DIE	102
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	103
PIR2	—	C2IF	C1IF	—	BCLIF	TMR6IF	TMR4IF	CCP2IF	104
PIR3	—	—	CW GIF	ZCDIF	—	—	CLC2IF	CLC1IF	105
PIR4	SCANIF	CRCIF	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF	106
PIR5	TMR3GIF	TMR3IF	TMR5GIF	TMR5IF	—	AT1IF	PID1EIF	PID1DIF	107

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

FIGURE 8-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT



8.2 Low-Power Sleep Mode

This device contains an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode.

Low-Power Sleep mode allows the user to optimize the operating current in Sleep. Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register, putting the LDO and reference circuitry in a low-power state whenever the device is in Sleep.

8.2.1 SLEEP CURRENT VS. WAKE-UP TIME

In the Default Operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The Normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.

8.2.2 PERIPHERAL USAGE IN SLEEP

Some peripherals that can operate in Sleep mode will not operate properly with the Low-Power Sleep mode selected. The LDO will remain in the Normal-Power mode when those peripherals are enabled. The Low-Power Sleep mode is intended for use with these peripherals:

- Brown-Out Reset (BOR)
- Watchdog Timer (WDT)
- External interrupt pin/Interrupt-on-change pins
- Timer1 (with external clock source)

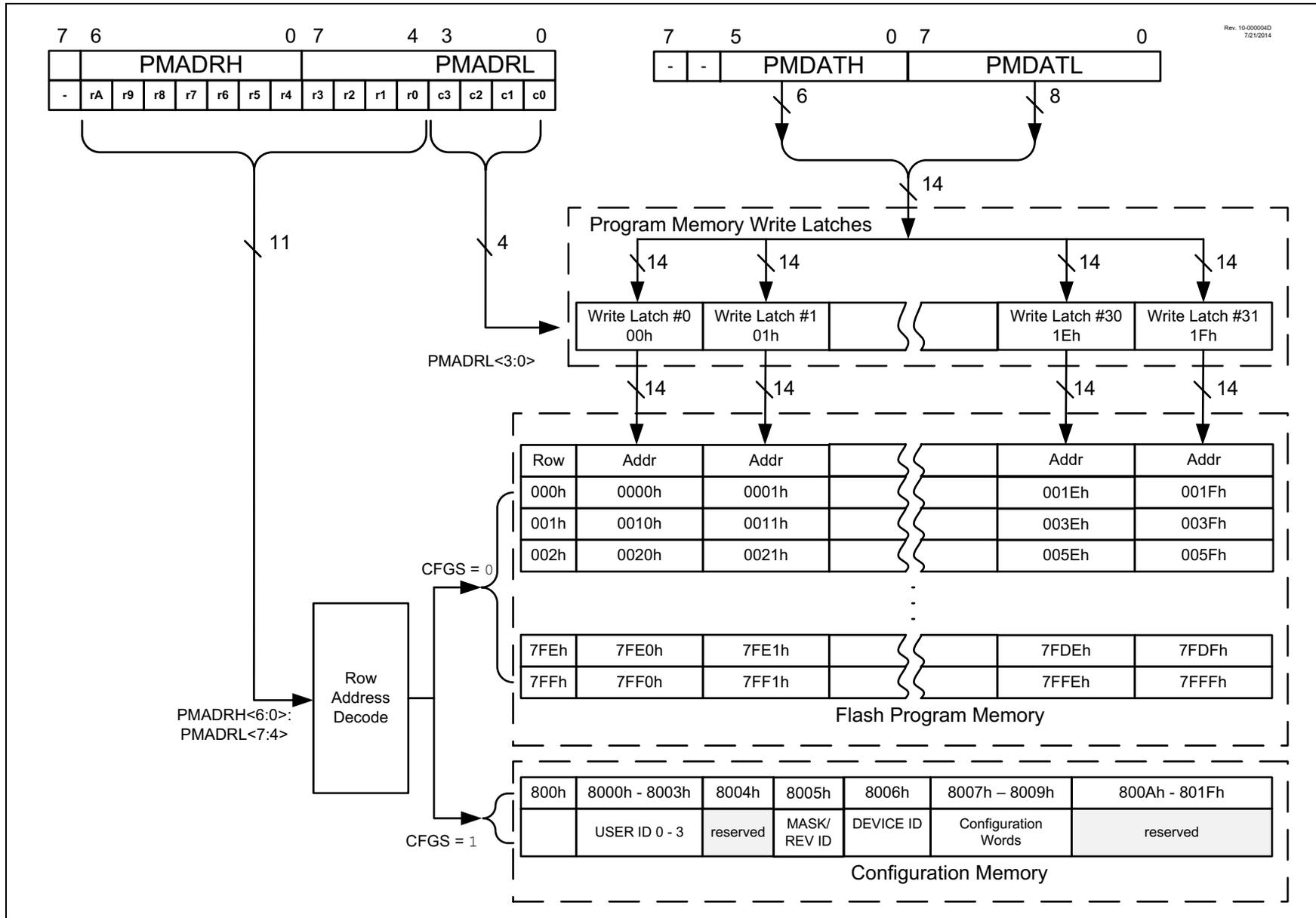
The Complementary Waveform Generator (CWG) can utilize the HFINTOSC oscillator as either a clock source or as an input source. Under certain conditions, when the HFINTOSC is selected for use with the CWG modules, the HFINTOSC will remain active during Sleep. This will have a direct effect on the Sleep mode current.

Please refer to sections **Section 28.11 "Operation During Sleep"** for more information.

Note: The PIC16LF1614/8 does not have a configurable Low-Power Sleep mode. PIC16LF1614/8 is an unregulated device and is always in the lowest power state when in Sleep, with no wake-up time penalty. This device has a lower maximum VDD and I/O voltage than the PIC16F1614/8. See **Section 35.0 "Electrical Specifications"** for more information.

FIGURE 10-5: BLOCK WRITES TO FLASH PROGRAM MEMORY WITH 32 WRITE LATCHES

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7/21/2014



REGISTER 12-7: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	SLRA5	SLRA4	—	SLRA2	SLRA1	SLRA0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **SLRA<5:4>:** PORTA Slew Rate Enable bits
For RA<5:4> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate
- bit 3 **Unimplemented:** Read as '0'
- bit 2-0 **SLRA<2:0>:** PORTA Slew Rate Enable bits
For RA<2:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-8: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **INLVLA<5:0>:** PORTA Input Level Select bits
For RA<5:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

14.6 Register Definitions: Interrupt-on-Change Control

REGISTER 14-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAP<5:0>:** Interrupt-on-Change PORTA Positive Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCAF_x bit and IOCIF flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 14-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAN<5:0>:** Interrupt-on-Change PORTA Negative Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCAF_x bit and IOCIF flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 14-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared HS - Bit is set in hardware

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAF<5:0>:** Interrupt-on-Change PORTA Flag bits

- 1 = An enabled change was detected on the associated pin.
Set when IOCAP_x = 1 and a rising edge was detected on RAX, or when IOCAN_x = 1 and a falling edge was detected on RAX.
- 0 = No change was detected, or the user cleared the detected change.

22.5.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

22.5.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

22.5.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 22-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note: Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

22.5.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 22-5 for timing details.

If the Single Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 22-6 for timing details.

22.5.5 TIMER1 GATE VALUE STATUS

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

22.5.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

TABLE 22-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	152
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	103
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Count								227*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Count								227*
TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Count								227*
TMR3L	Holding Register for the Least Significant Byte of the 16-bit TMR3 Count								227*
TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Count								227*
TMR5L	Holding Register for the Least Significant Byte of the 16-bit TMR5 Count								227*
TRISA	—	—	TRISA5	TRISA4	— ⁽¹⁾	TRISA2	TRISA1	TRISA0	151
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		—	T1SYNC	—	TMR1ON	231
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS<1:0>		232
T3CON	TMR3CS<1:0>		T3CKPS<1:0>		—	T3SYNC	—	TMR3ON	231
T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/ DONE	T3GVAL	T3GSS<1:0>		232
T5CON	TMR5CS<1:0>		T5CKPS<1:0>		—	T5SYNC	—	TMR5ON	231
T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	T5GGO/ DONE	T5GVAL	T5GSS<1:0>		232

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

* Page provides register information.

Note 1: Unimplemented, read as '1'.

23.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the TxCON register are cleared).
- The diagrams illustrate any clock except $F_{osc}/4$ and show clock-sync delays of at least two full cycles for both ON and Timer2_ers. When using $F_{osc}/4$, the clock-sync delay is at least one instruction period for Timer2_ers; ON applies in the next instruction period.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 26.4 “CCP/PWM Clock Selection”**. The signals are not a part of the Timer2 module.

23.5.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2 operation. The timer increments with each clock input when $ON = 1$ and does not increment when $ON = 0$. When the TMRx count equals the PRx period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 23-4. With $PRx = 5$, the counter advances until $TMRx = 5$, and goes to zero with the next clock.

FIGURE 23-4: SOFTWARE GATE MODE TIMING DIAGRAM (MODE = 00000)

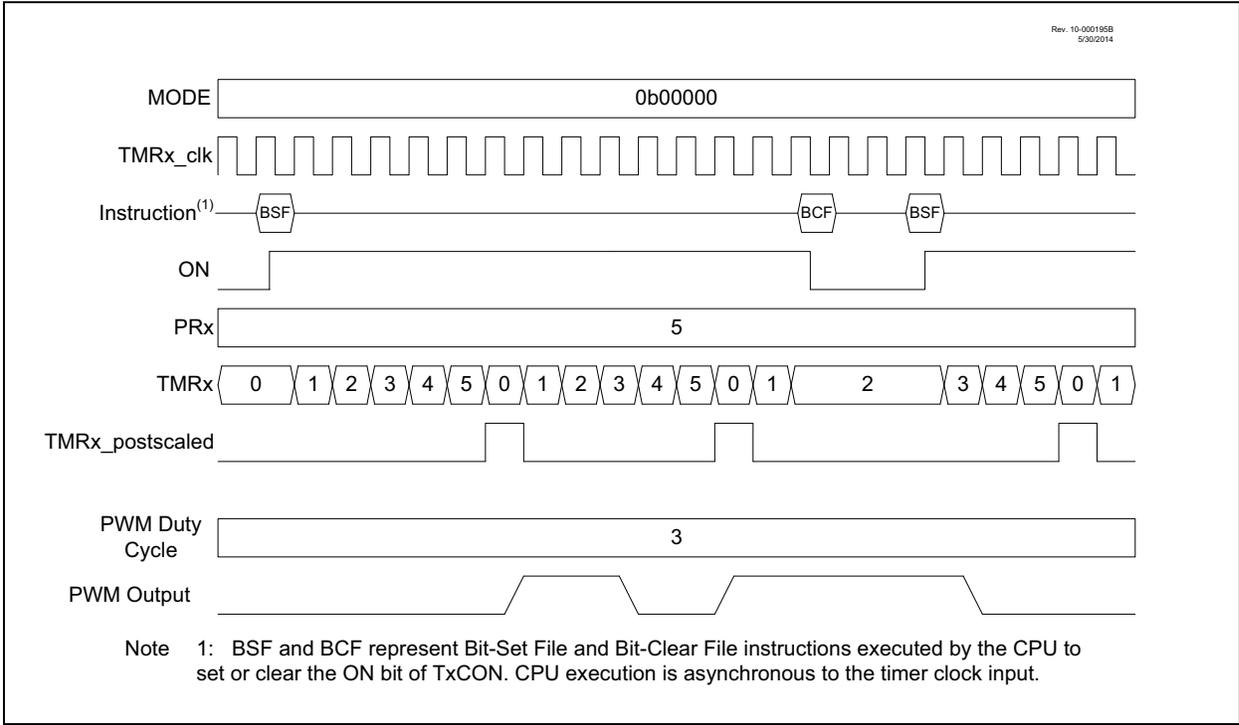


FIGURE 23-13: LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 10110)

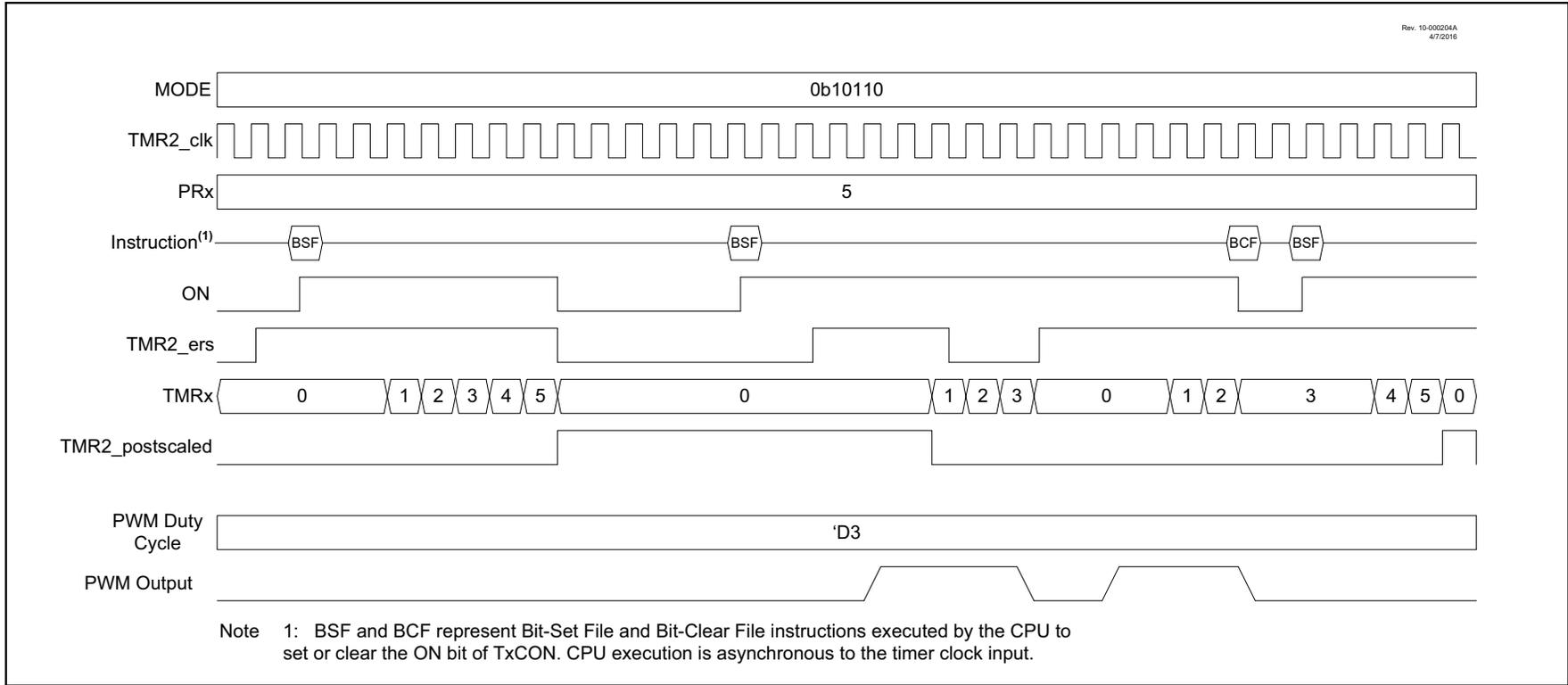


TABLE 23-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	EN	—	OUT	FMT	MODE<3:0>				352
CCP2CON	EN	—	OUT	FMT	MODE<3:0>				352
INTCON	GIE	PEIE	TMR0IE	INTE	IOCFIE	TMR0IF	INTF	IOCFIF	97
PIE1	TMR1GIE	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	103
PR2	Timer2 Module Period Register								235*
TMR2	Holding Register for the 8-bit TMR2 Register								235*
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				254
T2CLKCON	—	—	—	—	CS<3:0>				253
T2RST	—	—	—	—	RSEL<3:0>				256
T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					255
PR4	Timer4 Module Period Register								235*
TMR4	Holding Register for the 8-bit TMR4 Register								235*
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				254
T4CLKCON	—	—	—	—	CS<3:0>				253
T4RST	—	—	—	—	RSEL<3:0>				256
T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					255
PR6	Timer6 Module Period Register								235*
TMR6	Holding Register for the 8-bit TMR6 Register								235*
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				254
T6CLKCON	—	—	—	—	—	T6CS<2:0>			253
T6RST	—	—	—	—	RSEL<3:0>				256
T6HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					255

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

* Page provides register information.

TABLE 25-7: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	152
ANSELB ⁽¹⁾	—	—	ANSB5	ANSB4	—	—	—	—	159
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	—	—	ANSC3	ANSC2	ANSC1	ANSC0	166
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	323
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	103
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	322
RxyPPS	—	—	—	RxyPPS<4:0>					172
SP1BRGL	BRG<7:0>								324
SP1BRGH	BRG<15:8>								324
TRISA	—	—	TRISA5	TRISA4	— ⁽²⁾	TRISA2	TRISA1	TRISA0	151
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	158
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	165
TX1REG	EUSART Transmit Data Register								313*
TX1STA	CSRC	TX9	TXEN	SYNC	SENCB	BRGH	TRMT	TX9D	321

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master transmission.

* Page provides register information.

Note 1: PIC16(L)F1618 only.

2: Unimplemented, read as '1'.

REGISTER 26-2: CCPTMRS: PWM TIMER SELECTION CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
P4TSEL<1:0>		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>	
bit 7						bit 0	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-6 **P4TSEL<1:0>**: PWM4 Timer Selection bits
 11 = Reserved
 10 = PWM4 is based off Timer6 in PWM mode
 01 = PWM4 is based off Timer4 in PWM mode
 00 = PWM4 is based off Timer2 in PWM mode
- bit 5-4 **P3TSEL<1:0>**: PWM3 Timer Selection bits
 11 = Reserved
 10 = PWM3 is based off Timer6 in PWM mode
 01 = PWM3 is based off Timer4 in PWM mode
 00 = PWM3 is based off Timer2 in PWM mode
- bit 3-2 **C2TSEL<1:0>**: CCP2 (PWM2) Timer Selection bits
 11 = Reserved
 10 = CCP2 is based off Timer6 in PWM mode
 01 = CCP2 is based off Timer4 in PWM mode
 00 = CCP2 is based off Timer2 in PWM mode
- bit 1-0 **C1TSEL<1:0>**: CCP1 (PWM1) Timer Selection bits
 11 = Reserved
 10 = CCP1 is based off Timer6 in PWM mode
 01 = CCP1 is based off Timer4 in PWM mode
 00 = CCP1 is based off Timer2 in PWM mode

29.2 Data Gating

Outputs from the input multiplexers are directed to the desired logic function input through the data gating stage. Each data gate can direct any combination of the four selected inputs.

Note: Data gating is undefined at power-up.

The gate stage is more than just signal direction. The gate can be configured to direct each input signal as inverted or non-inverted data. Directed signals are ANDed together in each gate. The output of each gate can be inverted before going on to the logic function stage.

The gating is in essence a 1-to-4 input AND/NAND/OR/NOR gate. When every input is inverted and the output is inverted, the gate is an OR of all enabled data inputs. When the inputs and output are not inverted, the gate is an AND of all enabled inputs.

Table 29-2 summarizes the basic logic that can be obtained in gate 1 by using the gate logic select bits. The table shows the logic of four input variables, but each gate can be configured to use less than four. If no inputs are selected, the output will be zero or one, depending on the gate output polarity bit.

TABLE 29-2: DATA GATING LOGIC

CLCxGLS0	LCxG1POL	Gate Logic
0x55	1	AND
0x55	0	NAND
0xAA	1	NOR
0xAA	0	OR
0x00	0	Logic 0
0x00	1	Logic 1

It is possible (but not recommended) to select both the true and negated values of an input. When this is done, the gate output is zero, regardless of the other inputs, but may emit logic glitches (transient-induced pulses). If the output of the channel must be zero or one, the recommended method is to set all gate bits to zero and use the gate polarity bit to set the desired level.

Data gating is configured with the logic gate select registers as follows:

- Gate 1: CLCxGLS0 (Register 29-6)
- Gate 2: CLCxGLS1 (Register 29-7)
- Gate 3: CLCxGLS2 (Register 29-8)
- Gate 4: CLCxGLS3 (Register 29-9)

Register number suffixes are different than the gate numbers because other variations of this module have multiple gate selections in the same register.

Data gating is indicated in the right side of Figure 29-2. Only one gate is shown in detail. The remaining three gates are configured identically with the exception that the data enables correspond to the enables for that gate.

29.2.1 LOGIC FUNCTION

There are eight available logic functions including:

- AND-OR
- OR-XOR
- AND
- S-R Latch
- D Flip-Flop with Set and Reset
- D Flip-Flop with Reset
- J-K Flip-Flop with Reset
- Transparent Latch with Set and Reset

Logic functions are shown in Figure 29-3. Each logic function has four inputs and one output. The four inputs are the four data gate outputs of the previous stage. The output is fed to the inversion stage and from there to other peripherals, an output pin, and back to the CLCx itself.

29.2.2 OUTPUT POLARITY

The last stage in the configurable logic cell is the output polarity. Setting the LCxPOL bit of the CLCxCON register inverts the output signal from the logic stage. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

GOTO Unconditional Branch

Syntax: [*label*] GOTO *k*

Operands: $0 \leq k \leq 2047$

Operation: $k \rightarrow PC<10:0>$
 $PCLATH<6:3> \rightarrow PC<14:11>$

Status Affected: None

Description: GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

INCF Increment f

Syntax: [*label*] INCF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination})$

Status Affected: Z

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ Increment f, Skip if 0

Syntax: [*label*] INCFSZ *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination})$,
 skip if result = 0

Status Affected: None

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

IORLW Inclusive OR literal with W

Syntax: [*label*] IORLW *k*

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: [*label*] IORWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

LSLF Logical Left Shift

Syntax: [*label*] LSLF *f {,d}*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<7>) \rightarrow C$
 $(f<6:0>) \rightarrow \text{dest}<7:1>$
 $0 \rightarrow \text{dest}<0>$

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



LSRF Logical Right Shift

Syntax: [*label*] LSRF *f {,d}*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $0 \rightarrow \text{dest}<7>$
 $(f<7:1>) \rightarrow \text{dest}<6:0>$,
 $(f<0>) \rightarrow C$,

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



TABLE 35-2: SUPPLY CURRENT (IDD)^(1,2) (CONTINUED)

PIC16LF1614/8		Standard Operating Conditions (unless otherwise stated)					
PIC16F1614/8							
Param. No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D015		—	9.6	36	μA	1.8	Fosc = 31 kHz, LFINTOSC, -40°C ≤ Ta ≤ +85°C
		—	16.2	60	μA	3.0	
D015		—	39	84	μA	2.3	Fosc = 31 kHz, LFINTOSC, -40°C ≤ Ta ≤ +85°C
		—	45	90	μA	3.0	
		—	51	108	μA	5.0	
D016		—	215	360	μA	1.8	Fosc = 500 kHz, HFINTOSC
		—	275	480	μA	3.0	
D016		—	270	450	μA	2.3	Fosc = 500 kHz, HFINTOSC
		—	300	500	μA	3.0	
		—	350	620	μA	5.0	
D017*		—	410	800	μA	1.8	Fosc = 8 MHz, HFINTOSC
		—	630	1200	μA	3.0	
D017*		—	530	950	μA	2.3	Fosc = 8 MHz, HFINTOSC
		—	660	1300	μA	3.0	
		—	730	1400	μA	5.0	
D018		—	600	1200	μA	1.8	Fosc = 16 MHz, HFINTOSC
		—	970	1850	μA	3.0	
D018		—	780	1500	μA	2.3	Fosc = 16 MHz, HFINTOSC
		—	1000	1900	μA	3.0	
		—	1090	2100	μA	5.0	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS; MCLR = VDD; WDT disabled.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.