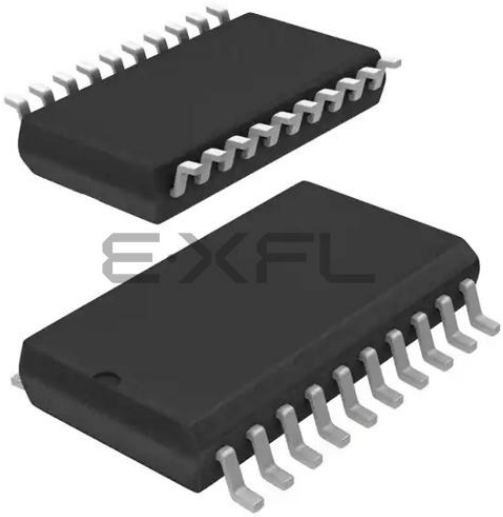

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f2m6

Contents

1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

5 Pinout and pin description

Table 4. Legend/abbreviations for pin description tables

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold **X** (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Table 6. STM8S103F2 and STM8S103F3 pin descriptions (continued)

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/[TIM1_ CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/[T IM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).1

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C Own address register low	0x00
0x00 5214		I2C_OARH	I2C Own address register high	0x00
0x00 5215		Reserved		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x0X
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E		I2C_PECR	I2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (21 byte)			

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

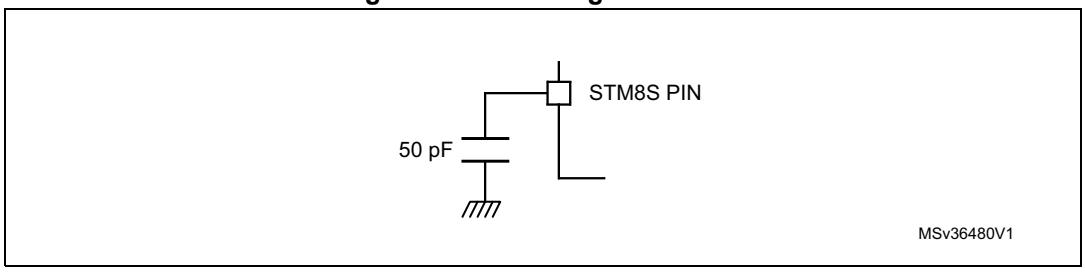
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

Figure 8. Pin loading conditions



10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 19. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D(3)	Power dissipation at T_A = 125 °C for suffix 3	TSSOP20	-	59	mW
		SO20W	-	55	
		UFQFPN20	-	55	
		LQFP32	-	83	
		UFQFPN32	-	132	
		SDIP32	-	83	
T_A	Ambient temperature for suffix 6 version	Maximum power dissipation	-40	85	°C
T_A	Ambient temperature for suffix 3 version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version	-40	130	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax}- T_A)/\Theta_{JA}$ (see *Section 12: Thermal characteristics*) with the value for T_{Jmax} given in the previous table and the value for Θ_{JA} given in *Section 12: Thermal characteristics*

Figure 10. f_{CPUmax} versus V_{DD}

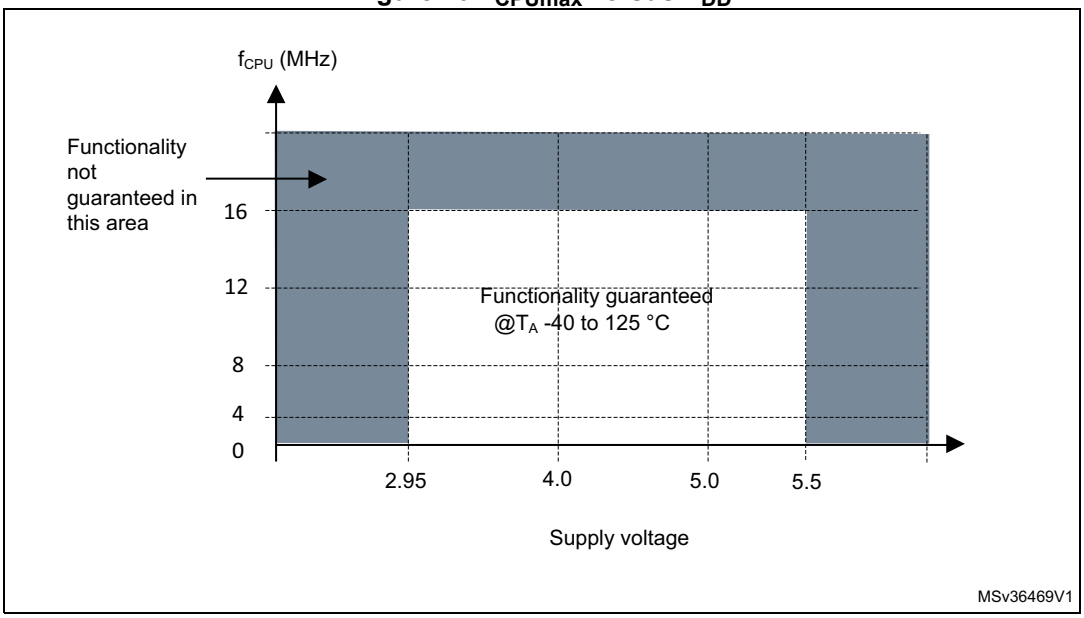


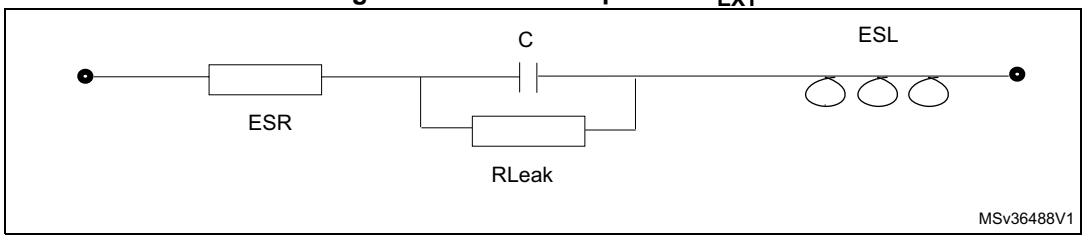
Table 20. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	∞	µs/V
	V_{DD} fall time rate(1)	-	2	-	∞	

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 19*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 9: Pin input voltage*.

Total supply current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

Total current consumption in active halt mode

Table 25. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	300	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power down mode	LSI RC osc. (128 kHz)	10	20	40	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 26. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	290	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Figure 16. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE external clock, V_{DD} = 5 V

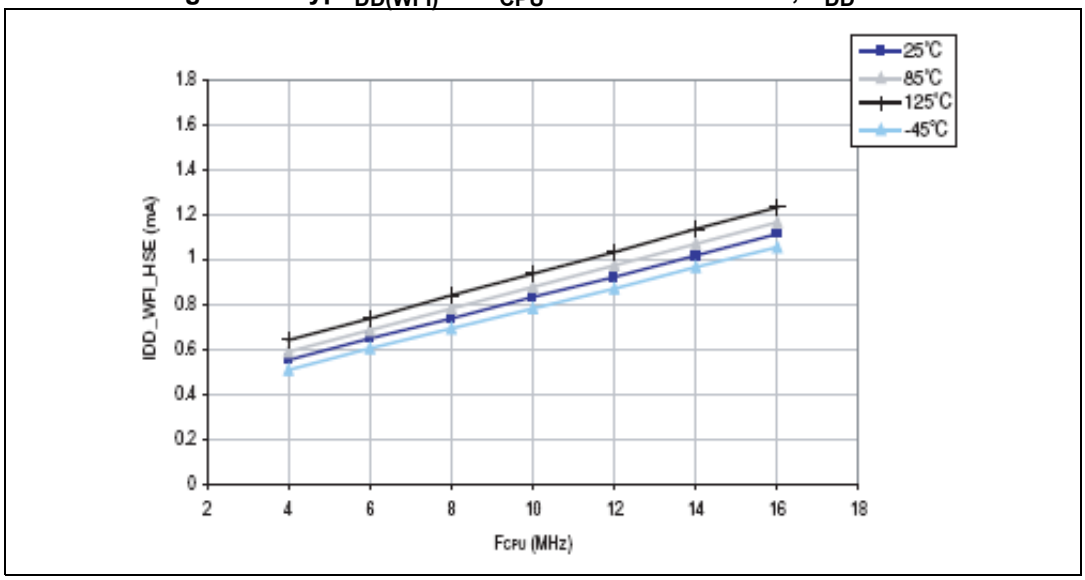
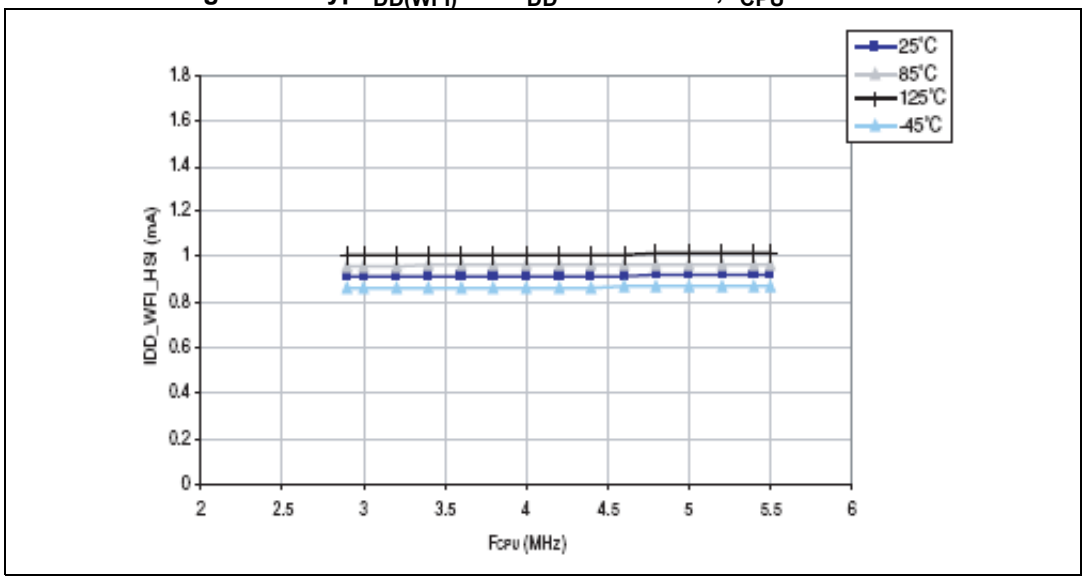


Figure 17. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3 V	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 20 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 20 pF	-	-	50(2)	
I_{lkg}	Digital input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1(3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250(3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design.
3. Guaranteed by characterization results

Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

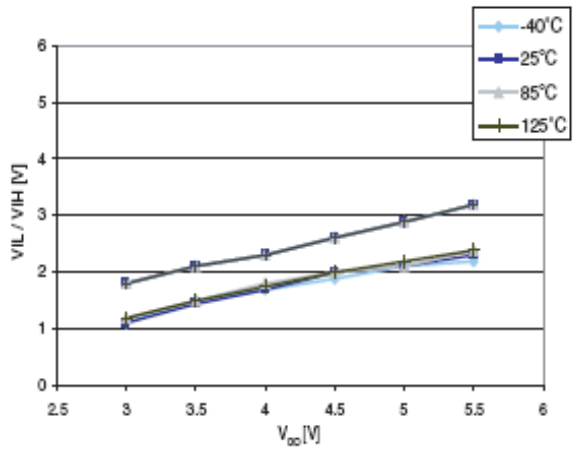


Figure 23. Typical pull-up current vs V_{DD} @ 4 temperatures

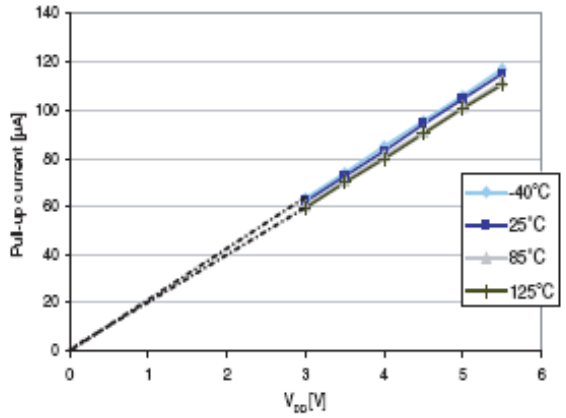


Figure 24. Typical pull-up resistance vs VDD @ 4 temperatures

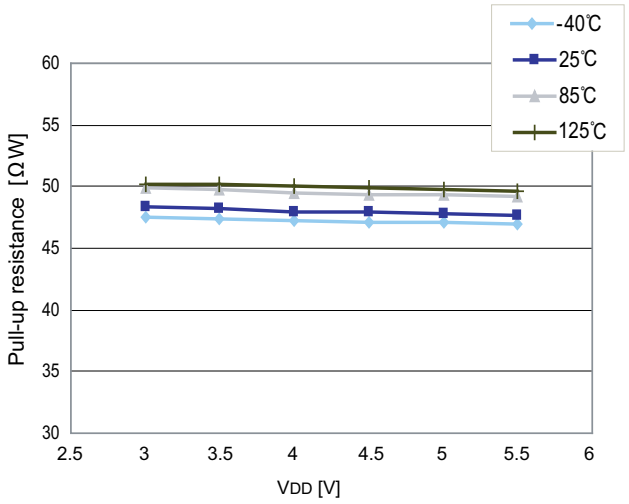
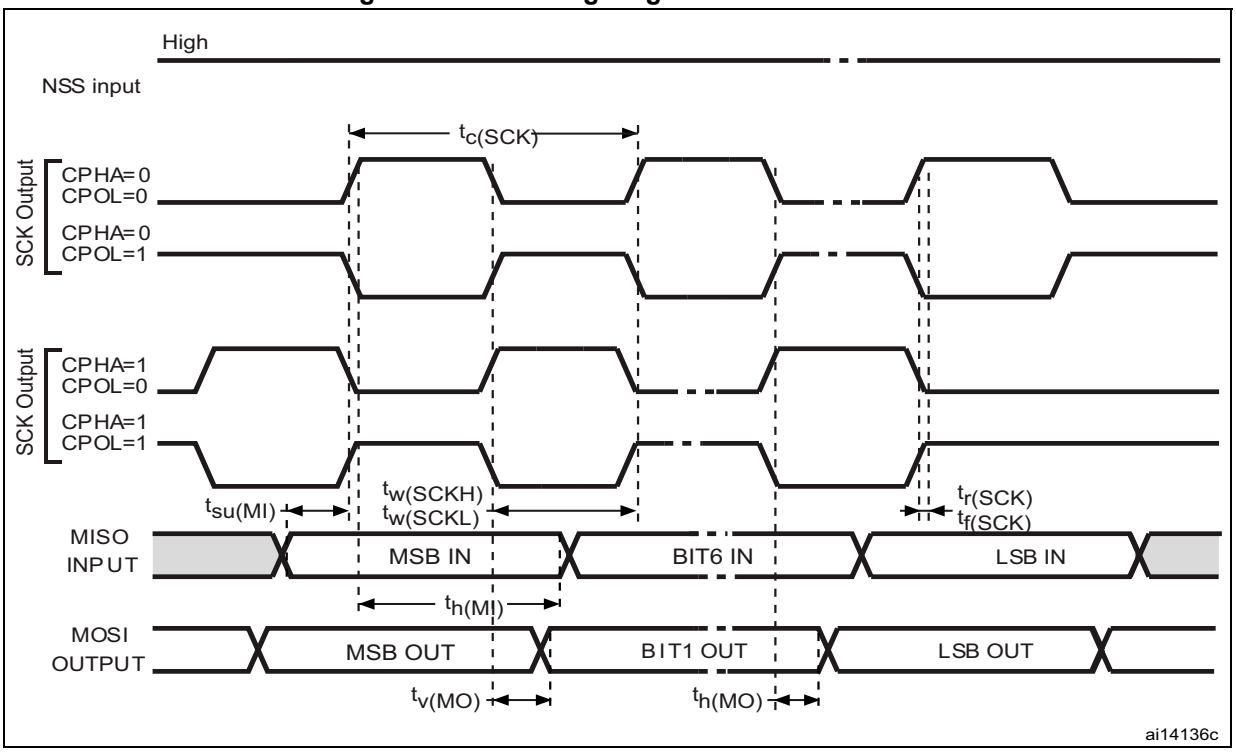


Table 39. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO}= 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO}= 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Guaranteed by characterization results

Figure 41. SPI timing diagram - master mode



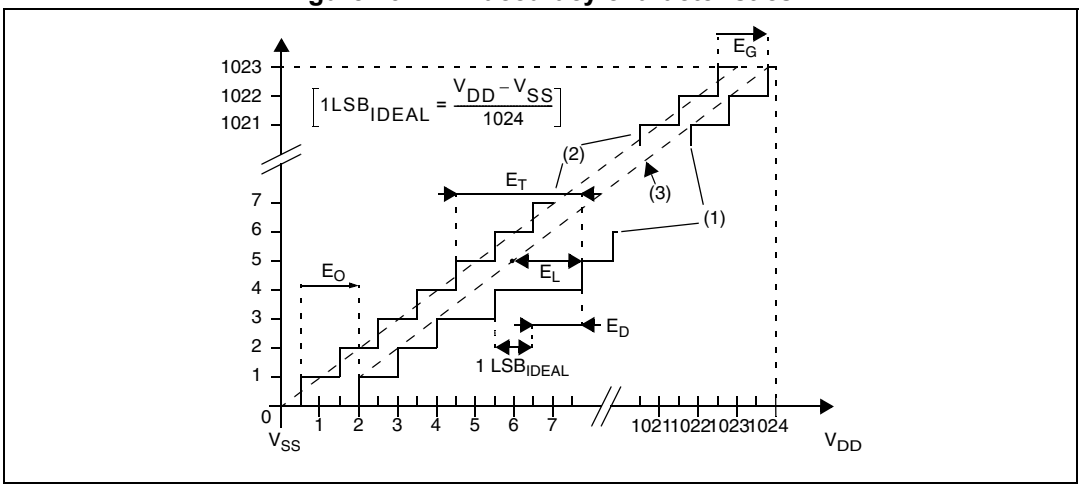
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 47. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Figure 43. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 48. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-4	4/A(1)

1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 49. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		EMI level	2.5	2.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to SD22-C101 LQFP32 package	IV	1000	

1. Guaranteed by characterization results

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

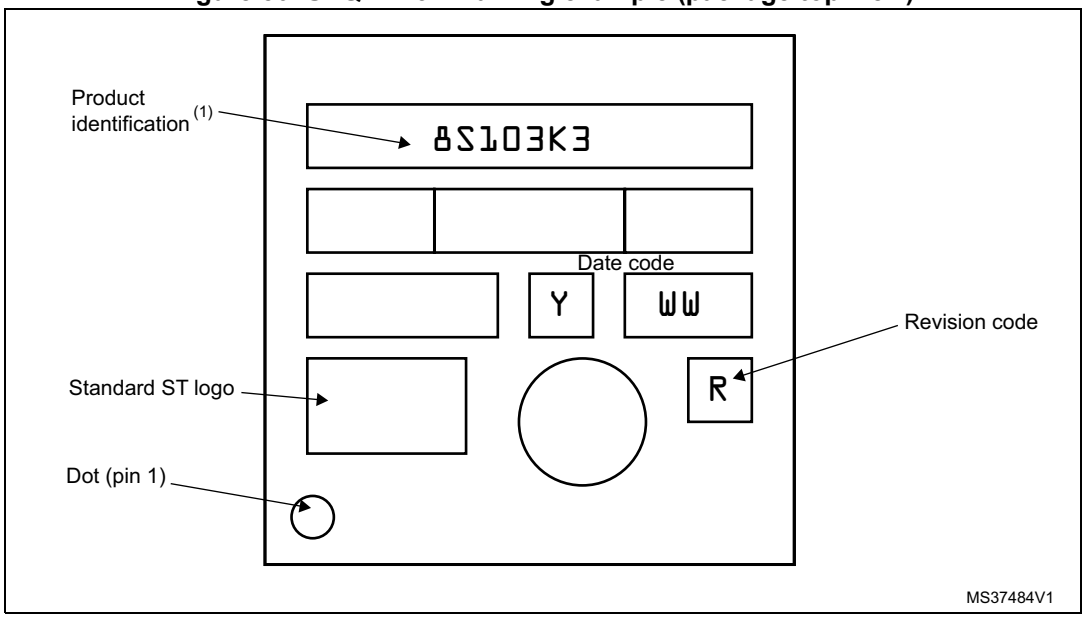
- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set
UBC, bit6	[ ] 0: Reset [ ] 1: Set
UBC, bit7	[ ] 0: Reset [ ] 1: Set

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP2 alternate function remapping for STM8S103K

Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

Table 59. Document revision history

Date	Revision	Changes
16-Oct-1999	4	Replaced VFQFPN32 package by UFQFPN32 package. – *Section 4.5: Clock controller*: replaced TIM2 and TIM3 with reserved and TIM2 respectively in *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers* – *Total current consumption in halt mode*: changed the maximum current consumption limit at 125 °C (and VDD= 5 V) from 35 µA to 55 µA. – *Functional EMS (electromagnetic susceptibility)*: renamed ESD as FESD (functional); added name of AN1709; replaced EC 1000 with IEC 61000. – *Designing hardened software to avoid noise problems*: replaced IEC 1000 with IEC 61000, added title of AN1015, and added footnote to EMS data table. – *Electromagnetic interference (EMI)*: replaced J 1752/3 with IEC 61967-2 and updated data of the EMI data table. – *Section 12.2: Selecting the product temperature range*: changed the value of LQFP32 7x7 mm thermal resistance from 59 °C/W to 60 °C/W. Added *Section 13.1: STM8S103 FASTROM microcontroller option list*.
22-Apr-2010	5	Added VFQFPN32 and SO20 packages. Updated Px_IDR reset value in *Table 7: I/O port hardware register map*. – *Section 10.3: Operating conditions*: updated VCAP and ESR low limit, added ESL parameter, and Note 1 below *Table 19: General operating conditions* Updated ACCHSI in *Table 34: HSI oscillator characteristics*. Modified IDD(H)inand. Removed note 3 related to Accuracy of HSI oscillator. Updated maximum power dissipation in *Table 19: General operating conditions*. Updated *Section 12: Thermal characteristics* Replaced package pitch digit by VFQFPN/UFQFPN package digit in *Figure 63: STM8S103F2/x3 access line ordering information scheme*[(1)], and removed note 1.