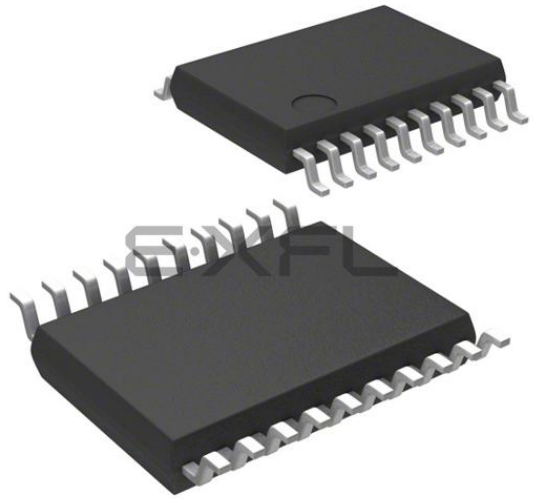

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f2p3

2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8S103F2/x3 access line features

Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

4.12 TIM4 - 8-bit basic timer

- 8-bit auto reload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complementary outputs	Ext. trigger	Timer synchronization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC1)

The STM8S103F2/x3 family products contain a 10-bit successive approximation A/D converter (ADC1) with up to 5 external multiplexed input channels and the following main features:

- Input voltage range: 0 to VDD
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

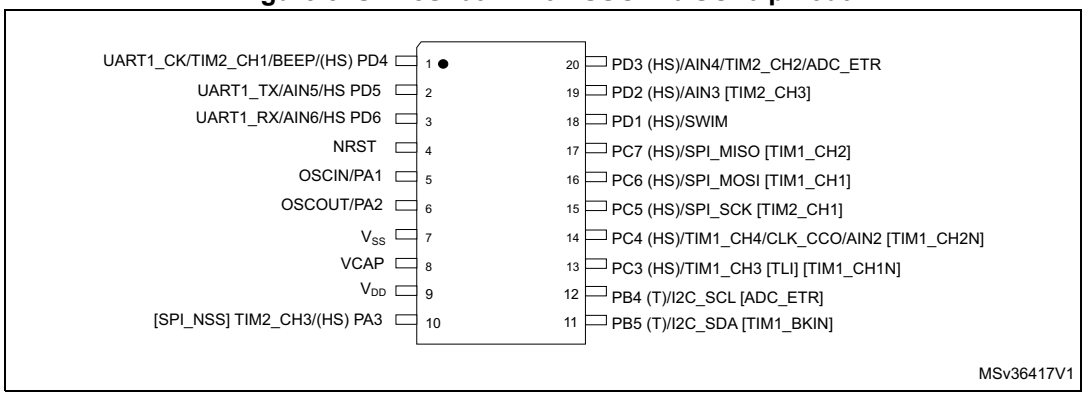
The following communication interfaces are implemented:

- UART1: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.1 master capability
- SPI: Full and half-duplex, 8 Mbit/s
- I²C: Up to 400 kbit/s

5.2 STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description

5.2.1 STM8S103F2/F3 TSSOP20/SO20 pinout

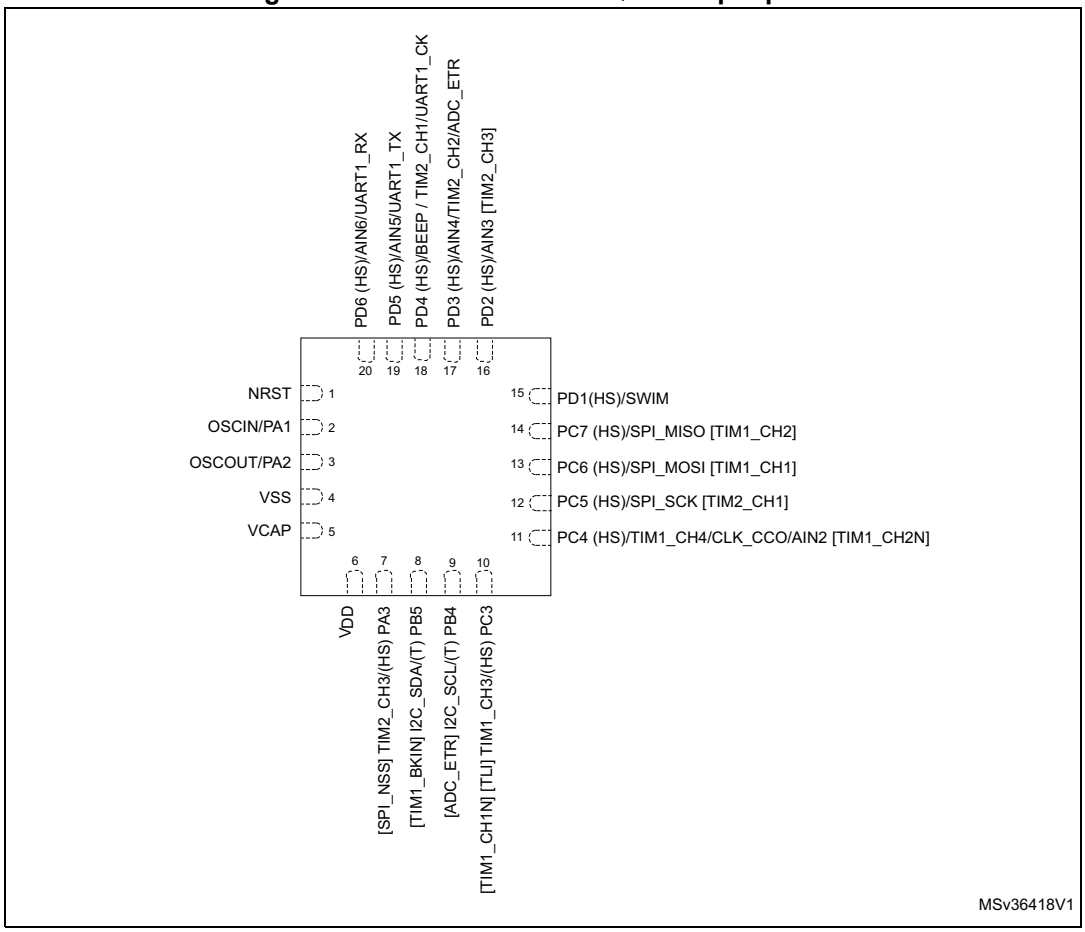
Figure 5. STM8S103F2/F3 TSSOP20/SO20 pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function)

5.2.2 STM8S103F2/F3 UFQFPN20 pinout

Figure 6. STM8S103F2/F3 UFQFPN20-pin pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

1. Depends on the external circuitry.

6.2.2 General hardware register map

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5059	Reserved area (60 byte)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 byte)			
0x00 5062	Flash	FLASH _PUKR	Flash program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 byte)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 byte)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

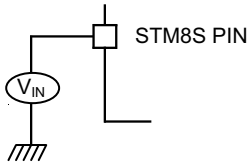
The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 15. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4865	X co-ordinate on the wafer	U_ID[7:0]							
0x4866		U_ID[15:8]							
0x4867	Y co-ordinate on the wafer	U_ID[23:16]							
0x4868		U_ID[31:24]							
0x4869	Wafer number	U_ID[39:32]							
0x486A	Lot number	U_ID[47:40]							
0x486B		U_ID[55:48]							
0x486C		U_ID[63:56]							
0x486D		U_ID[71:64]							
0x486E		U_ID[79:72]							
0x486F		U_ID[87:80]							
0x4870		U_ID[95:88]							

Figure 9. Pin input voltage



MSv36481V1

10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics* and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and a functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

The device's mission profile (application conditions) is compliant with the JEDEC JESD47 Qualification Standard, the extended mission profiles are available on demand.

Table 16. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 87*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. This pin must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 17. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	

Total current consumption in wait mode

Table 23. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 24. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.1	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 33. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized)(3)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

10.3.5 Memory characteristics

RAM and hardware registers

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Section 10.3: Operating conditions* for the value of V_{IT-max}.

Flash program memory/data EEPROM memory

Table 37. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU}≤ 16 MHz	2.95	-	5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte)	-	-	6	6.6	ms
	Fast programming time for 1 block (64 byte)	-	-	3	3.33	
t_{erase}	Erase time for 1 block (64 byte)	-	-	3	3.33	
N_{RW}	Erase/write cycles (program memory)(2)	T_A = +85 °C	100k	-	-	cycle
	Erase/write cycles (data memory)(2)	T_A = +125 °C	300k	1M	-	
t_{RET}	Data retention (program and data memory) after 10k erase/write cycles at T_A= +55 °C	T_{RET} = 55 °C	20	-	-	year
	Data retention (data memory) after 300k erase/write cycles at T_A= +125°C	T_{RET} = 85 °C	1	-	-	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 byte)	-	-	2	-	mA

1. Guaranteed by characterization results.
2. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

10.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 45. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD}= 2.95 to 5.5 V	1	-	4	MHz
		V_{DD}= 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4 MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7.0	-	µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
		-	14			$1/f_{ADC}$

1. During the sample time, the sampling capacitance, C_{AIN} (3 pF max), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 48. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-4	4/A(1)

1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

11.4 SDIP32 package information

Figure 54. SDIP32 package outline

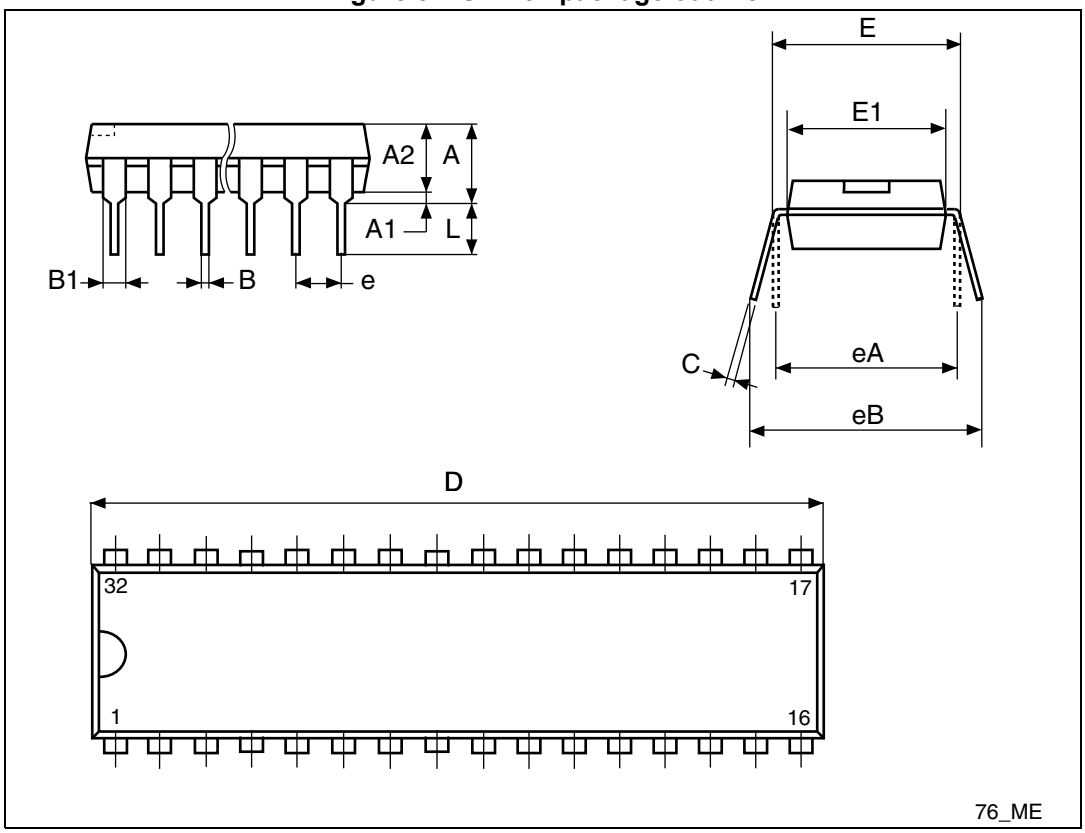


Table 55. SDIP32 package mechanical data

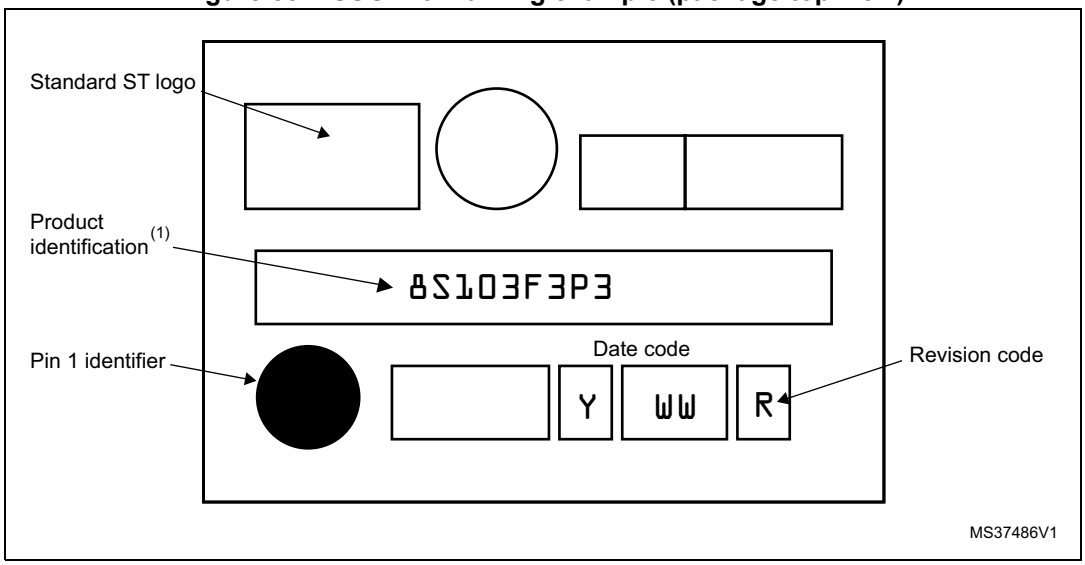
Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.556	3.759	5.080	0.1400	0.1480	0.2000
A1	0.508	-	-	0.0200	-	-
A2	3.048	3.556	4.572	0.1200	0.1400	0.1800
B	0.356	0.457	0.584	0.0140	0.0180	0.0230
B1	0.762	1.016	1.397	0.0300	0.0400	0.0550
C	0.203	0.254	0.356	0.0079	0.0100	0.0140
D	27.430	27.940	28.450	1.0799	1.1000	1.1201
E	9.906	10.410	11.050	0.3900	0.4098	0.4350
E1	7.620	8.890	9.398	0.3000	0.3500	0.3700
e	-	1.778	-	-	0.0700	-
eA	-	10.160	-	-	0.4000	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 58. TSSOP20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for the STM8 programming.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 59. Document revision history

Date	Revision	Changes
16-Oct-1999	4	Replaced VFQFPN32 package by UFQFPN32 package. – *Section 4.5: Clock controller*: replaced TIM2 and TIM3 with reserved and TIM2 respectively in *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers* – *Total current consumption in halt mode*: changed the maximum current consumption limit at 125 °C (and VDD= 5 V) from 35 µA to 55 µA. – *Functional EMS (electromagnetic susceptibility)*: renamed ESD as FESD (functional); added name of AN1709; replaced EC 1000 with IEC 61000. – *Designing hardened software to avoid noise problems*: replaced IEC 1000 with IEC 61000, added title of AN1015, and added footnote to EMS data table. – *Electromagnetic interference (EMI)*: replaced J 1752/3 with IEC 61967-2 and updated data of the EMI data table. – *Section 12.2: Selecting the product temperature range*: changed the value of LQFP32 7x7 mm thermal resistance from 59 °C/W to 60 °C/W. Added *Section 13.1: STM8S103 FASTROM microcontroller option list*.
22-Apr-2010	5	Added VFQFPN32 and SO20 packages. Updated Px_IDR reset value in *Table 7: I/O port hardware register map*. – *Section 10.3: Operating conditions*: updated VCAP and ESR low limit, added ESL parameter, and Note 1 below *Table 19: General operating conditions* Updated ACCHSI in *Table 34: HSI oscillator characteristics*. Modified IDD(H)inand. Removed note 3 related to Accuracy of HSI oscillator. Updated maximum power dissipation in *Table 19: General operating conditions*. Updated *Section 12: Thermal characteristics* Replaced package pitch digit by VFQFPN/UFQFPN package digit in *Figure 63: STM8S103F2/x3 access line ordering information scheme*[(1)], and removed note 1.

Table 59. Document revision history

Date	Revision	Changes
03-Oct-2016	13	Updated: – Name of “LQFP32 package” to “LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package” on *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 46: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint* – *Section 10.2: Absolute maximum ratings* – *Section 10.3.10: 10-bit ADC characteristics* – *Figure 40: SPI timing diagram where slave mode and CPHA = 1* – *Figure 41: SPI timing diagram - master mode* – *Figure 43: ADC accuracy characteristics* – *Figure 63: STM8S103F2/x3 access line ordering information scheme*(1): corrected package name from VFQFPN to UFQFPN – *Table 8: General hardware register map* – *Table 16: Voltage characteristics* – *Table 17: Current characteristics* – *Table 19: General operating conditions* – *Table 20: Operating conditions at power-up/power-down* – *Table 21: Total current consumption with code execution in run mode at V_{DD} = 5 V* – *Table 31: Peripheral current consumption* – *Table 49: EMI data* – Updated footnotes on *Table 18: Thermal characteristics*, *Table 38: I/O static characteristics*, *Table 43: SPI characteristics*, *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline*, *Figure 48: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*. – Updated all the “Device marking” sections on *Section 11: Package information*
13-Feb-2017	14	Updated: – *Section 10.2: Absolute maximum ratings* – *Section 11.3: UFQFPN20 package information* – *Table 5: STM8S103K3 pin descriptions* – *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* – *Table 21: Total current consumption with code execution in run mode at V_{DD} = 5 V* – Footnotes in all tables of *Section 10: Electrical characteristics* Added: – *Figure 52: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint*