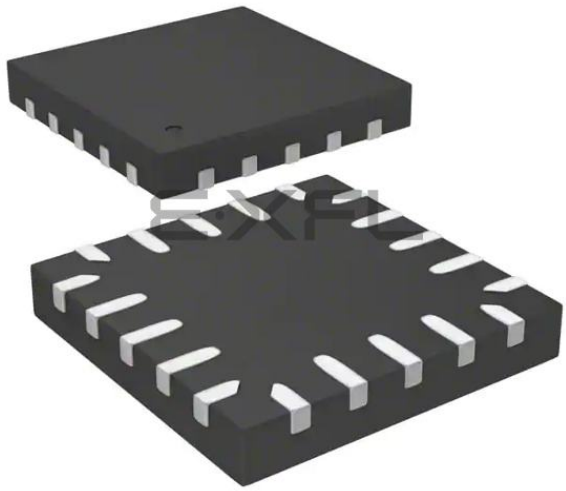

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f2u6tr

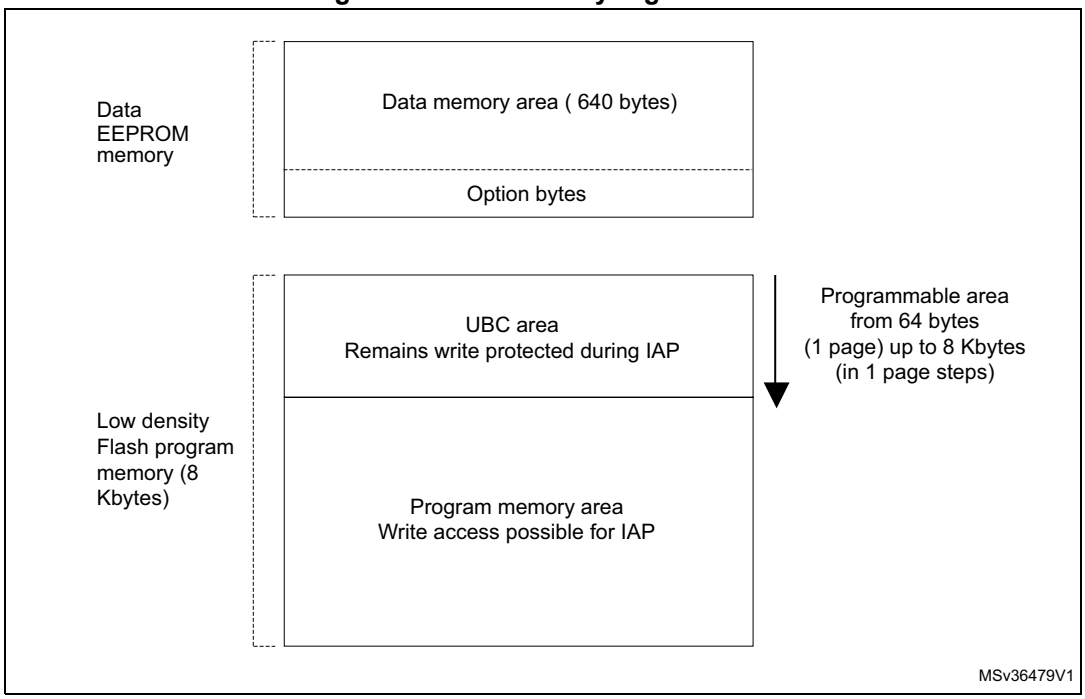
List of tables

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

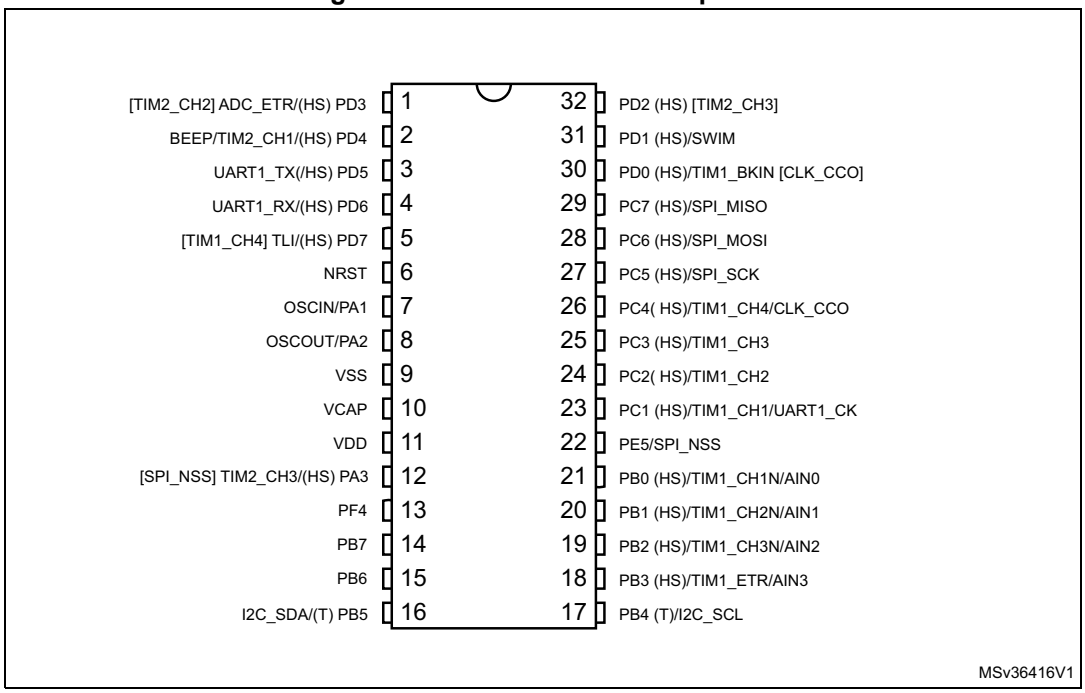
Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Figure 4. STM8S103K3 SDIP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S103K3 pin descriptions

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
6	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
7	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
8	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
9	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
10	5	VCAP	S	-	-	-	-	-	-		1.8 V regulator capacitor		-
11	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
12	7	PA3/ TIM2_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
13	8	PF4	I/O	**X**	X	-	-	O1	X	X	Port F4	-	-
14	9	PB7	I/O	**X**	X	X	-	O1	X	X	Port B7	-	-

Table 5. STM8S103K3 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
15	10	PB6	I/O	**X**	X	X	-	O1	X	X	Port B6	-	-
16	11	PB5/ I2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	-
17	12	PB4/ I2C_SCL	I/O	**X**	-	X	-	O1	T	-	Port B4	I2C clock	-
18	13	PB3/AIN3/ TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	Port B3	Analog input 3/ Timer 1 external trigger	-
19	14	PB2/AIN2/ TIM1_CH3N	I/O	**X**	X	X	HS	O3	X	X	Port B2	Analog input 2/ Timer 1 - inverted channel 3	-
20	15	PB1/AIN1/ TIM1_CH2N	I/O	**X**	X	X	HS	O3	X	X	Port B1	Analog input 1/ Timer 1 - inverted channel 2	-
21	16	PB0/AIN0/ TIM1_CH1N	I/O	**X**	X	X	HS	O3	X	X	Port B0	Analog input 0/ Timer 1 - inverted channel 1	-
22	17	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	Port E5	SPI master/slave select	-
23	18	PC1/ TIM1_CH1/ UART1_CK	I/O	**X**	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 UART1 clock	-
24	19	PC2/ TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	Port C2	Timer 1 - channel 2	-
25	20	PC3/ TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
26	21	PC4/ TIM1_CH4/ CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	-
27	22	PC5/ SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	-
28	23	PC6/ SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

Table 14. STM8S103Fx alternate function remapping bits for 20-pin devices

Option byte no.	Description
OPT2	**AFR7** Alternate function remapping option 7 0: AFR7 remapping option inactive: Default alternate functions.(1) 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N.
	AFR6 Alternate function remapping option 6 Reserved.
	AFR5 Alternate function remapping option 5 Reserved.
	AFR4 Alternate function remapping options 4:2 0: AFR4 remapping option inactive: Default alternate functions.(1) 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.
	AFR3 Alternate function remapping option 3 0: AFR3 remapping option inactive: Default alternate function.(1) 1: Port C3 alternate function = TLI.
	AFR2 Alternate function remapping option 2 Reserved
	AFR1 Alternate function remapping option 1(2) 0: AFR1 remapping option inactive: Default alternate functions.(1) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3.
	AFR0 Alternate function remapping option 0 0: AFR0 remapping option inactive: Default alternate functions.(1) 1: Port C5 alternate function = TIM2_CH1; port C6 alternate function = TIM1_CH1; port C7 alternate function = TIM1_CH2.

1. Refer to pinout description.
2. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

Table 19. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D(3)	Power dissipation at T_A = 125 °C for suffix 3	TSSOP20	-	59	mW
		SO20W	-	55	
		UFQFPN20	-	55	
		LQFP32	-	83	
		UFQFPN32	-	132	
		SDIP32	-	83	
T_A	Ambient temperature for suffix 6 version	Maximum power dissipation	-40	85	°C
T_A	Ambient temperature for suffix 3 version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version	-40	130	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax}- T_A)/\Theta_{JA}$ (see *Section 12: Thermal characteristics*) with the value for T_{Jmax} given in the previous table and the value for Θ_{JA} given in *Section 12: Thermal characteristics*

Figure 10. f_{CPUmax} versus V_{DD}

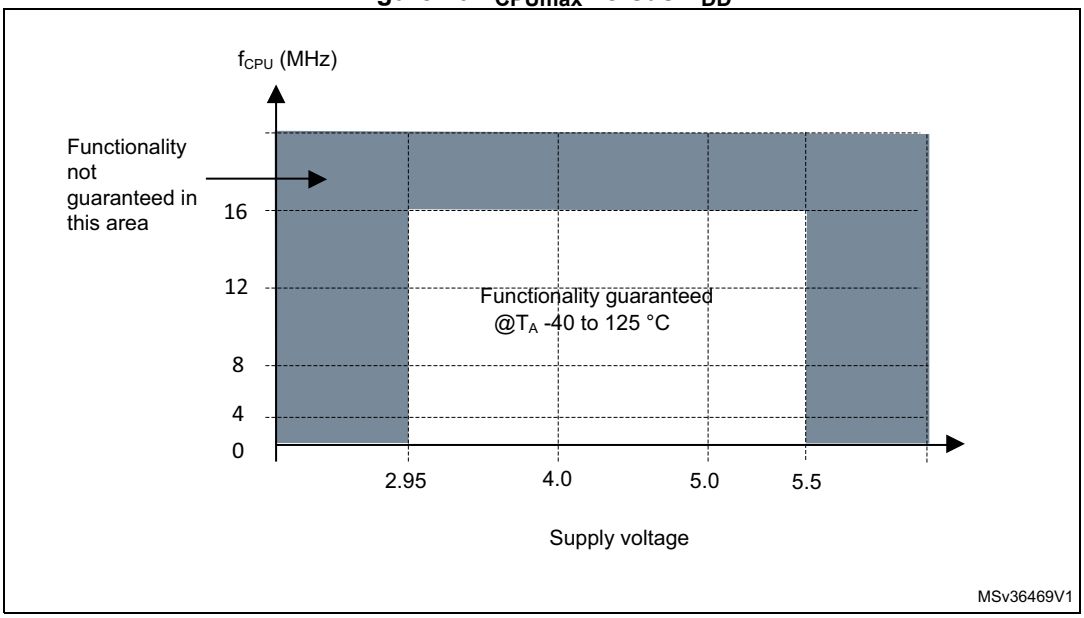


Table 20. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	∞	µs/V
	V_{DD} fall time rate(1)	-	2	-	∞	

10.3.3 External clock sources and timing characteristics

HSE user external clock

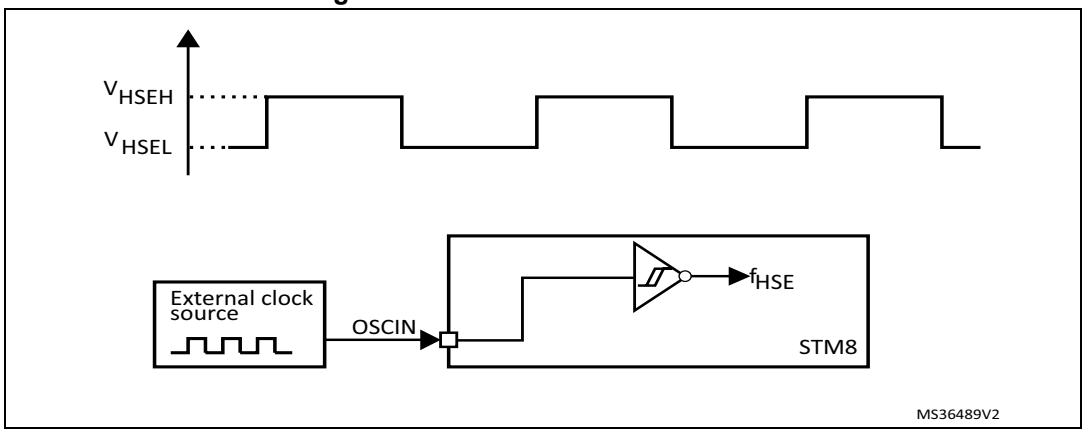
Subject to general operating conditions for V_{DD} and T_A.

Table 32. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source



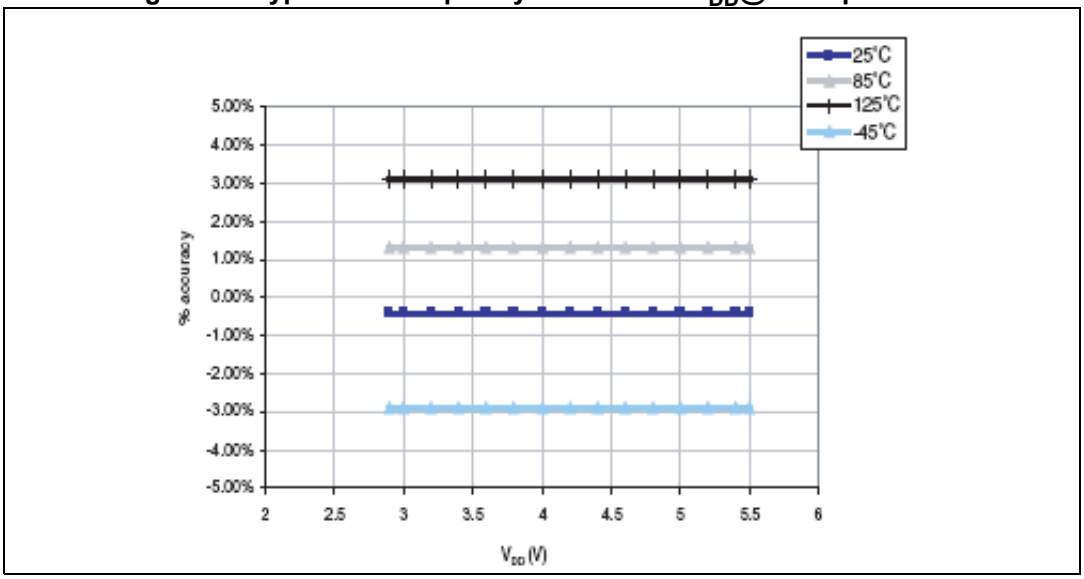
Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 35. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110	128	150	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7	µs
IDD(LSI)	LSI oscillator power consumption	-	-	5	-	µA

Figure 21. Typical LSI frequency variation vs V_{DD}@ 4 temperatures



10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 35. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

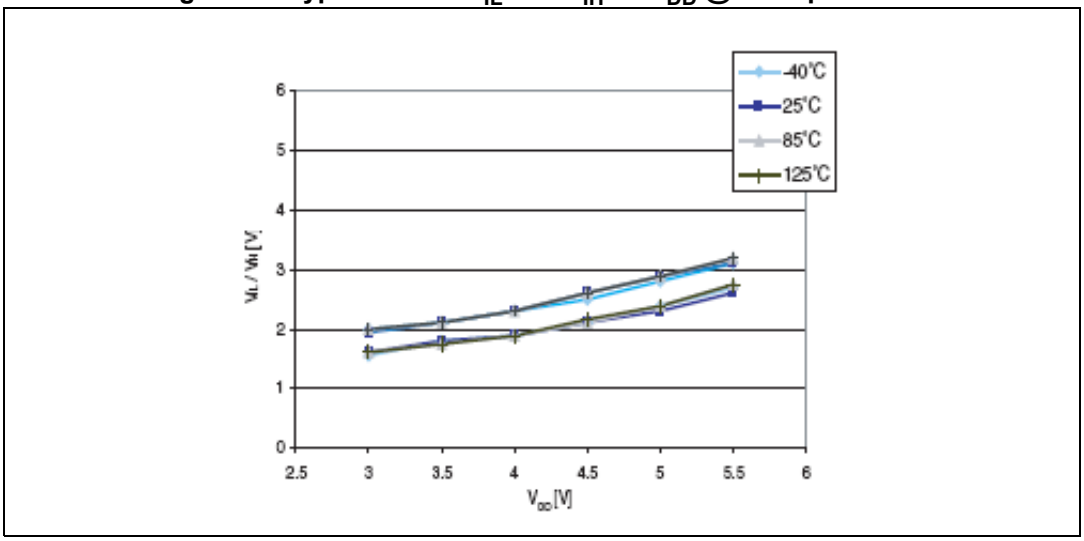


Figure 36. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

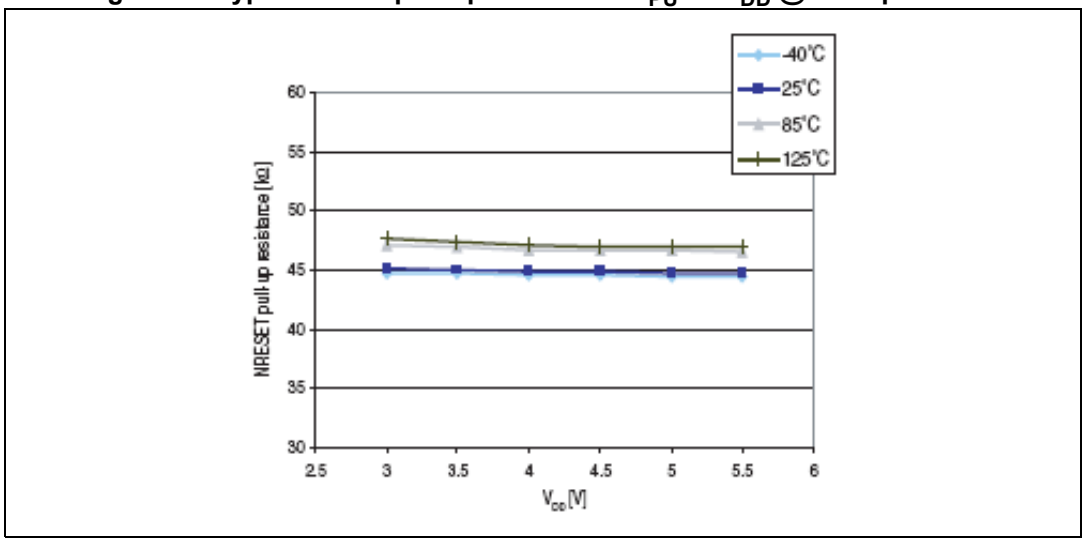
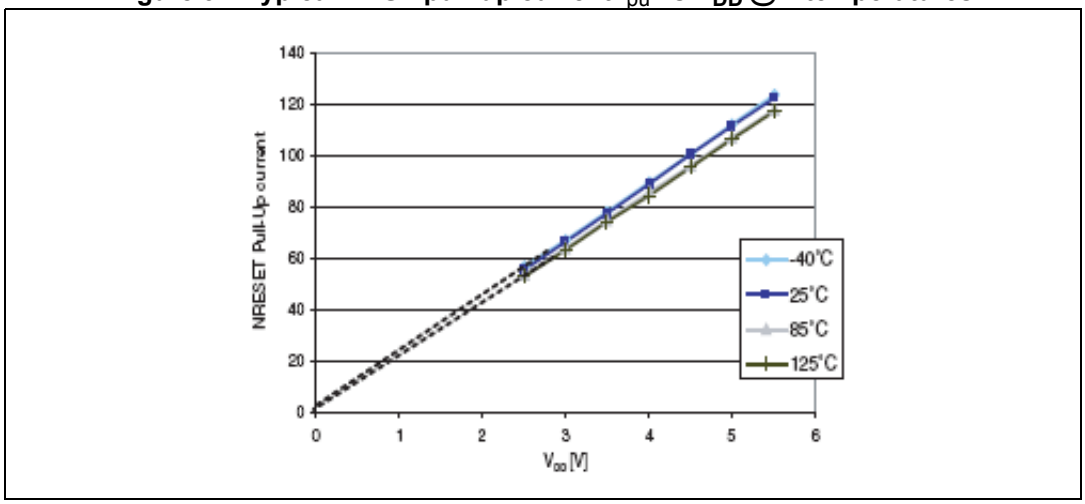


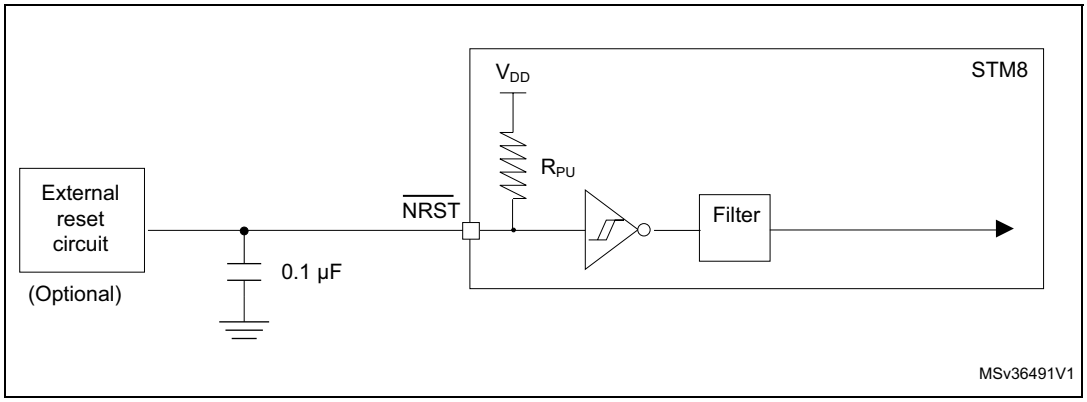
Figure 37. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 42: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.

Figure 38. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI characteristics

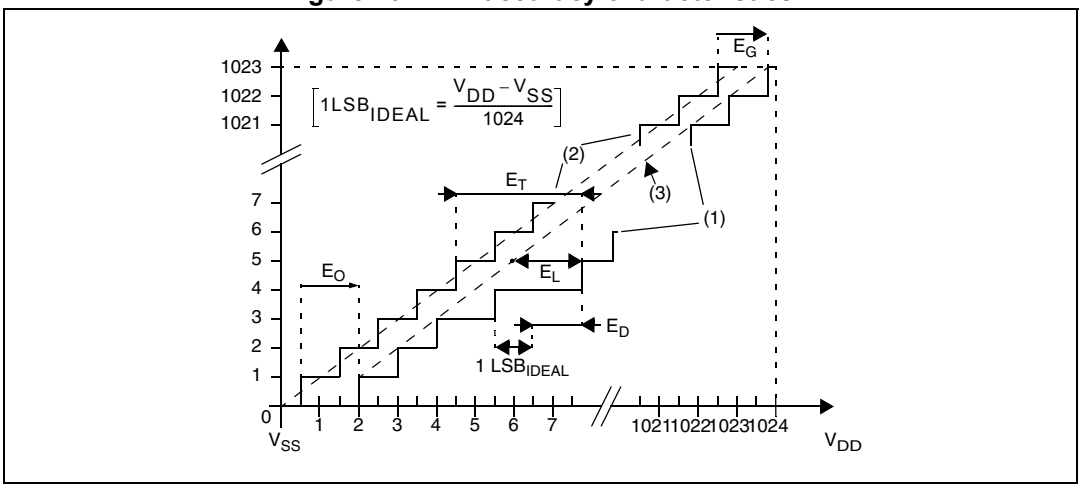
Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	7	

Table 47. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

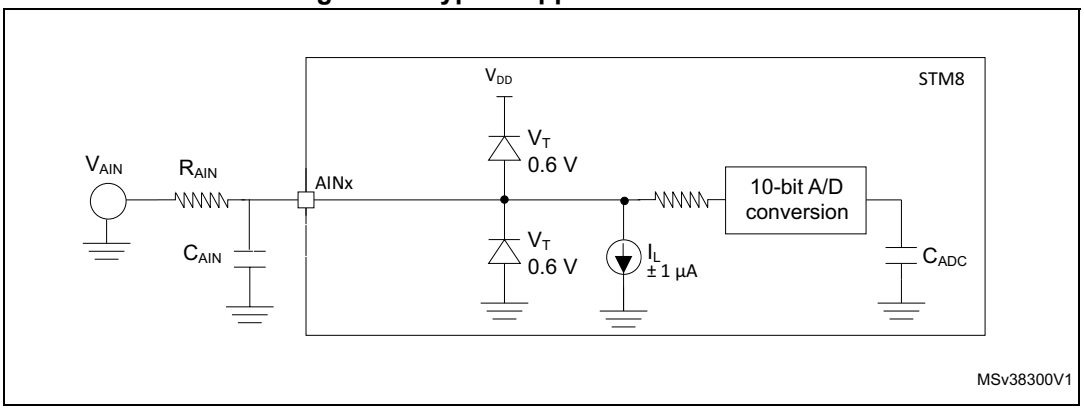
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Figure 43. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 44. Typical application with ADC



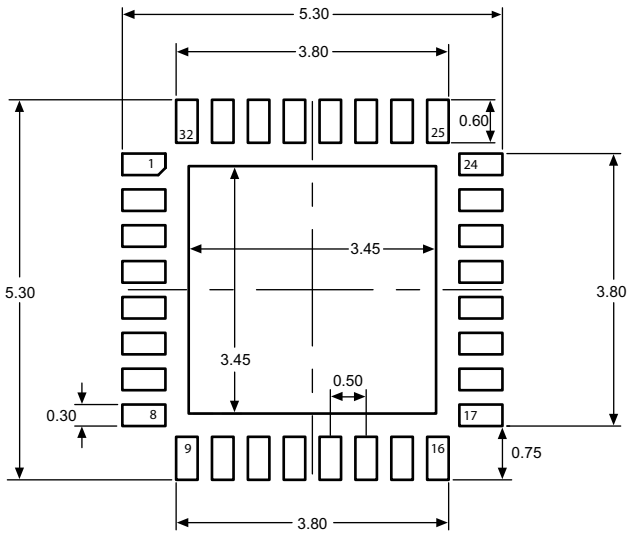
1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

Table 53. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. UFQFPN32 - 32-pin, 5 x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Section 11.7: UFQFPN recommended footprint shows the recommended footprints for UFQFPN with and without on-board emulation.

11.4 SDIP32 package information

Figure 54. SDIP32 package outline

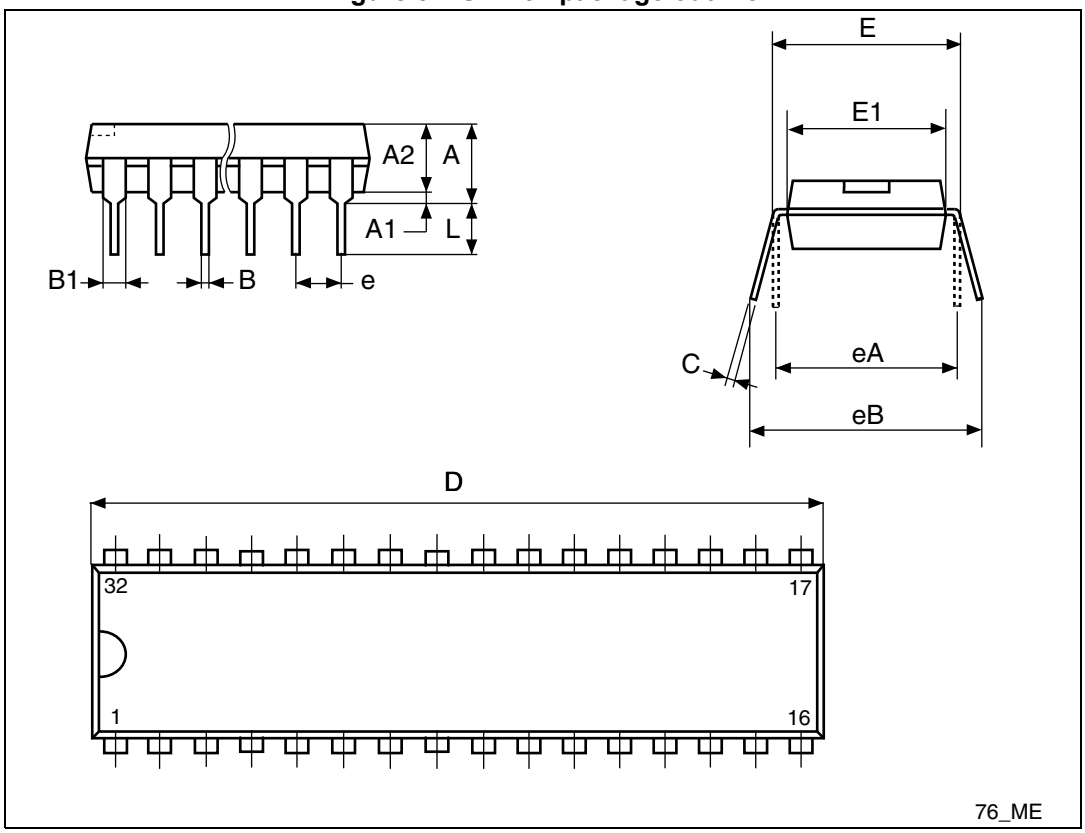


Table 55. SDIP32 package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.556	3.759	5.080	0.1400	0.1480	0.2000
A1	0.508	-	-	0.0200	-	-
A2	3.048	3.556	4.572	0.1200	0.1400	0.1800
B	0.356	0.457	0.584	0.0140	0.0180	0.0230
B1	0.762	1.016	1.397	0.0300	0.0400	0.0550
C	0.203	0.254	0.356	0.0079	0.0100	0.0140
D	27.430	27.940	28.450	1.0799	1.1000	1.1201
E	9.906	10.410	11.050	0.3900	0.4098	0.4350
E1	7.620	8.890	9.398	0.3000	0.3500	0.3700
e	-	1.778	-	-	0.0700	-
eA	-	10.160	-	-	0.4000	-

Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set
UBC, bit6	[ ] 0: Reset [ ] 1: Set
UBC, bit7	[ ] 0: Reset [ ] 1: Set

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP2 alternate function remapping for STM8S103K

Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....
Date:	.....
Signature:	.....

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

Table 59. Document revision history

Date	Revision	Changes
09-Sep-2010	6	Removed VFQFPN32 package. Removed internal reference voltage from *Section 4.13: Analog-to-digital converter (ADC1)*. Updated the reset state information in *Table 4: Legend/abbreviations for pin description tables* in *Section 5: Pinout and pin description*. Added footnote to PD1/SWIM pin in *Table 5: STM8S103K3 pin descriptions*. Updated pins 14 and 19 (TSSOP20/SO20) / pins 11 and 16 (UFQFPN20) in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions*. Standardized all reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*. Updated AFR2 description of OPT 2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*s. Replaced 0.01 µF with 0.1 µf in *Figure 38: Recommended reset pin protection*. Added *Figure 42: Typical application with I^2C bus and timing diagram* and *Table 44: I^2C characteristics*. Updated footnote 1 in *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated the Special marking section in *Section 13.1: STM8S103 FASTROM microcontroller option list*: Updated AFR2 description of OTP2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices* Updated existing footnote and added three additional footnotes to *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*
12-Jul-2011	7	Updated the note related to true open-drain outputs in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* Removed CLK_CANCCR register from *Table 8: General hardware register map*. Added note for Px_IDR registers in *Table 7: I/O port hardware register map*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 38: Recommended reset pin protection*. Removed typical HSI accuracy curve in *Section 10.3.4: Internal clock sources and timing characteristics*. Renamed package type 2 into package pitch and added pitch code “C” in *Figure 63: STM8S103F2/x3 access line ordering information scheme(1)* and added UFQFPN20 in *Section 13.1: STM8S103 FASTROM microcontroller option list*. Updated the disclaimer.