_____STMicroelectronics - <u>STM8S103F3M6TR Datasheet</u>





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 × 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f3m6tr

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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4.14.1 UART1

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (fCPU/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
 - Address bit (MSB)
 - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (fCPU/16)

LIN master mode

- Emission: Generates 13-bit synch. break frame
- Reception: Detects 11-bit break frame

4.14.2 SPI

- Maximum speed: 8 Mbit/s (fMASTER/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin



5.1 STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description

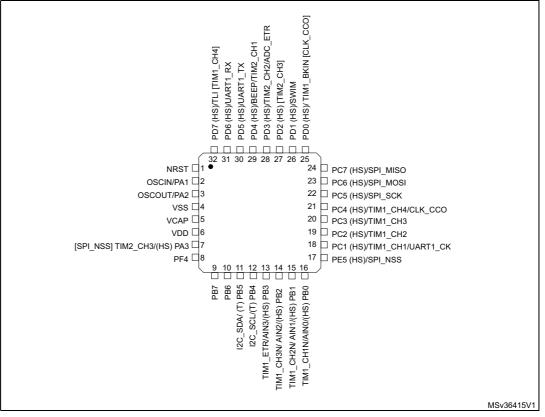


Figure 3. STM8S103K3 UFQFPN32/LQFP32 pinout

1. (HS) high sink capability.

2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).

3. [] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).



STM8S103F2 STM8S103F3 STM8S103K3

[TIM2_CH2] ADC_ETR/(HS) PD3	1	32 PD2 (HS) [TIM2_CH3]
BEEP/TIM2_CH1/(HS) PD4	2	31] PD1 (HS)/SWIM
UART1_TX(/HS) PD5	3	
UART1_RX/(HS) PD6	4	29 D PC7 (HS)/SPI_MISO
[TIM1_CH4] TLI/(HS) PD7	5	28 PC6 (HS)/SPI_MOSI
NRST	6	27 D PC5 (HS)/SPI_SCK
OSCIN/PA1	7	26 PC4(HS)/TIM1_CH4/CLK_CCO
OSCOUT/PA2	8	25 рсз (нѕ)/тім1_снз
VSS	9	24 PC2(HS)/TIM1_CH2
VCAP	10	23 D PC1 (HS)/TIM1_CH1/UART1_CK
VDD	11	22 PE5/SPI_NSS
[SPI_NSS] TIM2_CH3/(HS) PA3	12	21] рво (нs)/тім1_сн1N/АІN0
PF4	13	20] рв1 (нs)/тім1_сн2N/АіN1
PB7	14	19] рв2 (нѕ)/тім1_снзм/аім2
PB6	15	18 🗍 РВЗ (HS)/ТІМ1_ЕТК/АІNЗ
I2C_SDA/(T) PB5	16	17] PB4 (T)/I2C_SCL
		MSv36416V1

Figure 4. STM8S103K3 SDIP32 pinout

1. (HS) high sink capability.

2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).

3. [] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

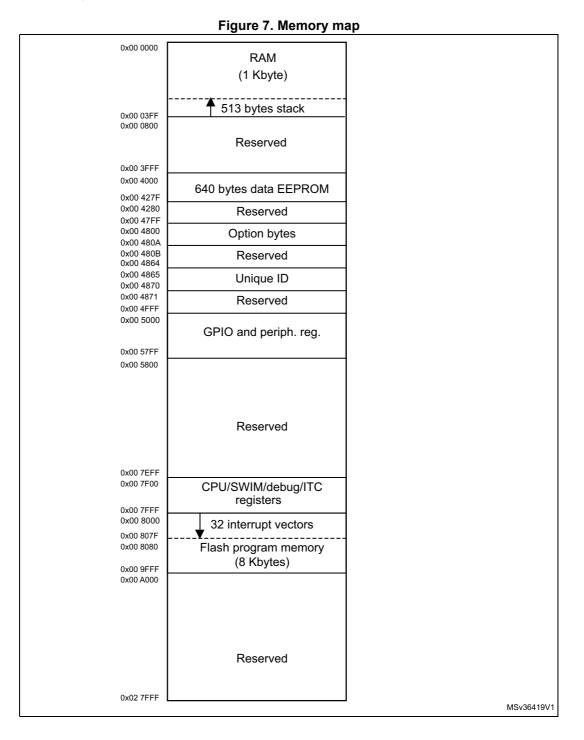
					Input			Out	put		_		<u>_</u>
	°32				mput			Out	ւթու		50	ate	
SDIP32	LQFP/ UFQFP32	Pin name	Type	floating	ndm	Ext. interrupt	High sink ⁽¹⁾	Speed	ao	dd	Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
6	1	NRST	I/O	-	Х	-	-	-	-	-	Re	eset	-
7	2	PA1/ OSCIN ⁽²⁾	I/O	x	х	х	-	01	х	х	Port A1	Resonator/ crystal in	-
8	3	PA2/ OSCOUT	I/O	x	х	х	-	01	х	х	Port A2	Resonator/ crystal out	-
9	4	VSS	S	-	-	-	-	-	-	-	Digita	l ground	-
10	5	VCAP	S	-	-	-	-	-	-		1.8 V regula	ator capacitor	-
11	6	VDD	S	-	-	-	-	-	-	-	Digital po	ower supply	-
12	7	PA3/ TIM2_CH3 [SPI_NSS]	I/O	x	х	x	HS	O3	х	x	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
13	8	PF4	I/O	X	Х	-	-	01	Х	Х	Port F4	-	-
14	9	PB7	I/O	X	Х	Х	-	01	Х	Х	Port B7	-	-

Table 5.	STM8S103K3	pin	descriptions
	0111100100100	PIII	accomptions



6 Memory and register map

6.1 Memory map





AddressBlockRegister labelRegister nameRest status0x00 50C3			eral hardware regist		
0x00 50C4CLK_SWRClock master switch register0xE10x00 50C5CLK_SWRClock switch control register0xXX0x00 50C6CLK_CKDIVRClock divider register0x180x00 50C7CLK_CCRPeripheral clock gating register0x0FF0x00 50C8CLK_CCRClock security system register0x000x00 50C9CLK_CCCRConfigurable clock control register0x000x00 50C4CLK_CCCRConfigurable clock control register0x000x00 50C6CLK_PCKENR2Peripheral clock gating register0x000x00 50CDCLK_SWIMCCRSWIM clock control register0x000x00 50C1WWD6SWIM clock control register0x7F0x00 50D1WWD6WWD6_CRWWDG control register0x7F0x00 50D2WWD6WWD6_RWRWWDR window register0x7F0x00 50D3 to 00 50DFReserved area (13 byte)0x000x0X0x00 50E1IWD6IWD6_RRIWD6 key register0x2X ⁽²⁾ 0x00 50F1IWD6IWD6_RRIWD6 precaler register0x000x00 50F2AWU_CSR1AWU control/status register0x030x00 50F3BEEPAWU_APRAWU asynchronous prescaler buffer register0x3F0x00 50F4AWU_SPI_CR2SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 50C4SPI_CR2SPI control register0x00 <th>Address</th> <th>Block</th> <th>Register label</th> <th>Register name</th> <th>Reset status</th>	Address	Block	Register label	Register name	Reset status
0x00 50C5CLK_SWCRClock switch control register0xXX0x00 50C6CLK_CKDIVRClock divider register0x180x00 50C7CLK_CCSRClock security system register0x000x00 50C8CLK_CSSRClock security system register0x000x00 50C9CLK_CCCRConfigurable clock control register0x000x00 50CACLK_PCKENR2Peripheral clock gating register0x0FF0x00 50CACLK_PCKENR2Peripheral clock gating register0x0F0x00 50CDCLK_SWIMCCRSWIM clock control register0x000x00 50CDCLK_SWIMCCRSWIM clock control register0x7F0x00 50C1WWDGWWDG_CRWWDG control register0x7F0x00 50D1WWDGWWDG_WRWWDG control register0x7F0x00 50E0WWDG_RIWDG prescaler register0x000x00 50E1IWDGIWDG_RRIWDG prescaler register0x000x00 50E1IWDGAWU_CSR1AWU control/status register0x070x00 50F1AWUAWU_APRAWU control/status register0x030x00 50F3BEEPBEEP_CSRBEEP control/status register0x060x00 50F4VAWUSPI_CR1SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00	0x00 50C3		CLK_CMSR	Clock master status register	0xE1
0x00 50C6CLK_CKDIVRClock divider register0x180x00 50C7CLK_PCKENR1Peripheral clock gating register 10xFF0x00 50C8CLK_CSSRClock security system register0x000x00 50C9CLK_CCORConfigurable clock control register0x000x00 50CACLK_PCKENR2Peripheral clock gating register 20xFF0x00 50CCCLK_PCKENR2Peripheral clock gating register0x000x00 50CDCLK_SWIMCCRSWIM clock control register0x000x00 50CDCLK_SWIMCCRSWIM clock control register0x7F0x00 50C1WWDGWWDG_CRWWDG control register0x7F0x00 50D1WWDGWWDG_WRWWDR window register0x7F0x00 50D2WWDGReserved area (13 byte)0x000x00 50E1IWDGIWDG_RRIWDG register0x020x00 50E2IWDG_RRIWDG register0x000x00 50F1AWUAWU_CSR1AWU control/status register0x030x00 50F3BEEPBEEP_CSRBEEP control/status register0x010x00 50F4AWUSPI_CR1SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 502SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 50F4SPI_CR2SPI control register0x000x00 5204SPI_CR2SPI control register0x000x00 5204SPI_CR2SPI contro	0x00 50C4		CLK_SWR	Clock master switch register	0xE1
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0x00 50E3 to 0x00 50EFReserved area (13 byte)0x00 50F0AWU_CSR1AWU control/status register 10x000x00 50F1AWU_APRAWU asynchronous prescaler buffer register0x3F0x00 50F2AWU_TBRAWU timebase selection register0x000x00 50F3BEEPBEEP_CSRBEEP control/status register0x1F0x00 50F4 to 0x00 50FFVReserved area (12 byte)0x000x00 5200SPI_CR1SPI control register 10x000x00 5201SPI_CR2SPI control register 20x000x00 5202SPI_SRSPI status register0x020x00 5203SPI_DRSPI control register0x020x00 5204SPI_CRPRSPI data register0x020x00 5205SPI_CRCPRSPI CRC polynomial register0x070x00 5205SPI_RXCRCRSPI Rx CRC register0x07	0x00 50E1	IWDG	IWDG_PR	IWDG prescaler register	0x00
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0x00 50F2AWU_IBRregister0x000x00 50F3BEEPBEEP_CSRBEEP control/status register0x1F0x00 50F4 to 0x00 50FFReserved area (12 byte)0x000x00 5200\$PI_CR1SPI control register 10x000x00 5201\$PI_CR2SPI control register 20x000x00 5202\$PI_ICRSPI interrupt control register 20x000x00 5203\$PI_SRSPI status register0x020x00 5204\$PI_CRCPRSPI data register0x000x00 5205\$PI_CRCPRSPI CRC polynomial register0x070x00 5206\$PI_RXCRCRSPI Rx CRC register0xFF	0x00 50F1	AWU	AWU_APR		0x3F
0x00 50F4 to 0x00 50FF Reserved area (12 byte) 0x00 5200 \$\$PI_CR1 \$\$PI control register 1 0x00 0x00 5201 \$\$PI_CR2 \$\$PI control register 2 0x00 0x00 5202 \$\$\$PI_ICR2 \$\$\$PI interrupt control register 2 0x00 0x00 5203 \$\$\$\$PI_SR \$\$\$\$PI status register 0x02 0x00 5204 \$	0x00 50F2	WWDG	AWU_TBR		0x00
0x00 5200SPI_CR1SPI control register 10x000x00 5201SPI_CR2SPI control register 20x000x00 5202SPI_ICRSPI interrupt control register0x000x00 5203SPI_SRSPI status register0x020x00 5204SPI_DRSPI data register0x000x00 5205SPI_CRCPRSPI CRC polynomial register0x070x00 5206SPI_RXCRCRSPI Rx CRC register0xFF	0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
Ox00 5201SPI_CR2SPI control register 2Ox000x00 5202SPI_ICRSPI interrupt control register0x000x00 5203SPI_SRSPI status register0x020x00 5204SPI_DRSPI data register0x000x00 5205SPI_CRCPRSPI CRC polynomial register0x070x00 5206SPI_RXCRCRSPI Rx CRC register0xFF	0x00 50F4 to 0x00 50FF		Reser	ved area (12 byte)	
Ox00 5202 SPI_ICR SPI interrupt control register Ox00 0x00 5203 SPI_SR SPI status register 0x02 0x00 5204 SPI_DR SPI data register 0x00 0x00 5205 SPI_CRCPR SPI CRC polynomial register 0x07 0x00 5206 SPI_RXCRCR SPI Rx CRC register 0xFF	0x00 5200		SPI_CR1	SPI control register 1	0x00
Ox00 5203 SPI 0x00 5204 SPI_SR 0x00 5205 SPI_CRCPR 0x00 5206 SPI_RXCRCR	0x00 5201		SPI_CR2	SPI control register 2	0x00
SPI SPI 0x00 5204 SPI_DR 0x00 5205 SPI_CRCPR 0x00 5206 SPI_RXCRCR	0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5204 SPI_DR SPI data register 0x00 0x00 5205 SPI_CRCPR SPI CRC polynomial register 0x07 0x00 5206 SPI_RXCRCR SPI Rx CRC register 0xFF	0x00 5203	0.01	SPI_SR	SPI status register	0x02
0x00 5206 SPI_RXCRCR SPI Rx CRC register 0xFF	0x00 5204	SPI	SPI_DR	SPI data register	0x00
	0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5207 SPI_TXCRCR SPI Tx CRC register 0xFF	0x00 5206	WWDG IWDG AWU BEEP	SPI_RXCRCR	SPI Rx CRC register	0xFF
	0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF

Table 8. General hardware register map (continued)



6.2.3 CPU/SWIM/debug module/interrupt controller registers

		ebug module/interrup				
Address	Block	Register label	Register name	Reset status		
0x00 7F00		А	Accumulator	0x00		
0x00 7F01		PCE	Program counter extended	0x00		
0x00 7F02		PCH	Program counter high	0x00		
0x00 7F03		PCL	Program counter low	0x00		
0x00 7F04		ХН	X index register high	0x00		
0x00 7F05	CPU ⁽¹⁾	XL	X index register low	0x00		
0x00 7F06		YH	Y index register high	0x00		
0x00 7F07		YL	Y index register low	0x00		
0x00 7F08		SPH	Stack pointer high	0x03		
0x00 7F09		SPL	Stack pointer low	0xFF		
0x00 7F0A		CCR	Condition code register	0x28		
0x00 7F0B to 0x00 7F5F		Reserved area (85 byte)				
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00		
0x00 7F70		ITC_SPR1	Interrupt software priority register 1	0xFF		
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF		
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF		
0x00 7F73	ITC	ITC_SPR4	Interrupt software priority register 4	0xFF		
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF		
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF		
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF		
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF		
0x00 7F78 to 0x00 7F79		Reserved	area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00		
0x00 7F81 to 0x00 7F8F		Reserved	area (15 byte)			

Table 9. CPU/SWIM/debug module/interrupt controller registers



IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address			
21	Reserved	-	-	-	0x00 805C			
22	ADC1	ADC1 end of conversion/analog watchdog interrupt	-	-	0x00 8060			
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064			
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068			
	Reserved							

Table 10. Interrupt mapping (continued)

1. Except PA1.



Option byte no.	Description
OPT0	ROP[7:0] Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.
OPT1	UBC[7:0] User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected Page 0 and 1 contain the interrupt vectors. 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory write-protected <i>Note: Refer to the family reference manual (RM0016) section on Flash write</i> <i>protection for more details.</i>
OPT2	AFR[7:0] Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
	HSITRIM: High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register LSI_EN: Low speed internal clock enable
	0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
OPT3	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

Table 12. Option byte description



Symbol	Parameter	Conditi	ons	Тур	Max ⁽¹⁾	Unit
			HSE crystal osc. (16 MHz)	4.5	-	
	Supply	f _{CPU} = f _{MASTER} = 16 MHz	HSE user ext. clock (16 MHz)	4.3	4.75	
	Supply current in		HSI RC osc. (16 MHz)	3.7	4.5	
I _{DD(RUN)}	Run mode, code	f _{CPU} = f _{MASTER} = 2 MHz	HSI RC osc. (16 MHz/8) ⁽²⁾	0.84	1.05	mA
	executed	f _{CPU} = f _{MASTER} /128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
	from Flash	f _{CPU} = f _{MASTER} /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		f _{CPU} = f _{MASTER} = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V (continued)

1. Guaranteed by characterization results. Guaranteed by characterization results.

2. Default clock configuration measured with all peripherals off.

Symbol	Parameter	Conditi	ons	Тур	Max ⁽¹⁾	Unit
			HSE crystal osc. (16 MHz)	1.8	-	
		f _{CPU} = f _{MASTER} = 16 MHz	HSE crystal osc. (16 MHz) 1.8 - HSE user ext. clock (16 MHz) 2 2.35 HSI RC osc. (16 MHz) 1.5 2 HSE user ext. clock (16 MHz) 0.81 - HSE user ext. clock (16 MHz) 0.81 - HSI RC osc. (16 MHz) 0.7 0.87 HSI RC osc. (16 MHz) 0.46 0.58 LSI RC osc. (128 kHz) 0.41 0.55 HSE user ext. clock (16 MHz) 4 - HSE osc. (128 kHz) 0.41 0.55 HSE crystal osc. (16 MHz) 4 - HSE user ext. clock (16 MHz) 4.3 4.75 HSI RC osc. (16 MHz) 3.9 4.7 HSI RC osc. (16 MHz) 0.84 1.05			
	Supply current in		HSI RC osc. (16 MHz)	1.5	2	
I _{DD(RUN)}	Run mode, code	f _{CPU} = f _{MASTER} /128 = 125 kHz		0.81	-	mA
	executed from RAM		HSI RC osc. (16 MHz)	0.7	0.87	
		f _{CPU} = f _{MASTER} /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		f _{CPU} = f _{MASTER} = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
			HSE crystal osc. (16 MHz)	4	-	
	Quantu	f _{CPU} = f _{MASTER} = 16 MHz		4.3	4.75	
	Supply current in		HSI RC osc. (16 MHz)	3.9	4.7	
I _{DD(RUN)}	Run mode, code	f _{CPU} = f _{MASTER} = 2 MHz	HSI RC osc. (16 MHz/8) ⁽²⁾	0.84	1.05	mA
	executed	f _{CPU} = f _{MASTER} /128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
	from Flash	f _{CPU} = f _{MASTER} /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	- 2.35 2 - 0.87 0.58 0.55 - 4.75 4.7 1.05 0.9 0.58	
		f _{CPU} = f _{MASTER} = 128 kHz	LSI RC osc. (128 kHz)	6 MHz)1.8-22.35Hz)1.52 $(-1)^{-1}$ Hz)1.52 $(-1)^{-1}$ Hz)0.70.81-Hz)0.70.87Hz/8)0.460.58Hz)0.410.556 MHz)4- $(-1)^{-1}$ 4.34.75Hz)3.94.7Hz/8)0.460.58		

1. Guaranteed by characterization results.

2. Default clock configuration measured with all peripherals off.



10.3.3 External clock sources and timing characteristics

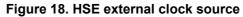
HSE user external clock

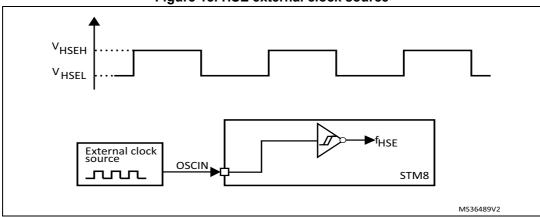
Subject to general operating conditions for V_{DD} and $T_{\text{A}}.$

Table 32	. HSE user	external	clock	characteristics
----------	------------	----------	-------	-----------------

Symbol	Parameter	Conditions	Min	Мах	Unit
f _{HSE_ext}	User external clock source frequency	-	0	16	MHz
V _{HSEH} ⁽¹⁾	OSCIN input pin high level voltage	-	0.7 x V _{DD}	V _{DD} + 0.3 V	V
V _{HSEL} ⁽¹⁾	OSCIN input pin low level voltage	-	V _{SS}	0.3 x V _{DD}	v
I _{LEAK_HSE}	OSCIN input leakage current	V_{SS} < V_{IN} < V_{DD}	-1	+1	μA

1. Guaranteed by characterization results.







HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
f _{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R _F	Feedback resistor	-	-	220	-	kΩ
C ⁽¹⁾	Recommended load capacitance ⁽²⁾	-	-	-	20	pF
1	HSE oscillator power	C = 20 pF f _{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized) ⁽³⁾	mA
IDD(HSE)	consumption	C = 10 pF f _{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized) ⁽³⁾	mA
9 _m	Oscillator transconductance	-	5	-	-	mA/V
t _{SU(HSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized	-	1	-	ms

Table	33.	HSE	oscillator	characteristics
Table	UU .		oscillator	Characteristics

1. C is approximately equivalent to 2 x crystal Cload.

2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details

3. Guaranteed by characterization results.

 t_{SU(HSE)} is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.



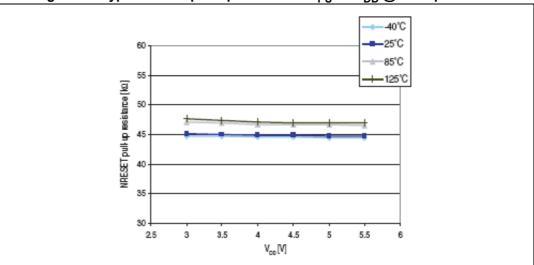
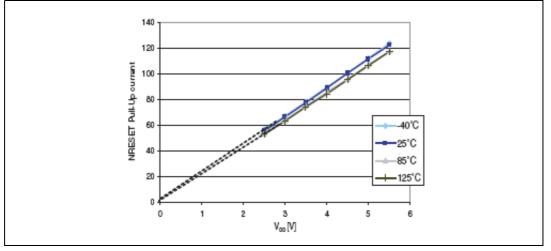


Figure 36. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

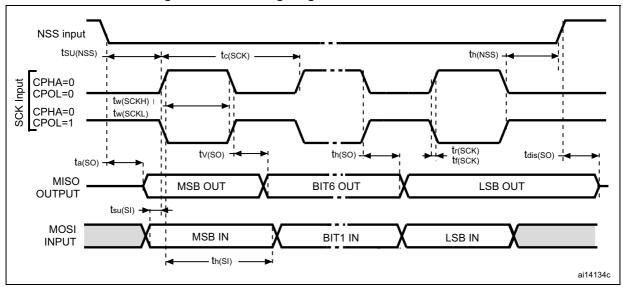
Figure 37. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures

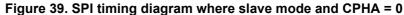


The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 42: NRST pin characteristics*), otherwise the reset is not taken into account internally.

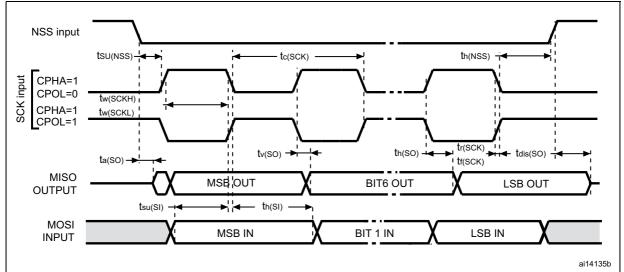
For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.







1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}





1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 $V_{\text{DD}}.$



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

11.1 LQFP32 package information

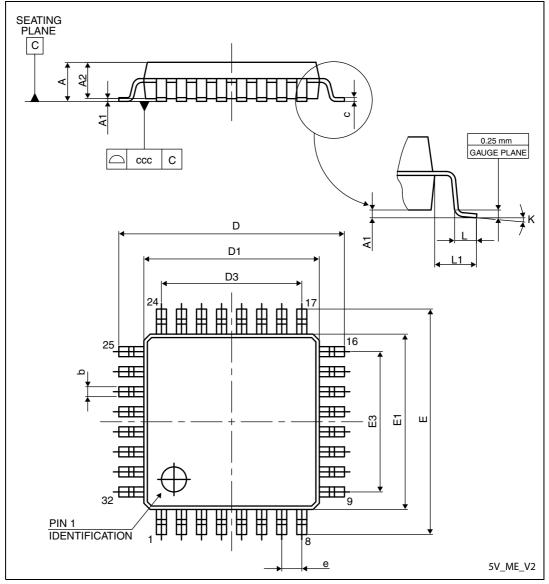


Figure 45. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline

1. Drawing is not to scale.

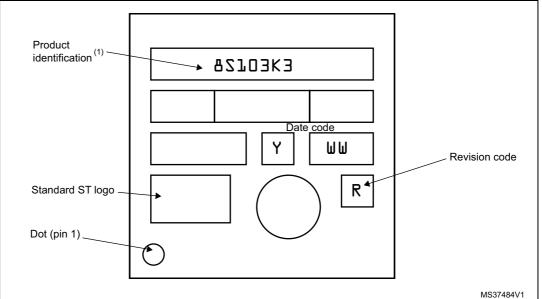


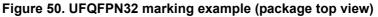
DocID15441 Rev 14

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



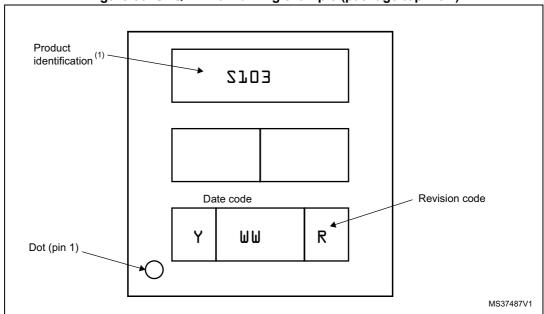


Figure 53. UFQFPN20 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

13.1 STM8S103 FASTROM microcontroller option list

(last update: April 2010)

Customer	
Address	
Contact	
Phone number	
FASTROM code reference ⁽¹⁾	

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

Device type/memory size/package (check only one option)

FASTROM device	4 Kbyte	8 Kbyte
LQFP32	-	[] STM8S103K3
UFQFPN20	[] STM8S103F2	[] STM8S103F3
UFQFPN32	-	[] STM8S103K3
TSSOP20	[] STM8S103F2	[] STM8S103F3
SO20W	[] STM8S103F2	[] STM8S103F3

Conditioning (check only one option)

[] Tape and reel or [] Tray

Special marking (check only one option)

[] No [] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

UFQFPN20: 1 line of 4 characters max: ""	
UFQFPN32: 1 line of 7 characters max: ""	
LQFP32: 2 lines of 7 characters max: "" and ""	"
TSSOP20/SO20: 1 line of 10 characters max: "	"

Three characters are reserved for code identification.



Table 59. Document revision history			
Date	Revision	Changes	
09-Sep-2010	6	Removed VFQFPN32 package. Removed internal reference voltage from Section 4.13: Analog-to- digital converter (ADC1). Updated the reset state information in Table 4: Legend/abbreviations for pin description tables in Section 5: Pinout and pin description. Added footnote to PD1/SWIM pin in Table 5: STM8S103K3 pin descriptions. Updated pins 14 and 19 (TSSOP20/SO20) / pins 11 and 16 (UFQFPN20) in Table 6: STM8S103F2 and STM8S103F3 pin descriptions. Standardized all reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in Table 8: General hardware register map. Updated AFR2 description of OPT 2 in Table 14: STM8S103Fx alternate function remapping bits for 20-pin devicess. Replaced 0.01 µF with 0.1 µf in Figure 38: Recommended reset pin protection. Added Figure 42: Typical application with I ² C bus and timing diagram and Table 44: I ² C characteristics. Updated footnote 1 in Table 46: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = 5 \text{ V}$ and Table 47: ADC accuracy with $R_{AIN} < 10 \text{ kQ}$ $V_{DD} = $	
12-Jul-2011	7	Updated the note related to true open-drain outputs in <i>Table 6:</i> <i>STM8S103F2 and STM8S103F3 pin descriptions</i> Removed CLK_CANCCR register from <i>Table 8: General hardware</i> <i>register map.</i> Added note for Px_IDR registers in <i>Table 7: I/O port hardware register</i> <i>map.</i> Added recommendation concerning NRST pin level, and power consumption sensitive applications, above <i>Figure 38: Recommended</i> <i>reset pin protection.</i> Removed typical HSI accuracy curve in <i>Section 10.3.4: Internal clock</i> <i>sources and timing characteristics.</i> Renamed package type 2 into package pitch and added pitch code "C" in <i>Figure 63: STM8S103F2/x3 access line ordering information</i> <i>scheme</i> ⁽¹⁾ and added UFQFPN20 in <i>Section 13.1: STM8S103</i> <i>FASTROM microcontroller option list.</i> Updated the disclaimer.	

Table 59. Document revision history



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