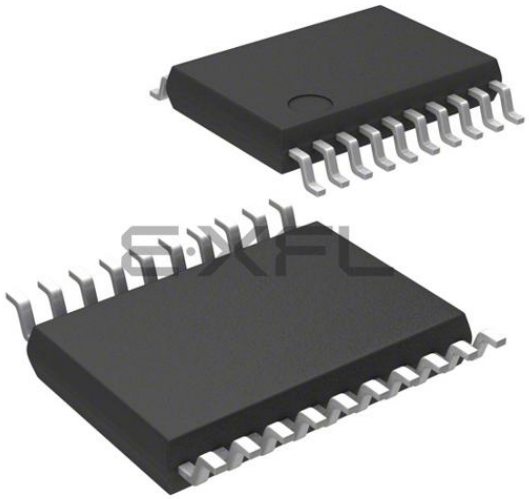

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f3p3tr

2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8S103F2/x3 access line features

Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels,
- 32 interrupt vectors with hardware priority,
- Up to 27 external interrupts on 6 vectors including TLI,
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- 8 Kbyte of Flash program single voltage Flash memory,
- 640 byte true data EEPROM,
- User option byte area.

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

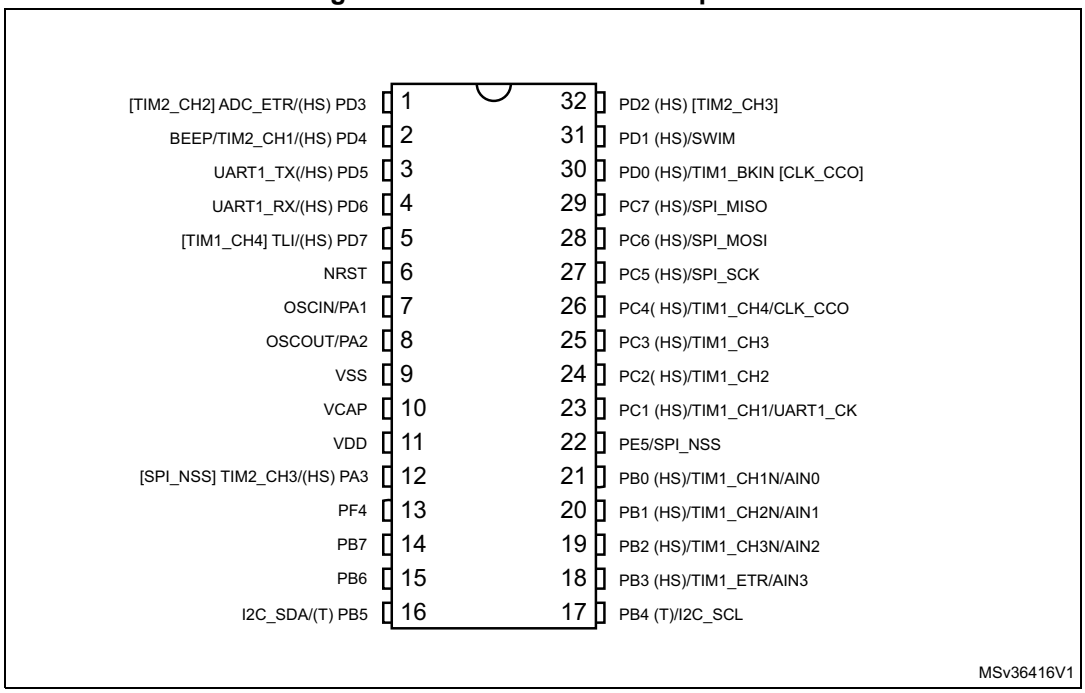
This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2 - 16-bit general purpose timer

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update

Figure 4. STM8S103K3 SDIP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S103K3 pin descriptions

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
6	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
7	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
8	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
9	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
10	5	VCAP	S	-	-	-	-	-	-		1.8 V regulator capacitor		-
11	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
12	7	PA3/ TIM2_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
13	8	PF4	I/O	**X**	X	-	-	O1	X	X	Port F4	-	-
14	9	PB7	I/O	**X**	X	X	-	O1	X	X	Port B7	-	-

Table 5. STM8S103K3 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
15	10	PB6	I/O	**X**	X	X	-	O1	X	X	Port B6	-	-
16	11	PB5/ I2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	-
17	12	PB4/ I2C_SCL	I/O	**X**	-	X	-	O1	T	-	Port B4	I2C clock	-
18	13	PB3/AIN3/ TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	Port B3	Analog input 3/ Timer 1 external trigger	-
19	14	PB2/AIN2/ TIM1_CH3N	I/O	**X**	X	X	HS	O3	X	X	Port B2	Analog input 2/ Timer 1 - inverted channel 3	-
20	15	PB1/AIN1/ TIM1_CH2N	I/O	**X**	X	X	HS	O3	X	X	Port B1	Analog input 1/ Timer 1 - inverted channel 2	-
21	16	PB0/AIN0/ TIM1_CH1N	I/O	**X**	X	X	HS	O3	X	X	Port B0	Analog input 0/ Timer 1 - inverted channel 1	-
22	17	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	Port E5	SPI master/slave select	-
23	18	PC1/ TIM1_CH1/ UART1_CK	I/O	**X**	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 UART1 clock	-
24	19	PC2/ TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	Port C2	Timer 1 - channel 2	-
25	20	PC3/ TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
26	21	PC4/ TIM1_CH4/ CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	-
27	22	PC5/ SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	-
28	23	PC6/ SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-

Table 6. STM8S103F2 and STM8S103F3 pin descriptions (continued)

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/[TIM1_ CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/[T IM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).1

5.3 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

1. Depends on the external circuitry.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

8 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option byte can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option byte can also be modified ‘on the fly’ by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

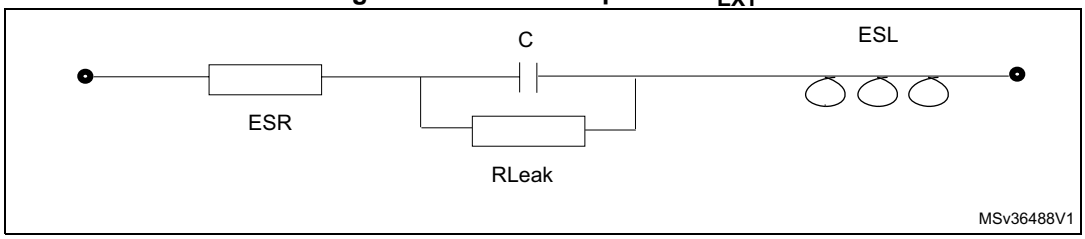
Table 11. Option byte

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC [7:0]								0x00
0x4802		NOPT1	NUBC [7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805h	Misc. option	OPT3	Reserved			HSI TRIM	LSI _ EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI _ EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								0x00
0x480A		NOPT5	NHSECNT [7:0]								0xFF

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 19*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 9: Pin input voltage*.

Total supply current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

Total current consumption in wait mode

Table 23. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 24. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.1	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 25. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	300	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power down mode	LSI RC osc. (128 kHz)	10	20	40	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 26. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	290	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 27. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20	55	

1. Guaranteed by characterization results.

Table 28. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low power mode wakeup times

Table 29. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(2)	0 to 16 MHz			-	See note(3)	µs
$t_{WU(WFI)}$	Wakeup time from run mode(2)	f_{CPU}= f_{MASTER}= 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in operating mode(5)	HSI (after wakeup)	3(6)	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in operating mode(5)	HSI (after wakeup)	48(6)	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in power-down mode(5)	HSI (after wakeup)	50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in operating mode(5)			52	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in power-down mode(5)			54	-	

1. Guaranteed by characterization results.

2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 30. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	400	-	µA
		V_{DD} = 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 31. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	130	
$I_{DD(TIM4)}$	TIM4 supply current(1)	50	
$I_{DD(UART1)}$	UART1 supply current (2)	120	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 35. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

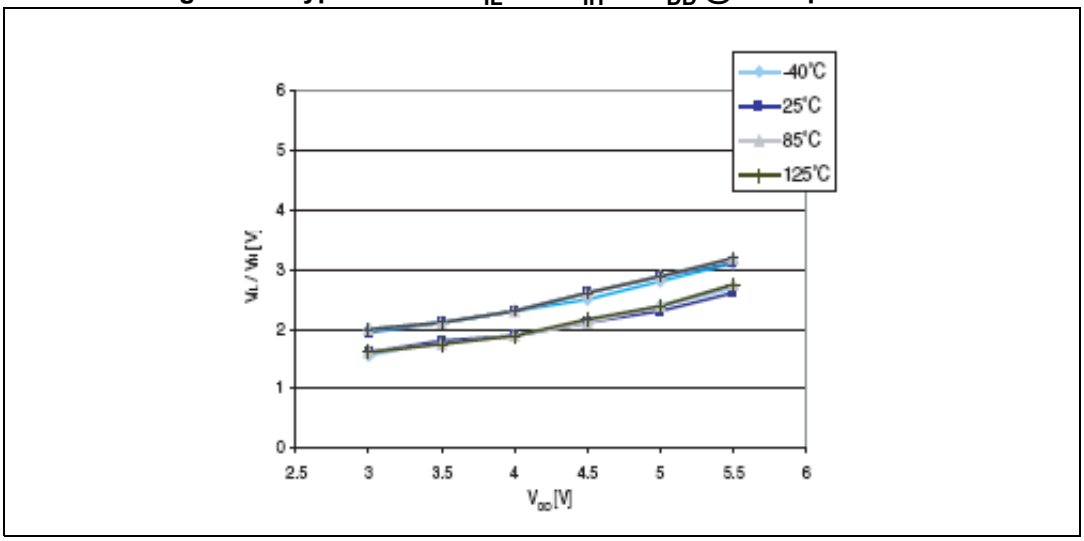


Table 46. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	2.2	4	
		f_{ADC} = 6 MHz	2.4	4.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1.1	2.5	
		f_{ADC} = 4 MHz	1.5	3	
		f_{ADC} = 6 MHz	1.8	3	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.5	3	
		f_{ADC} = 4 MHz	2.1	3	
		f_{ADC} = 6 MHz	2.2	4	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	
		f_{ADC} = 6 MHz	0.8	2	

1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Table 59. Document revision history

Date	Revision	Changes
04-Apr-2012	8	Updated notes related to V_{CAP} in *Table 19: General operating conditions*. Added values of t_R/t_F for 50 pF load capacitance, and updated note in *Table 38: I/O static characteristics*. Updated typical and maximum values of R_{PU} in *Table 38: I/O static characteristics* and *Table 42: NRST pin characteristics*. Changed SCK input to SCK output in *Section 10.3.8: SPI serial peripheral interface* Modified *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* to add package top view.
26-Jun-2012	9	Added *Section 11.4: SDIP32 package information*.
04-Feb-2015	10	Updated *Section 11.5: TSSOP20 package information* and *Section 11.3: UFQFPN20 package information*.
10-Mar-2015	11	Updated: – *Table 34: HSI oscillator characteristics*: corrected HSI oscillator accuracy (factory calibrated) for V_{DD} = 5 V and T_A = 25 °C. – *Table 38: I/O static characteristics*: corrected the max. value for T_R/T_F, Fast I/Os, Load = 50 pF. Added: – *Figure 23: Typical pull-up current vs V_{DD} @ 4 temperatures*, – the rows for T_R/T_F, Fast I/Os, Load = 20 pF in *Table 38: I/O static characteristics*, – *Figure 47: LQFP32 marking example (package top view)*, – *Figure 50: UFQFPN32 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 55: SDIP32 marking example (package top view)*, – *Figure 58: TSSOP20 marking example (package top view)*, – *Figure 60: SO20 marking example (package top view)*.
26-Mar-2015	12	Corrected the values for “b” dimensions in *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.