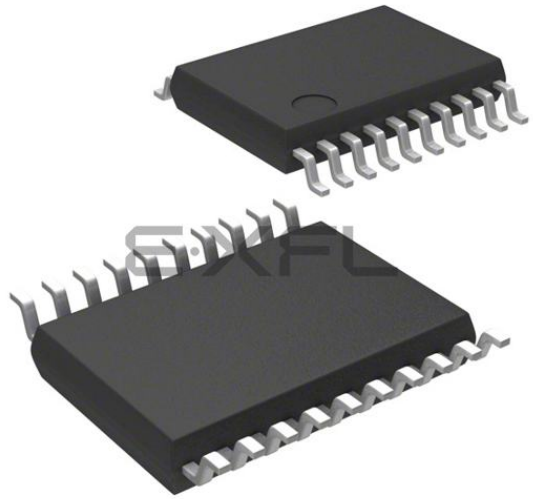

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f3p6

2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8S103F2/x3 access line features

Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels,
- 32 interrupt vectors with hardware priority,
- Up to 27 external interrupts on 6 vectors including TLI,
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- 8 Kbyte of Flash program single voltage Flash memory,
- 640 byte true data EEPROM,
- User option byte area.

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

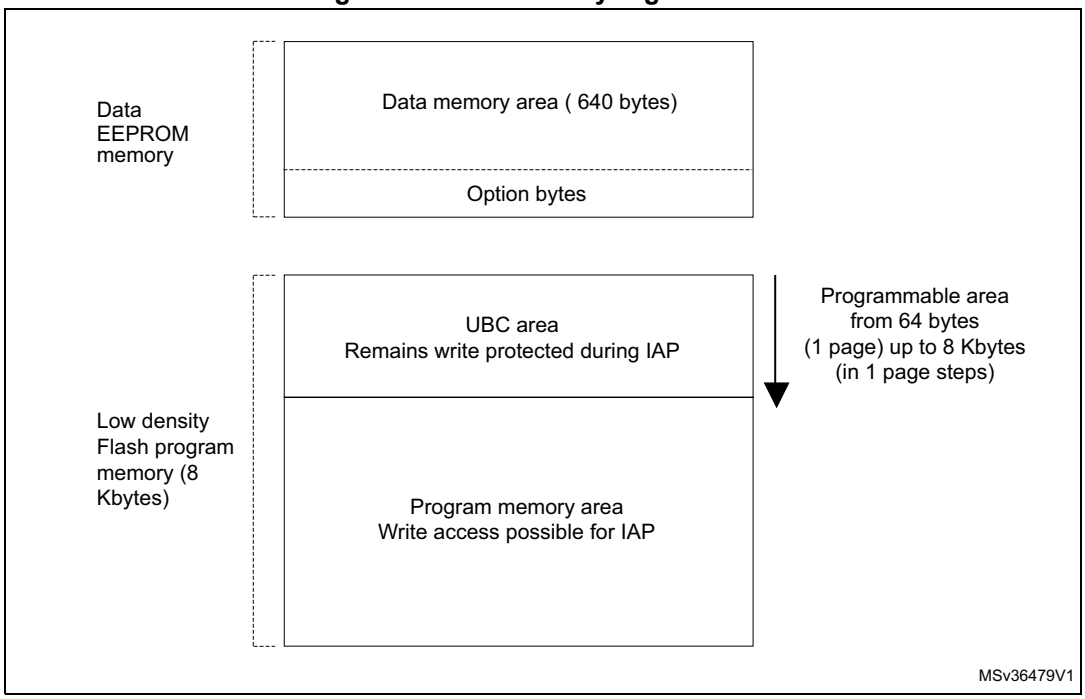
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

5 Pinout and pin description

Table 4. Legend/abbreviations for pin description tables

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold **X** (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Table 6. STM8S103F2 and STM8S103F3 pin descriptions (continued)

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/[TIM1_ CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/[T IM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).1

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	Reserved	-	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM2	TIM2 update/ overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/ compare	-	-	0x00 8040
15	Reserved	-	-	-	0x00 8044
16	Reserved	-	-	-	0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054
20	Reserved	-	-	-	0x00 8058

Table 12. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK:** External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

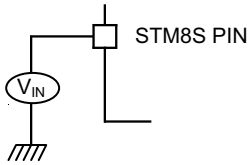
8.1 Alternate function remapping bits

Table 13. STM8S103K3 alternate function remapping bits for 32-pin devices

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 Reserved.
	AFR6 Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.(2) 1: Port D7 alternate function = TIM1_CH4.
	AFR5 Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.(2) 1: Port D0 alternate function = CLK_CCO.
	AFR[4:2] Alternate function remapping options 4:2 Reserved.
	AFR1 Alternate function remapping option 1 0: AFR1 remapping option inactive: Default alternate functions.(2) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3.
	AFR0 Alternate function remapping option 0 Reserved.

1. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.
2. Refer to pinout description.

Figure 9. Pin input voltage



MSv36481V1

10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics* and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and a functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

The device's mission profile (application conditions) is compliant with the JEDEC JESD47 Qualification Standard, the extended mission profiles are available on demand.

Table 16. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 87*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. This pin must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

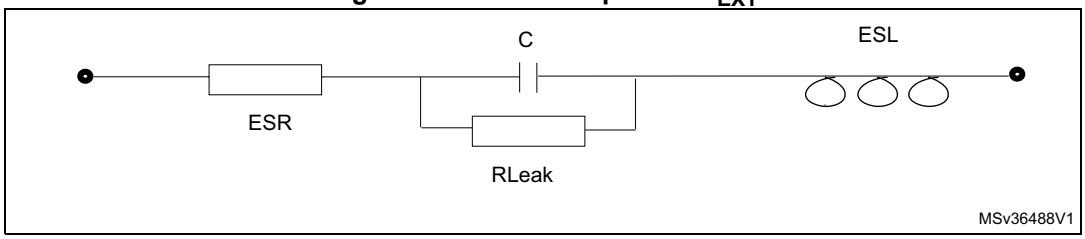
Table 17. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 19*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 9: Pin input voltage*.

Total supply current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

10.3.5 Memory characteristics

RAM and hardware registers

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Section 10.3: Operating conditions* for the value of V_{IT-max}.

Flash program memory/data EEPROM memory

Table 37. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU}≤ 16 MHz	2.95	-	5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte)	-	-	6	6.6	ms
	Fast programming time for 1 block (64 byte)	-	-	3	3.33	
t_{erase}	Erase time for 1 block (64 byte)	-	-	3	3.33	
N_{RW}	Erase/write cycles (program memory)(2)	T_A = +85 °C	100k	-	-	cycle
	Erase/write cycles (data memory)(2)	T_A = +125 °C	300k	1M	-	
t_{RET}	Data retention (program and data memory) after 10k erase/write cycles at T_A= +55 °C	T_{RET} = 55 °C	20	-	-	year
	Data retention (data memory) after 300k erase/write cycles at T_A= +125°C	T_{RET} = 85 °C	1	-	-	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 byte)	-	-	2	-	mA

1. Guaranteed by characterization results.
2. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 35. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

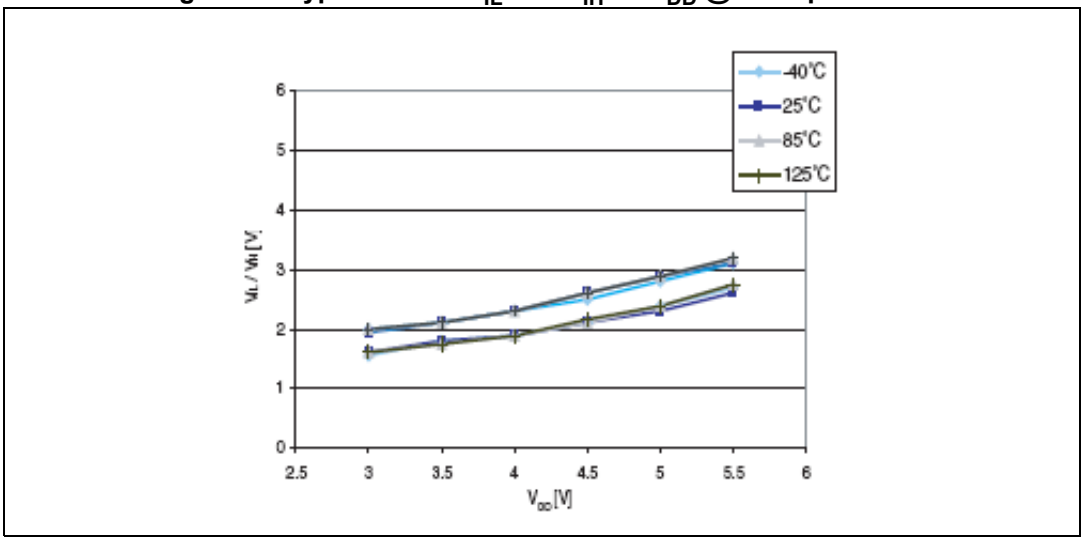
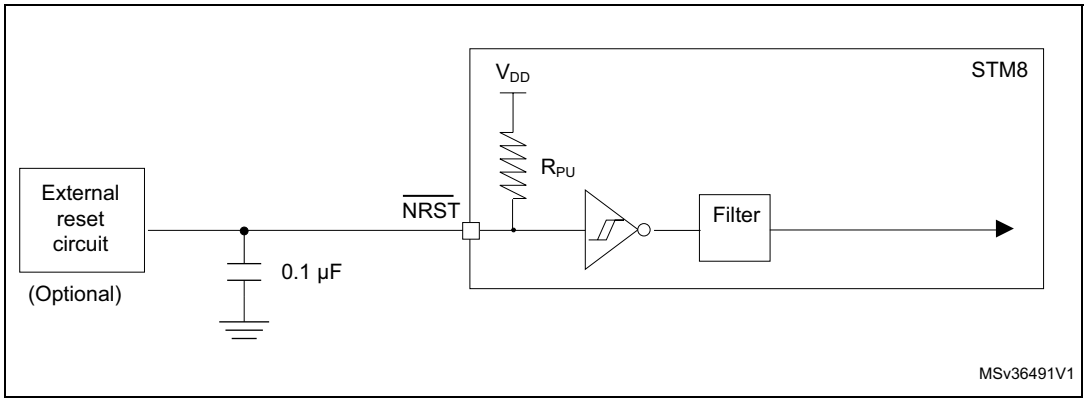


Figure 38. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI characteristics

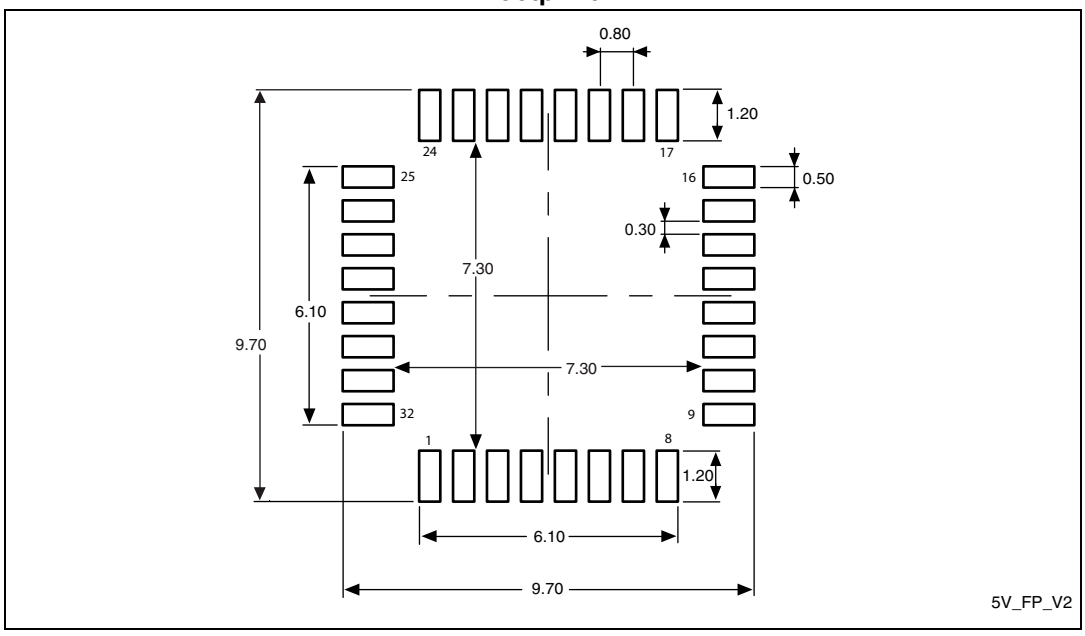
Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	7	

Table 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.5 TSSOP20 package information

Figure 56. TSSOP20 package outline

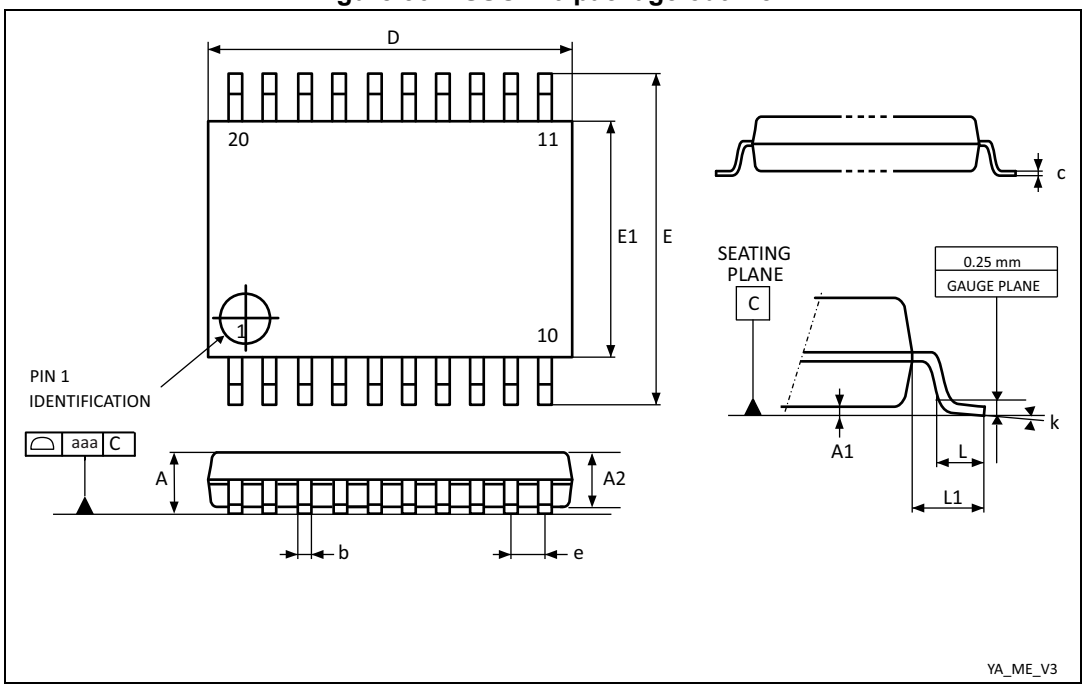


Table 56. TSSOP20 package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

11.6 SO20 package information

Figure 59. SO20 package outline

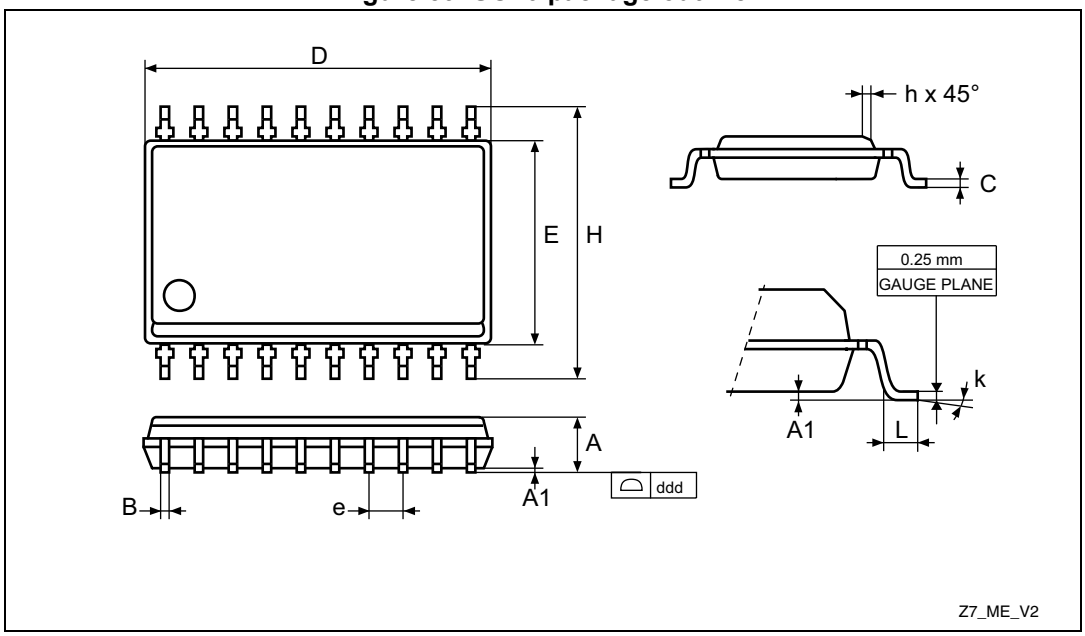


Table 57. SO20 mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	2.350	-	2.650	0.0925	-	0.1043
A1	0.100	-	0.300	0.0039	-	0.0118
B	0.330	-	0.510	0.013	-	0.0201
C	0.230	-	0.320	0.0091	-	0.0126
D	12.600	-	13.000	0.4961	-	0.5118
E	7.400	-	7.600	0.2913	-	0.2992
e	-	1.270	-	-	0.0500	-
H	10.000	-	10.650	0.3937	-	0.4193
h	0.250	-	0.750	0.0098	-	0.0295
L	0.400	-	1.270	0.0157	-	0.0500
k	0.0°	-	8.0°	0.0°	-	8.0°
ddd	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

AFR0	Reserved
AFR1 (check only one option)	[ ] 1: Port A3 alternate function = SPI_NSS and port D2 alternate function = TIM2_CH3 [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description
AFR2	Reserved
AFR3	Reserved
AFR4	Reserved
AFR5 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = CLK_CCO
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D7 alternate function = TIM1_CH4
AFR7	Reserved

OPT3 watchdog

WWDG_HALT (check only one option)	[ ] 0: No reset generated on halt if WWDG active[[ ] 1: Reset generated on halt if WWDG active
WWDG_HW (check only one option)	[ ] 0: WWDG activated by software [ ] 1: WWDG activated by hardware
IWDG_HW (check only one option)	[ ] 0: IWDG activated by software [ ] 1: IWDG activated by hardware
LSI_EN (check only one option)	[ ] 0: LSI clock is not available as CPU clock source [ ] 1: LSI clock is available as CPU clock source
HSITRIM (check only one option)	[ ] 0: 3-bit trimming supported in CLK_HSITRIMR register [ ] 1: 4-bit trimming supported in CLK_HSITRIMR register

OPT4 watchdog

PRSC (check only one option)	[ ] for 16 MHz to 128 kHz prescaler [ ] for 8 MHz to 128 kHz prescaler [ ] for 4 MHz to 128 kHz prescaler
CKAWUSEL (check only one option)	[ ] LSI clock source selected for AWU [ ] HSE clock with prescaler selected as clock source for AWU
EXTCLK (check only one option)	[ ] External crystal connected to OSCIN/OSCOUT [ ] External signal on OSCIN

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....
Date:	.....
Signature:	.....

15 Revision history

Table 59. Document revision history

Date	Revision	Changes
02-Mar-2009	1	Initial release.
10-Apr-2009	2	Added *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers*. Updated *Section 4.8: Auto wakeup counter*. Modified the description of PB4 and PB5 (removed X in PP column) and added footnote concerning HS I/Os in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed TIM3 and UART from *Table 10: Interrupt mapping*. Updated VCAP specifications in *Section 10.3.1: VCAP external capacitor* Corrected the block size in *Table 37: Flash program memory/data EEPROM memory*t Updated *Section 10: Electrical characteristics*. Updated *Section 12: Thermal characteristics*.
10-Jun-1999	3	Document status changed from “preliminary data” to “datasheet”. Replaced WFQFPN20 package with UFQFPN package. Replaced ‘VFQFN’ with ‘VFQFPN’. Added bullet point on the unique identifier to *Features*. Updated *Section 4.8: Auto wakeup counter*. Updated wpu and PP status of PB5/12C_SDA and PB4/12C_SCL pins in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. Updated *Section 6.1: Memory map*. Updated reset status of port D CR1 register in *Table 7: I/O port hardware register map*. Updated alternate function remapping descriptions in *Table 13: STM8S103K3 alternate function remapping bits for 32-pin devices* and *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*. Added *Section 9: Unique ID*. Updated *Section 10.3: Operating conditions*. Updated the caption of *Figure 20: Typical HSI frequency variation vs V_{DD} @ 4 temperatures*. Updated *Table 43: SPI characteristics* and added TBD occurrences. Added max values to *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated *Section 10.3.11: EMC characteristics*.

Table 59. Document revision history

Date	Revision	Changes
04-Apr-2012	8	Updated notes related to V_{CAP} in *Table 19: General operating conditions*. Added values of t_R/t_F for 50 pF load capacitance, and updated note in *Table 38: I/O static characteristics*. Updated typical and maximum values of R_{PU} in *Table 38: I/O static characteristics* and *Table 42: NRST pin characteristics*. Changed SCK input to SCK output in *Section 10.3.8: SPI serial peripheral interface* Modified *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* to add package top view.
26-Jun-2012	9	Added *Section 11.4: SDIP32 package information*.
04-Feb-2015	10	Updated *Section 11.5: TSSOP20 package information* and *Section 11.3: UFQFPN20 package information*.
10-Mar-2015	11	Updated: – *Table 34: HSI oscillator characteristics*: corrected HSI oscillator accuracy (factory calibrated) for V_{DD} = 5 V and T_A = 25 °C. – *Table 38: I/O static characteristics*: corrected the max. value for T_R/T_F, Fast I/Os, Load = 50 pF. Added: – *Figure 23: Typical pull-up current vs V_{DD} @ 4 temperatures*, – the rows for T_R/T_F, Fast I/Os, Load = 20 pF in *Table 38: I/O static characteristics*, – *Figure 47: LQFP32 marking example (package top view)*, – *Figure 50: UFQFPN32 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 55: SDIP32 marking example (package top view)*, – *Figure 58: TSSOP20 marking example (package top view)*, – *Figure 60: SO20 marking example (package top view)*.
26-Mar-2015	12	Corrected the values for “b” dimensions in *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.