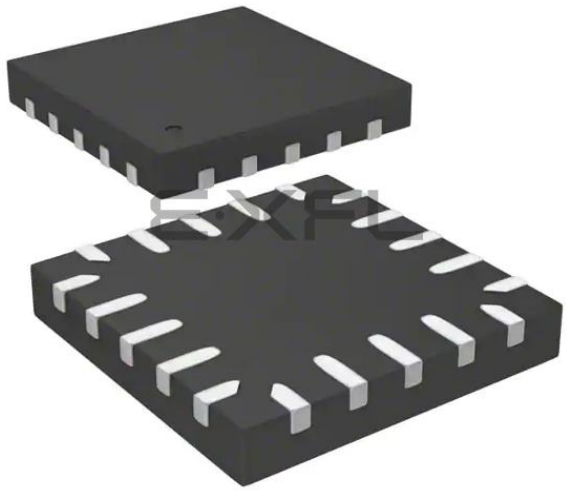

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103f3u6atr

List of figures

4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

Instruction set

- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

Table 5. STM8S103K3 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
15	10	PB6	I/O	**X**	X	X	-	O1	X	X	Port B6	-	-
16	11	PB5/ I2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	-
17	12	PB4/ I2C_SCL	I/O	**X**	-	X	-	O1	T	-	Port B4	I2C clock	-
18	13	PB3/AIN3/ TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	Port B3	Analog input 3/ Timer 1 external trigger	-
19	14	PB2/AIN2/ TIM1_CH3N	I/O	**X**	X	X	HS	O3	X	X	Port B2	Analog input 2/ Timer 1 - inverted channel 3	-
20	15	PB1/AIN1/ TIM1_CH2N	I/O	**X**	X	X	HS	O3	X	X	Port B1	Analog input 1/ Timer 1 - inverted channel 2	-
21	16	PB0/AIN0/ TIM1_CH1N	I/O	**X**	X	X	HS	O3	X	X	Port B0	Analog input 0/ Timer 1 - inverted channel 1	-
22	17	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	Port E5	SPI master/slave select	-
23	18	PC1/ TIM1_CH1/ UART1_CK	I/O	**X**	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 UART1 clock	-
24	19	PC2/ TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	Port C2	Timer 1 - channel 2	-
25	20	PC3/ TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
26	21	PC4/ TIM1_CH4/ CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	-
27	22	PC5/ SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	-
28	23	PC6/ SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-

Table 6. STM8S103F2 and STM8S103F3 pin descriptions

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	18	PD4/ BEEP/ TIM2_ CH1/ UART1 _CK	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output/ UART1 clock	-
2	19	PD5/ AIN5/ UART1 _TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ UART1 data transmit	-
3	20	PD6/ AIN6/ UART1 _RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
4	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM2_ CH3 [SPI_ NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
11	8	PB5/ I2C_ SDA [TIM1_ BKIN]	I/O	**X**	-	-	X	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_ SCL	I/O	**X**	-	-	X	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3 [TLI] [TIM1_ CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 - inverted channel 1 [AFR7]

6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 12. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK:** External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

8.1 Alternate function remapping bits

Table 13. STM8S103K3 alternate function remapping bits for 32-pin devices

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 Reserved.
	AFR6 Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.(2) 1: Port D7 alternate function = TIM1_CH4.
	AFR5 Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.(2) 1: Port D0 alternate function = CLK_CCO.
	AFR[4:2] Alternate function remapping options 4:2 Reserved.
	AFR1 Alternate function remapping option 1 0: AFR1 remapping option inactive: Default alternate functions.(2) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3.
	AFR0 Alternate function remapping option 0 Reserved.

1. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.
2. Refer to pinout description.

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

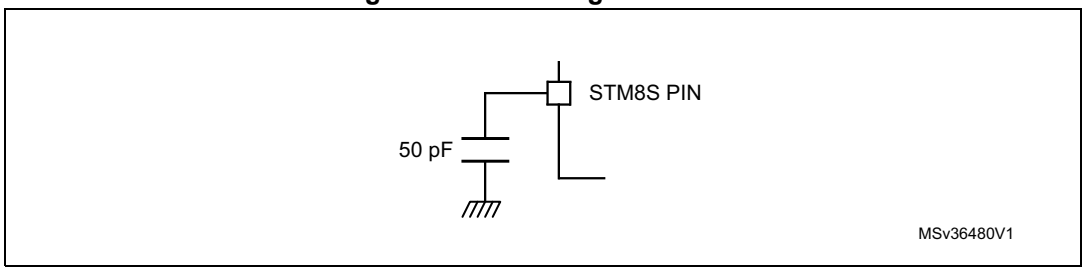
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

Figure 8. Pin loading conditions



10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 20. Operating conditions at power-up/power-down (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold	-	2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

Total current consumption in active halt mode

Table 25. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	300	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power down mode	LSI RC osc. (128 kHz)	10	20	40	

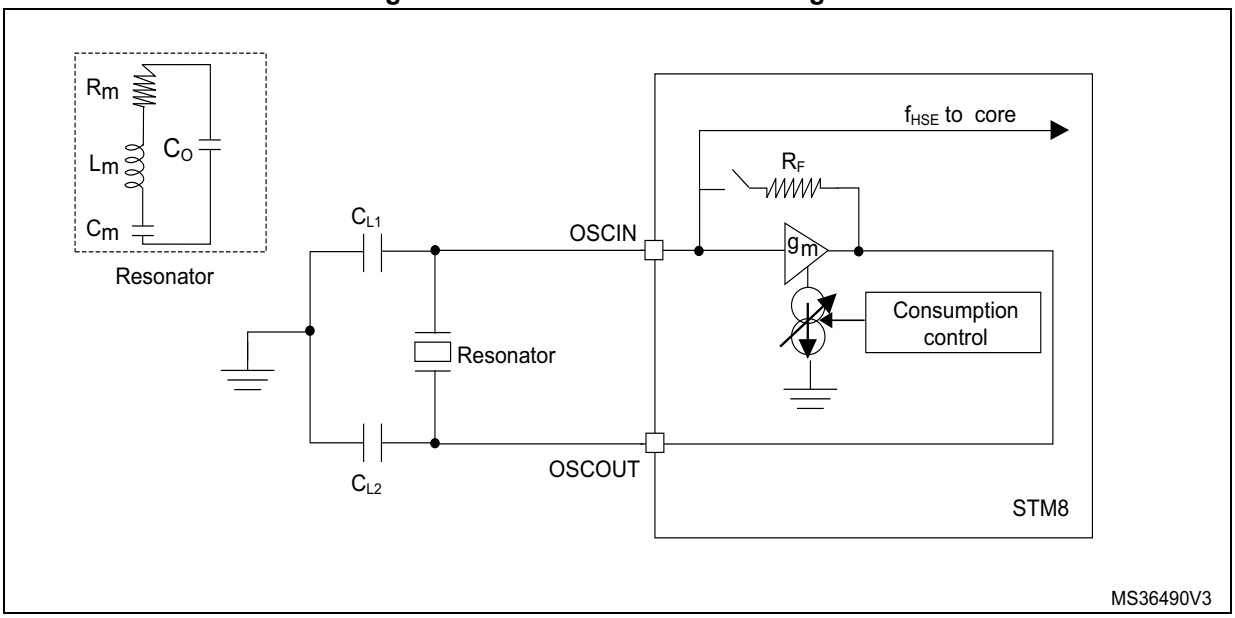
1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 26. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	290	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Figure 19. HSE oscillator circuit diagram



HSE oscillator critical g_m equation

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m \gg g_{mcrit}$

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3 V	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 20 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 20 pF	-	-	50(2)	
I_{lkg}	Digital input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1(3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250(3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design.
3. Guaranteed by characterization results

10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 35. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

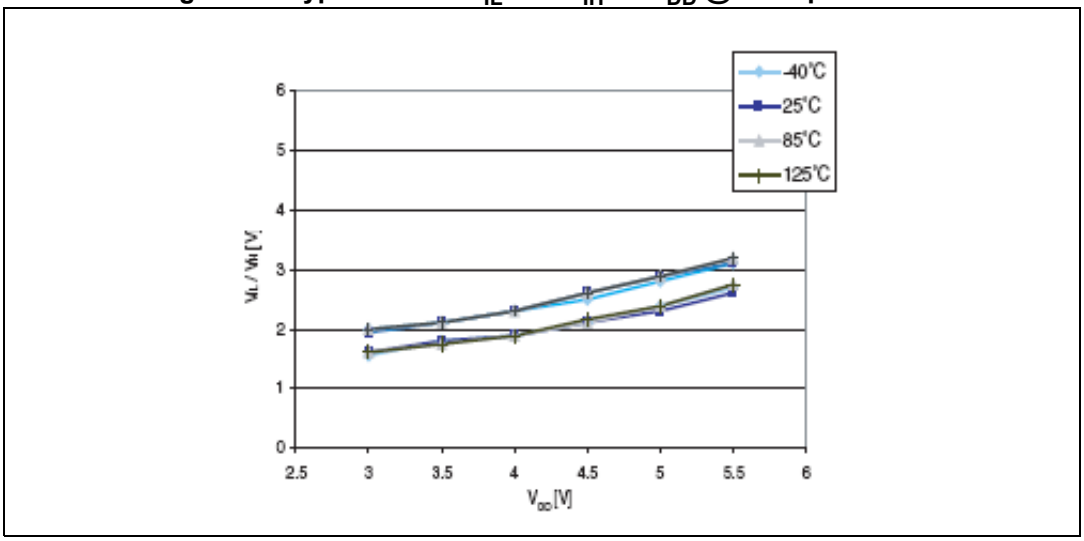
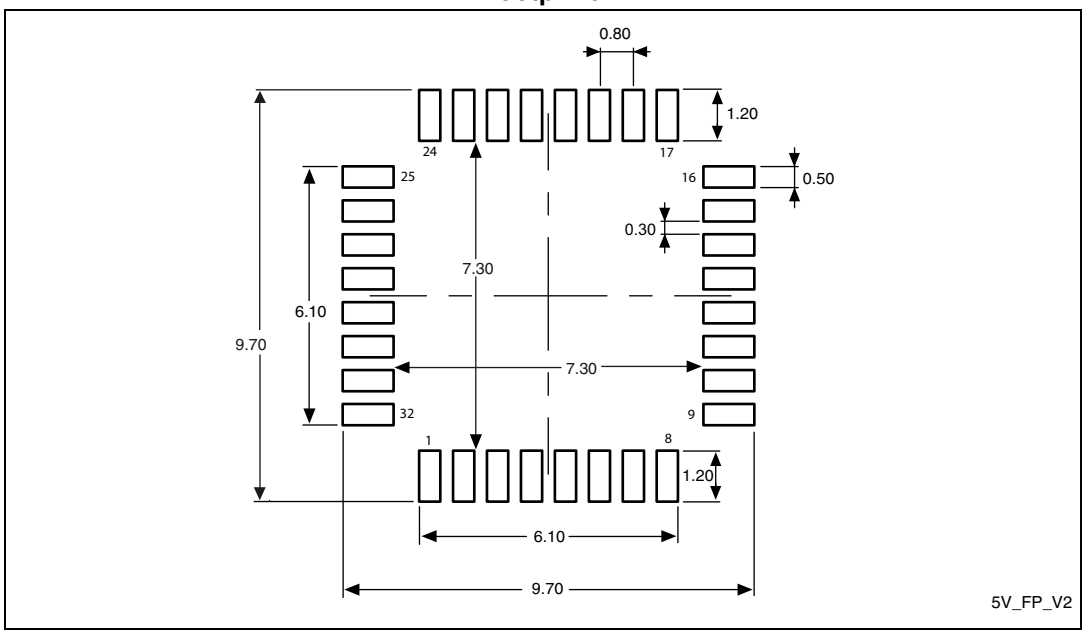


Table 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



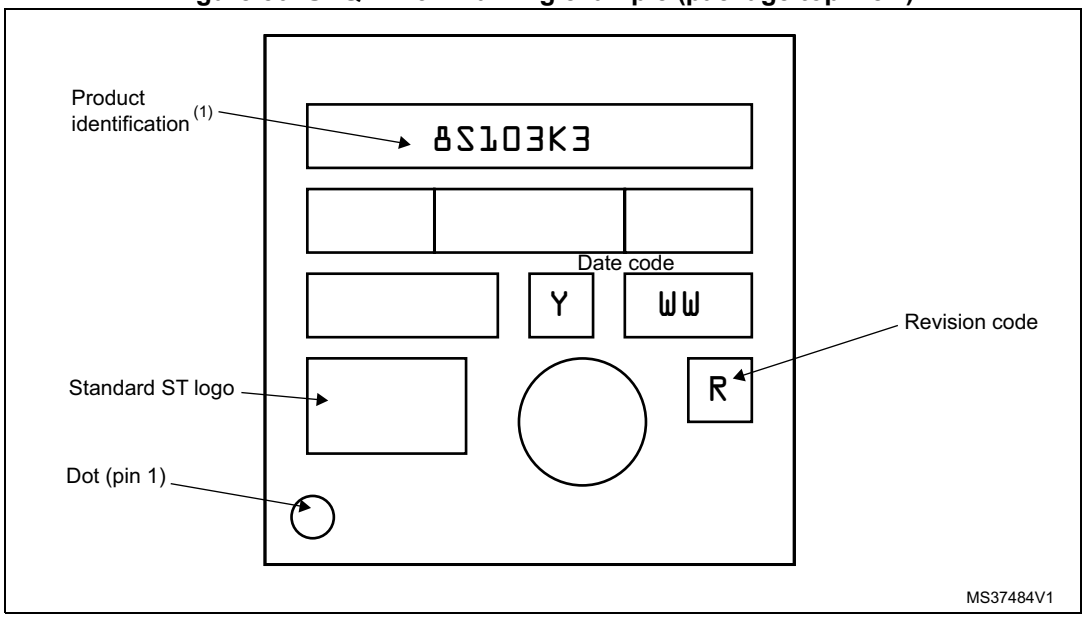
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

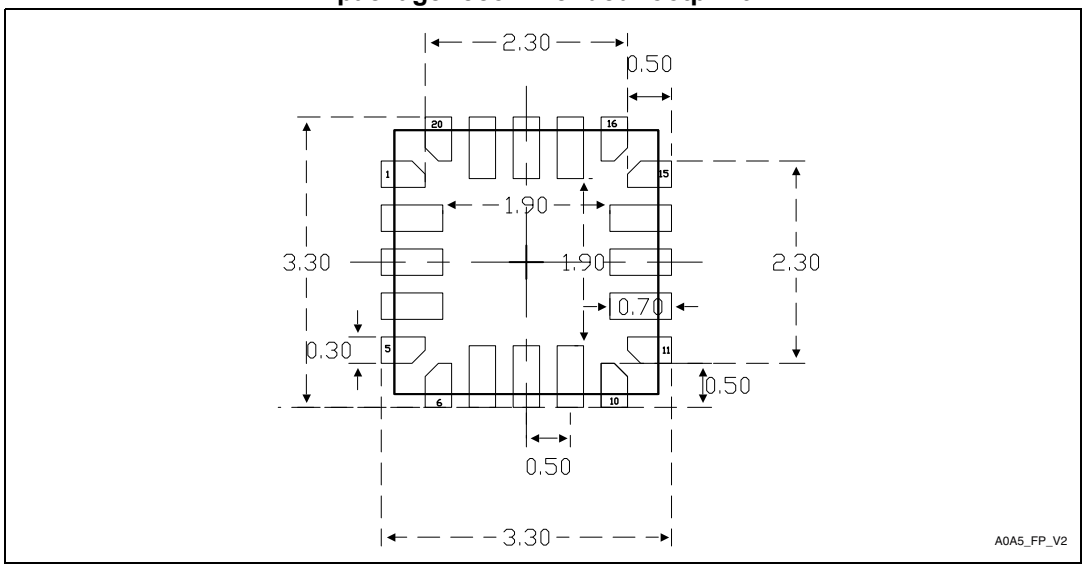
Table 54. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits

Section 11.7: UFQFPN recommended footprint shows the recommended footprints for UFQFPN with and without on-board emulation.

Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

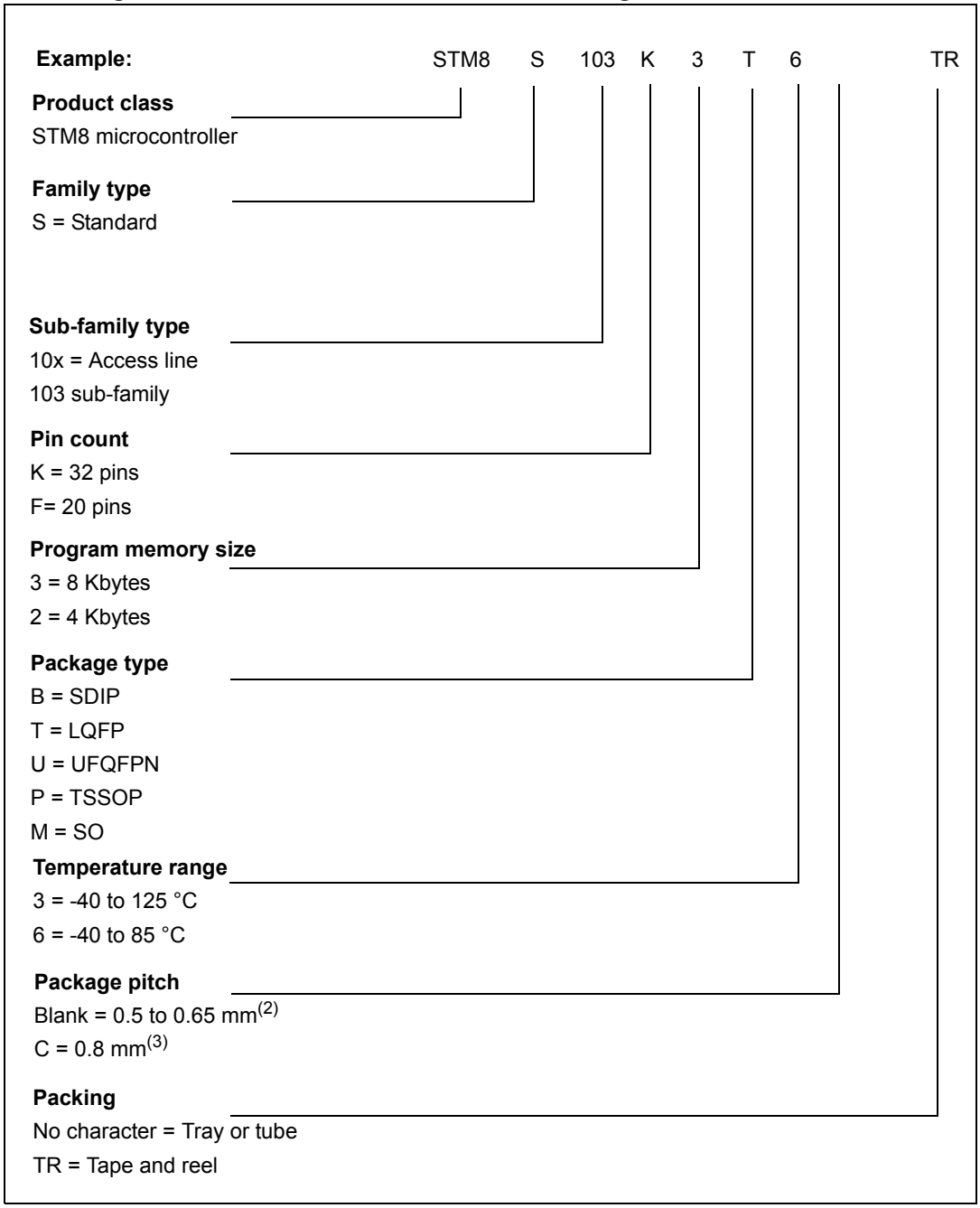
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

13 Ordering information

Figure 63. STM8S103F2/x3 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....
Date:	.....
Signature:	.....

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

15 Revision history

Table 59. Document revision history

Date	Revision	Changes
02-Mar-2009	1	Initial release.
10-Apr-2009	2	Added *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers*. Updated *Section 4.8: Auto wakeup counter*. Modified the description of PB4 and PB5 (removed X in PP column) and added footnote concerning HS I/Os in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed TIM3 and UART from *Table 10: Interrupt mapping*. Updated VCAP specifications in *Section 10.3.1: VCAP external capacitor* Corrected the block size in *Table 37: Flash program memory/data EEPROM memory*t Updated *Section 10: Electrical characteristics*. Updated *Section 12: Thermal characteristics*.
10-Jun-1999	3	Document status changed from “preliminary data” to “datasheet”. Replaced WFQFPN20 package with UFQFPN package. Replaced ‘VFQFN’ with ‘VFQFPN’. Added bullet point on the unique identifier to *Features*. Updated *Section 4.8: Auto wakeup counter*. Updated wpu and PP status of PB5/12C_SDA and PB4/12C_SCL pins in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. Updated *Section 6.1: Memory map*. Updated reset status of port D CR1 register in *Table 7: I/O port hardware register map*. Updated alternate function remapping descriptions in *Table 13: STM8S103K3 alternate function remapping bits for 32-pin devices* and *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*. Added *Section 9: Unique ID*. Updated *Section 10.3: Operating conditions*. Updated the caption of *Figure 20: Typical HSI frequency variation vs V_{DD} @ 4 temperatures*. Updated *Table 43: SPI characteristics* and added TBD occurrences. Added max values to *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated *Section 10.3.11: EMC characteristics*.