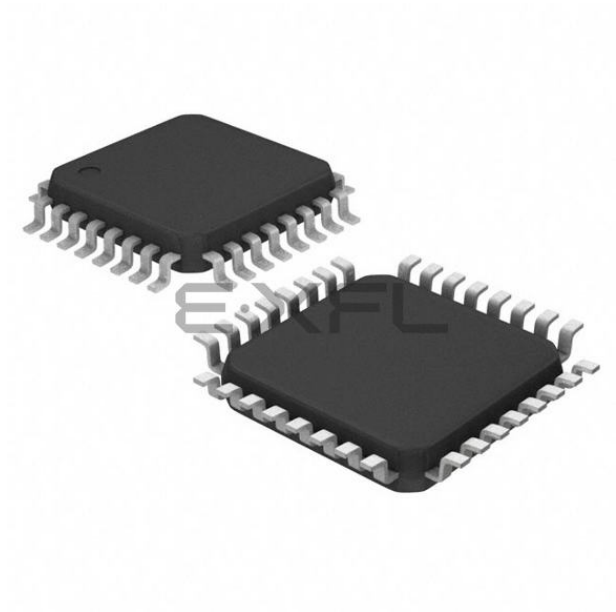

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103k3b6

List of figures

1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

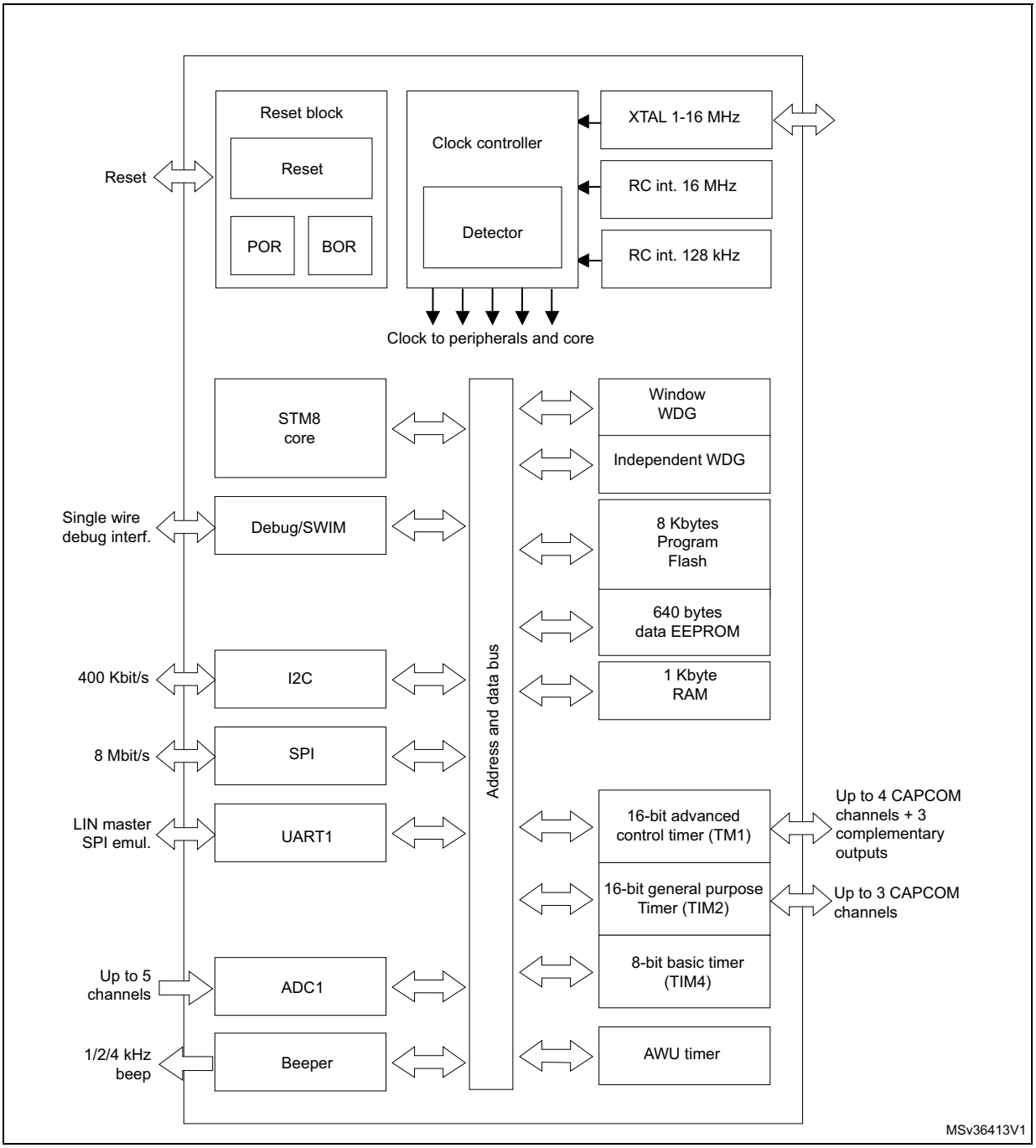
Table 1. STM8S103F2/x3 access line features

Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

3 Block diagram

Figure 1. STM8S103F2/x3 block diagram



4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

Instruction set

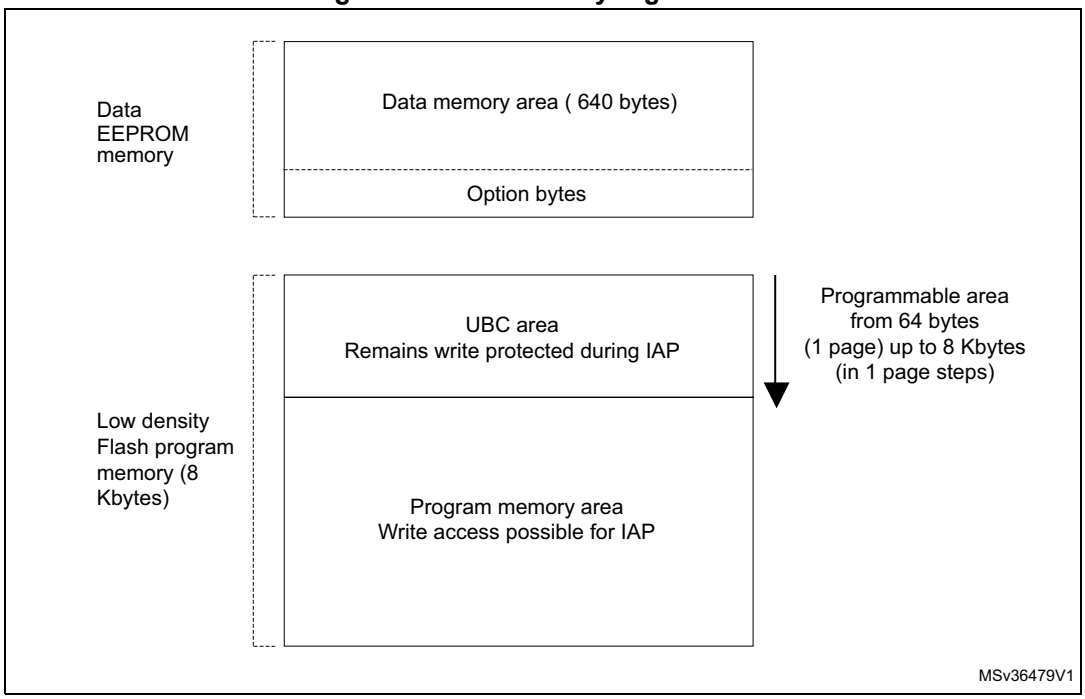
- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected Page 0 and 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory write-protected *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM:** High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 30. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	400	-	µA
		V_{DD} = 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 31. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	130	
$I_{DD(TIM4)}$	TIM4 supply current(1)	50	
$I_{DD(UART1)}$	UART1 supply current (2)	120	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 12. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

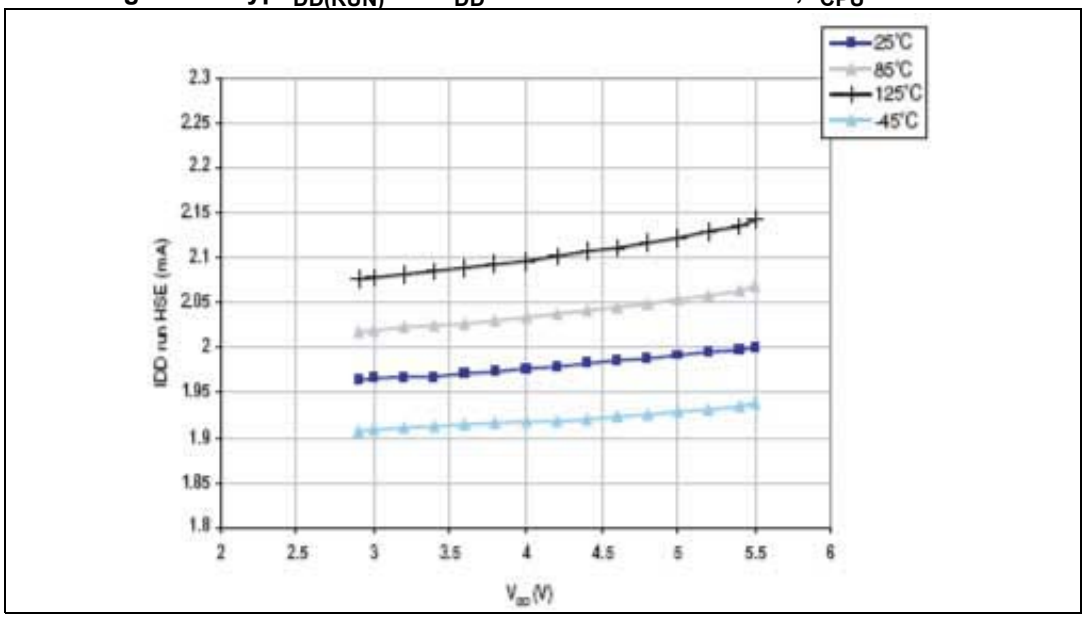
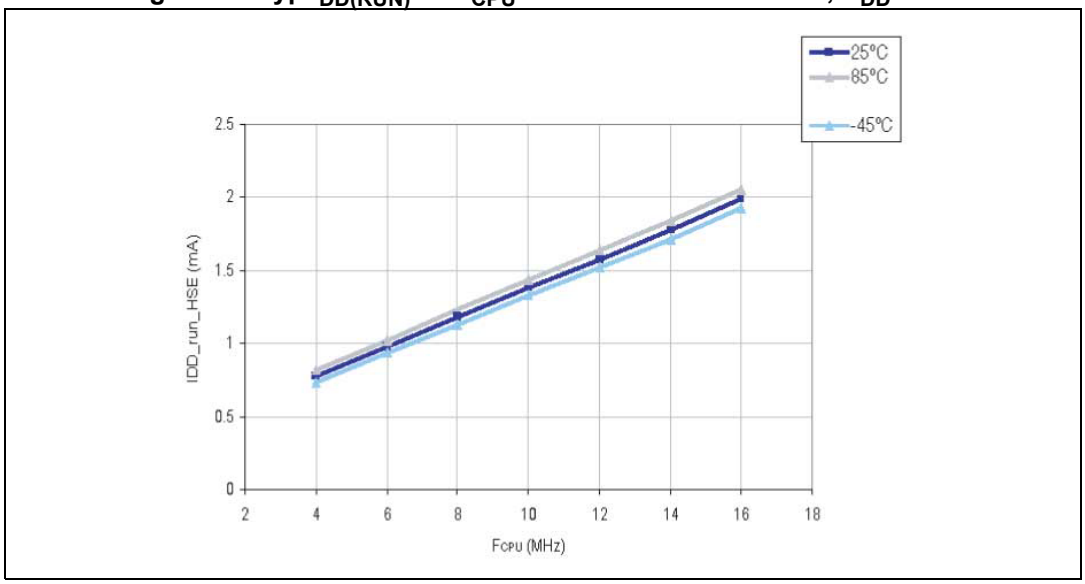


Figure 13. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V



10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 32. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source

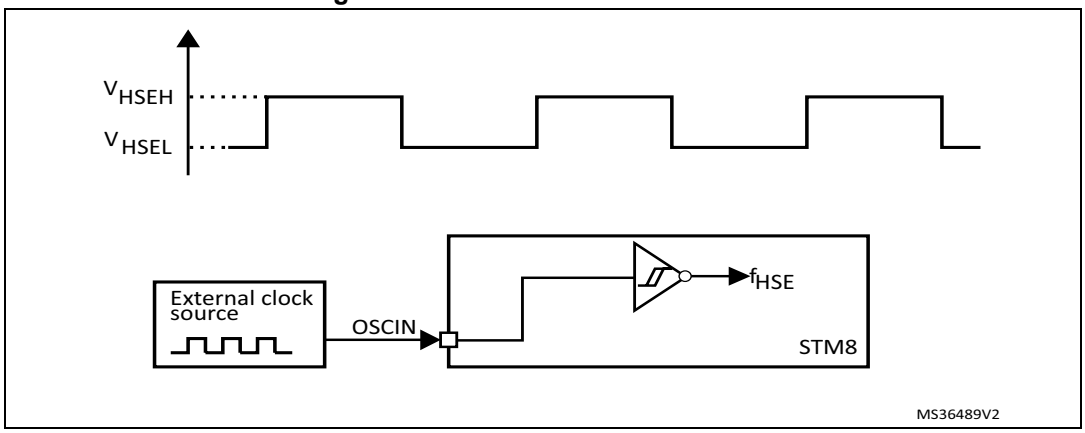


Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

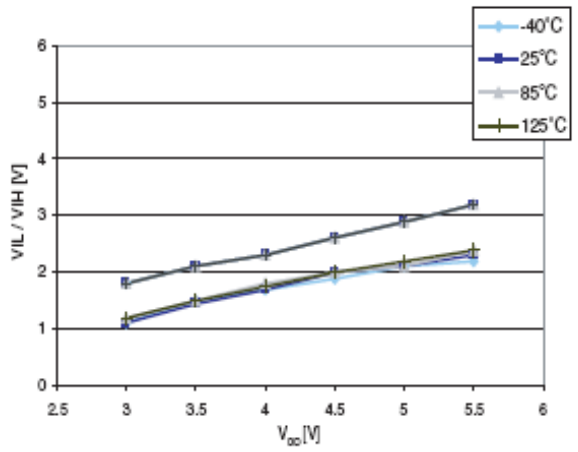


Figure 23. Typical pull-up current vs V_{DD} @ 4 temperatures

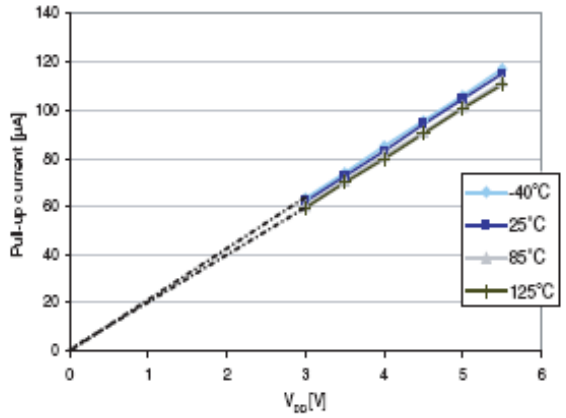


Figure 24. Typical pull-up resistance vs VDD @ 4 temperatures

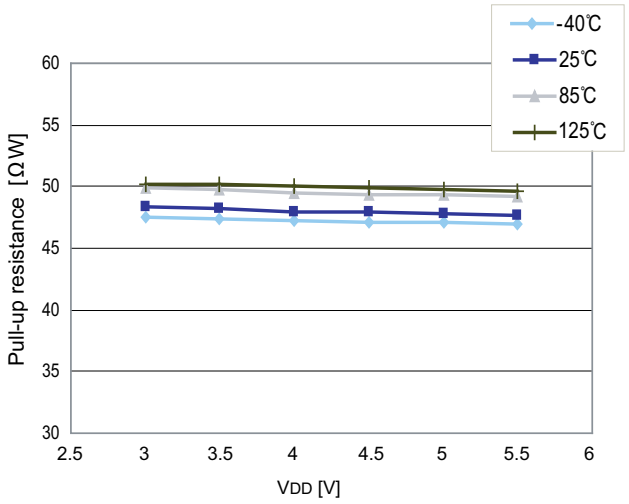
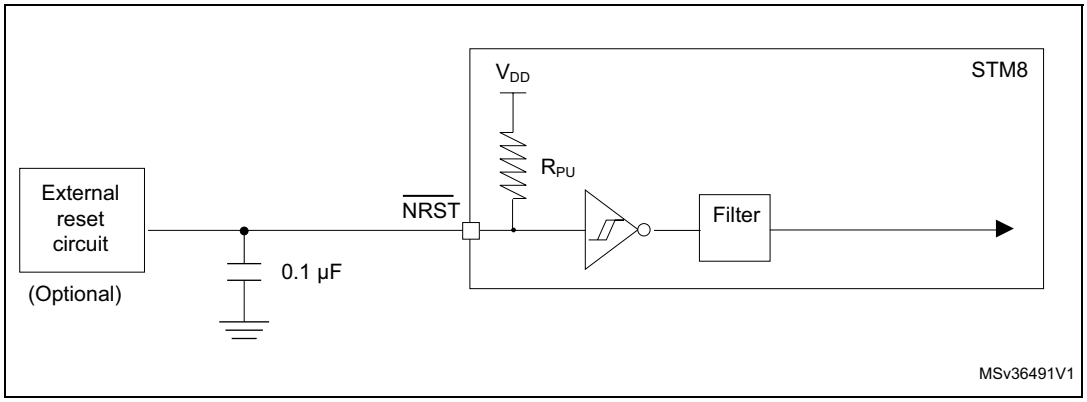


Table 39. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO}= 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO}= 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Guaranteed by characterization results

Figure 38. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	7	

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 49. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		EMI level	2.5	2.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to SD22-C101 LQFP32 package	IV	1000	

1. Guaranteed by characterization results

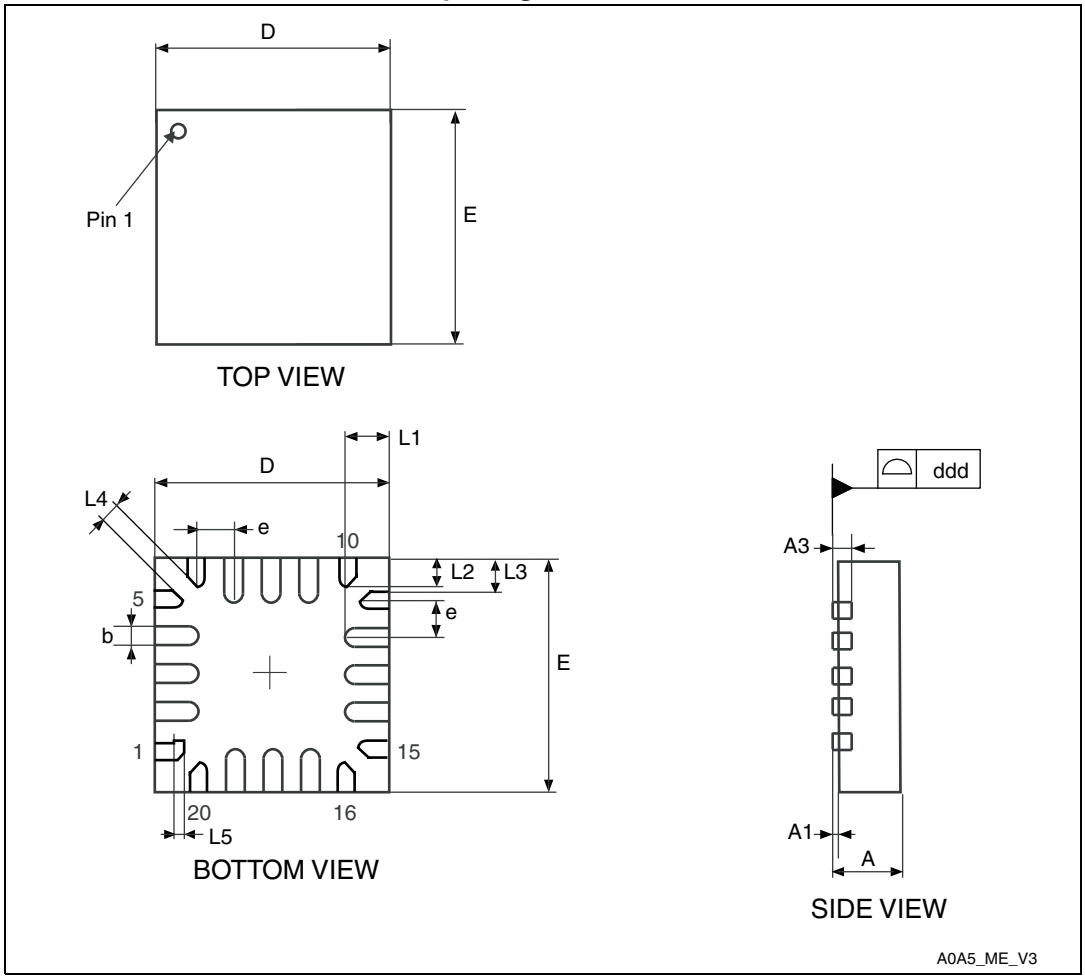
Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

11.3 UFQFPN20 package information

Figure 51. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Table 54. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157

15 Revision history

Table 59. Document revision history

Date	Revision	Changes
02-Mar-2009	1	Initial release.
10-Apr-2009	2	Added *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers*. Updated *Section 4.8: Auto wakeup counter*. Modified the description of PB4 and PB5 (removed X in PP column) and added footnote concerning HS I/Os in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed TIM3 and UART from *Table 10: Interrupt mapping*. Updated VCAP specifications in *Section 10.3.1: VCAP external capacitor* Corrected the block size in *Table 37: Flash program memory/data EEPROM memory*t Updated *Section 10: Electrical characteristics*. Updated *Section 12: Thermal characteristics*.
10-Jun-1999	3	Document status changed from “preliminary data” to “datasheet”. Replaced WFQFPN20 package with UFQFPN package. Replaced ‘VFQFN’ with ‘VFQFPN’. Added bullet point on the unique identifier to *Features*. Updated *Section 4.8: Auto wakeup counter*. Updated wpu and PP status of PB5/12C_SDA and PB4/12C_SCL pins in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. Updated *Section 6.1: Memory map*. Updated reset status of port D CR1 register in *Table 7: I/O port hardware register map*. Updated alternate function remapping descriptions in *Table 13: STM8S103K3 alternate function remapping bits for 32-pin devices* and *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*. Added *Section 9: Unique ID*. Updated *Section 10.3: Operating conditions*. Updated the caption of *Figure 20: Typical HSI frequency variation vs V_{DD} @ 4 temperatures*. Updated *Table 43: SPI characteristics* and added TBD occurrences. Added max values to *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated *Section 10.3.11: EMC characteristics*.

Table 59. Document revision history

Date	Revision	Changes
16-Oct-1999	4	Replaced VFQFPN32 package by UFQFPN32 package. – *Section 4.5: Clock controller*: replaced TIM2 and TIM3 with reserved and TIM2 respectively in *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers* – *Total current consumption in halt mode*: changed the maximum current consumption limit at 125 °C (and VDD= 5 V) from 35 µA to 55 µA. – *Functional EMS (electromagnetic susceptibility)*: renamed ESD as FESD (functional); added name of AN1709; replaced EC 1000 with IEC 61000. – *Designing hardened software to avoid noise problems*: replaced IEC 1000 with IEC 61000, added title of AN1015, and added footnote to EMS data table. – *Electromagnetic interference (EMI)*: replaced J 1752/3 with IEC 61967-2 and updated data of the EMI data table. – *Section 12.2: Selecting the product temperature range*: changed the value of LQFP32 7x7 mm thermal resistance from 59 °C/W to 60 °C/W. Added *Section 13.1: STM8S103 FASTROM microcontroller option list*.
22-Apr-2010	5	Added VFQFPN32 and SO20 packages. Updated Px_IDR reset value in *Table 7: I/O port hardware register map*. – *Section 10.3: Operating conditions*: updated VCAP and ESR low limit, added ESL parameter, and Note 1 below *Table 19: General operating conditions* Updated ACCHSI in *Table 34: HSI oscillator characteristics*. Modified IDD(H)inand. Removed note 3 related to Accuracy of HSI oscillator. Updated maximum power dissipation in *Table 19: General operating conditions*. Updated *Section 12: Thermal characteristics* Replaced package pitch digit by VFQFPN/UFQFPN package digit in *Figure 63: STM8S103F2/x3 access line ordering information scheme*[(1)], and removed note 1.

Table 59. Document revision history

Date	Revision	Changes
09-Sep-2010	6	Removed VFQFPN32 package. Removed internal reference voltage from *Section 4.13: Analog-to-digital converter (ADC1)*. Updated the reset state information in *Table 4: Legend/abbreviations for pin description tables* in *Section 5: Pinout and pin description*. Added footnote to PD1/SWIM pin in *Table 5: STM8S103K3 pin descriptions*. Updated pins 14 and 19 (TSSOP20/SO20) / pins 11 and 16 (UFQFPN20) in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions*. Standardized all reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*. Updated AFR2 description of OPT 2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*s. Replaced 0.01 µF with 0.1 µf in *Figure 38: Recommended reset pin protection*. Added *Figure 42: Typical application with I^2C bus and timing diagram* and *Table 44: I^2C characteristics*. Updated footnote 1 in *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated the Special marking section in *Section 13.1: STM8S103 FASTROM microcontroller option list*: Updated AFR2 description of OTP2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices* Updated existing footnote and added three additional footnotes to *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*
12-Jul-2011	7	Updated the note related to true open-drain outputs in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* Removed CLK_CANCCR register from *Table 8: General hardware register map*. Added note for Px_IDR registers in *Table 7: I/O port hardware register map*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 38: Recommended reset pin protection*. Removed typical HSI accuracy curve in *Section 10.3.4: Internal clock sources and timing characteristics*. Renamed package type 2 into package pitch and added pitch code “C” in *Figure 63: STM8S103F2/x3 access line ordering information scheme(1)* and added UFQFPN20 in *Section 13.1: STM8S103 FASTROM microcontroller option list*. Updated the disclaimer.

Table 59. Document revision history

Date	Revision	Changes
04-Apr-2012	8	Updated notes related to V_{CAP} in *Table 19: General operating conditions*. Added values of t_R/t_F for 50 pF load capacitance, and updated note in *Table 38: I/O static characteristics*. Updated typical and maximum values of R_{PU} in *Table 38: I/O static characteristics* and *Table 42: NRST pin characteristics*. Changed SCK input to SCK output in *Section 10.3.8: SPI serial peripheral interface* Modified *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* to add package top view.
26-Jun-2012	9	Added *Section 11.4: SDIP32 package information*.
04-Feb-2015	10	Updated *Section 11.5: TSSOP20 package information* and *Section 11.3: UFQFPN20 package information*.
10-Mar-2015	11	Updated: – *Table 34: HSI oscillator characteristics*: corrected HSI oscillator accuracy (factory calibrated) for V_{DD} = 5 V and T_A = 25 °C. – *Table 38: I/O static characteristics*: corrected the max. value for T_R/T_F, Fast I/Os, Load = 50 pF. Added: – *Figure 23: Typical pull-up current vs V_{DD} @ 4 temperatures*, – the rows for T_R/T_F, Fast I/Os, Load = 20 pF in *Table 38: I/O static characteristics*, – *Figure 47: LQFP32 marking example (package top view)*, – *Figure 50: UFQFPN32 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 55: SDIP32 marking example (package top view)*, – *Figure 58: TSSOP20 marking example (package top view)*, – *Figure 60: SO20 marking example (package top view)*.
26-Mar-2015	12	Corrected the values for “b” dimensions in *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.