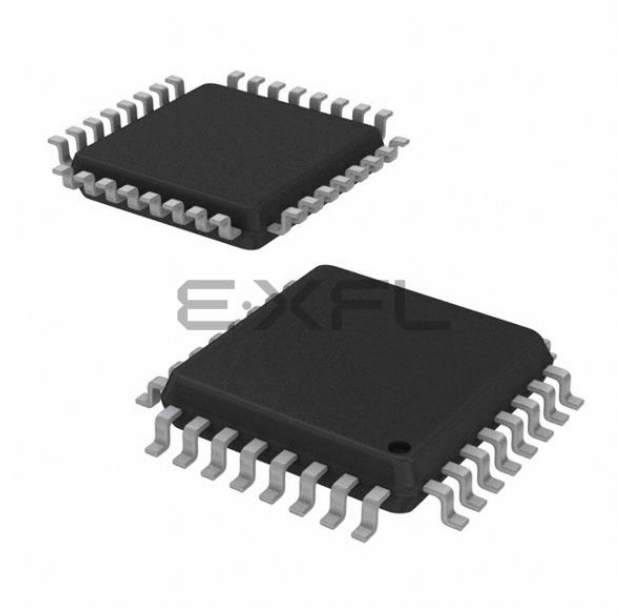

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103k3t3ctr

1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

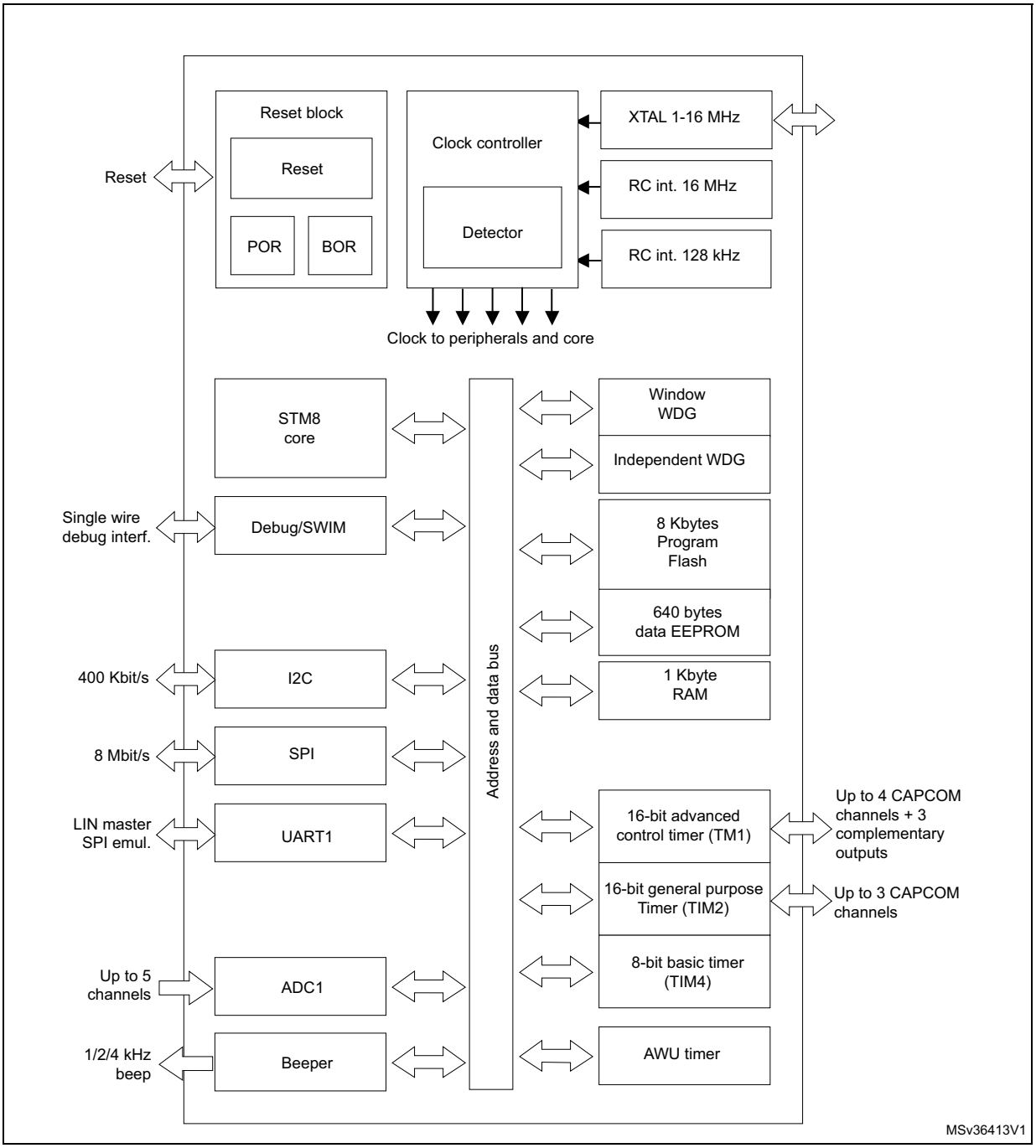
Table 1. STM8S103F2/x3 access line features

Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

3 Block diagram

Figure 1. STM8S103F2/x3 block diagram



Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

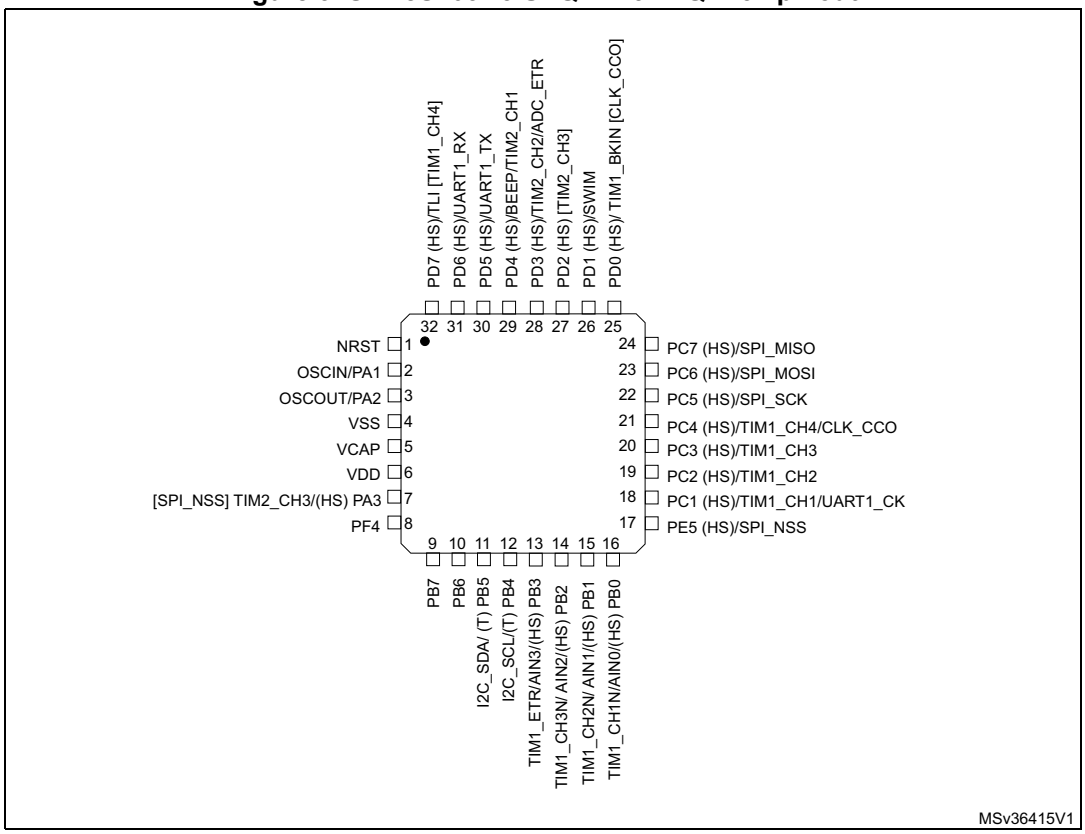
- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2 - 16-bit general purpose timer

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update

5.1 STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description

Figure 3. STM8S103K3 UFQFPN32/LQFP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8S103F2 and STM8S103F3 pin descriptions (continued)

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/[TIM1_ CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/[T IM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).1

Table 10. Interrupt mapping (continued)

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
21	Reserved	-	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1.

Table 12. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK:** External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

8.1 Alternate function remapping bits

Table 13. STM8S103K3 alternate function remapping bits for 32-pin devices

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 Reserved.
	AFR6 Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.(2) 1: Port D7 alternate function = TIM1_CH4.
	AFR5 Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.(2) 1: Port D0 alternate function = CLK_CCO.
	AFR[4:2] Alternate function remapping options 4:2 Reserved.
	AFR1 Alternate function remapping option 1 0: AFR1 remapping option inactive: Default alternate functions.(2) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3.
	AFR0 Alternate function remapping option 0 Reserved.

1. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.
2. Refer to pinout description.

Total current consumption in active halt mode

Table 25. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	300	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power down mode	LSI RC osc. (128 kHz)	10	20	40	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 26. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	290	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 30. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	400	-	µA
		V_{DD} = 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 31. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	130	
$I_{DD(TIM4)}$	TIM4 supply current(1)	50	
$I_{DD(UART1)}$	UART1 supply current (2)	120	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 33. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized)(3)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

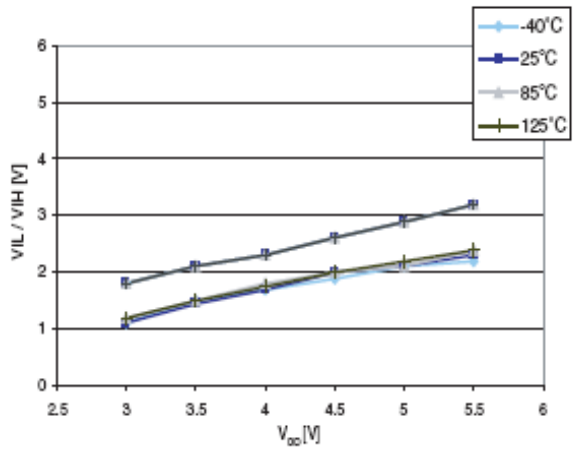


Figure 23. Typical pull-up current vs V_{DD} @ 4 temperatures

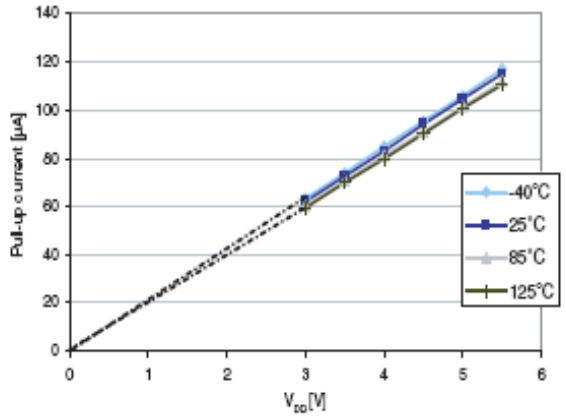


Figure 24. Typical pull-up resistance vs VDD @ 4 temperatures

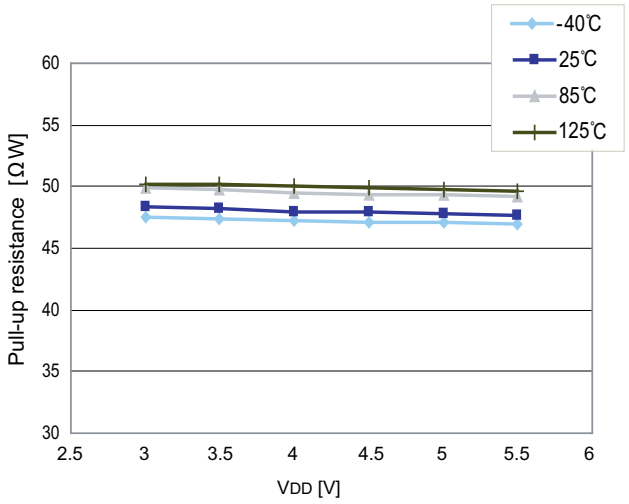


Table 39. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO}= 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO}= 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Guaranteed by characterization results

Table 40. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	1.0	V
	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.5(1)	
V_{OH}	Output high level with 2 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0(1)	

1. Guaranteed by characterization results

Table 41. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
		I_{IO}= 20 mA, V_{DD} = 5 V	-	1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO}= 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
		I_{IO}= 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Guaranteed by characterization results.

Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

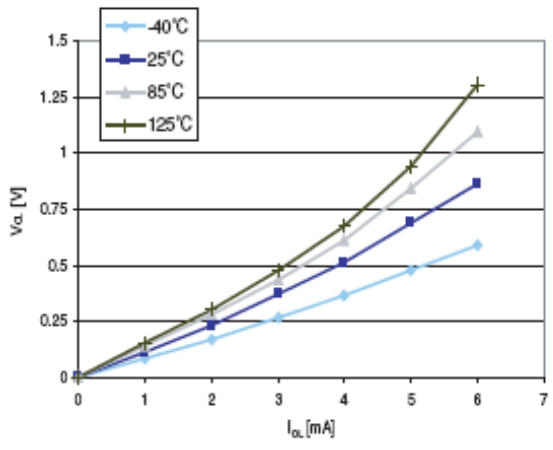


Figure 26. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

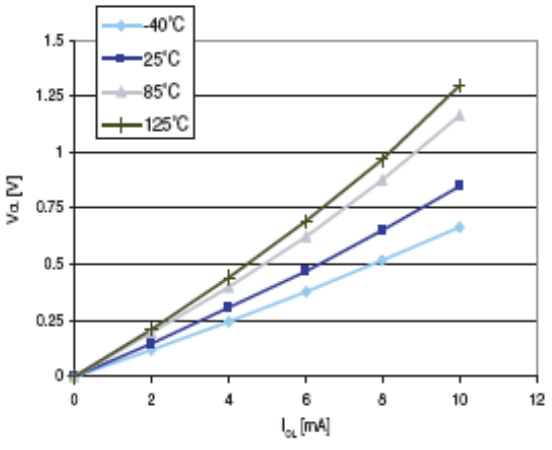
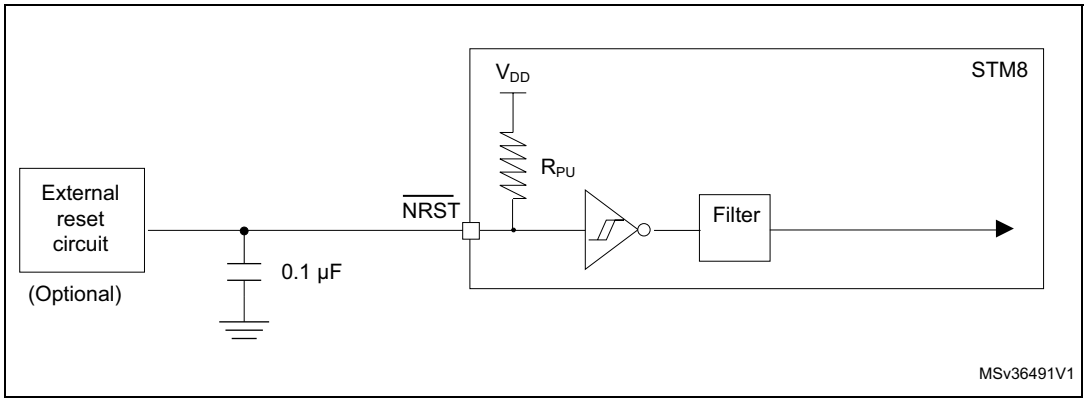


Figure 38. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	7	

Table 43. SPI characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$[2]	NSS setup time	Slave mode	4 * t_{MASTER}	-	
$t_{h(NSS)}$[2]	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2]	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$[2] $t_{su(SI)}$[2]	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$[2] $t_{h(SI)}$[2]	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$[2][3]	Data output access time	Slave mode	-	3* t_{MASTER}	
$t_{dis(SO)}$[2][4]	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$[2]	Data output valid time	Slave mode (after enable edge)	-	65	
$t_{v(MO)}$[2]	Data output valid time	Master mode (after enable edge)	-	30	
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	27	-	
$t_{h(MO)}$[2]		Master mode (after enable edge)	11	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 49. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		EMI level	2.5	2.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to SD22-C101 LQFP32 package	IV	1000	

1. Guaranteed by characterization results

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

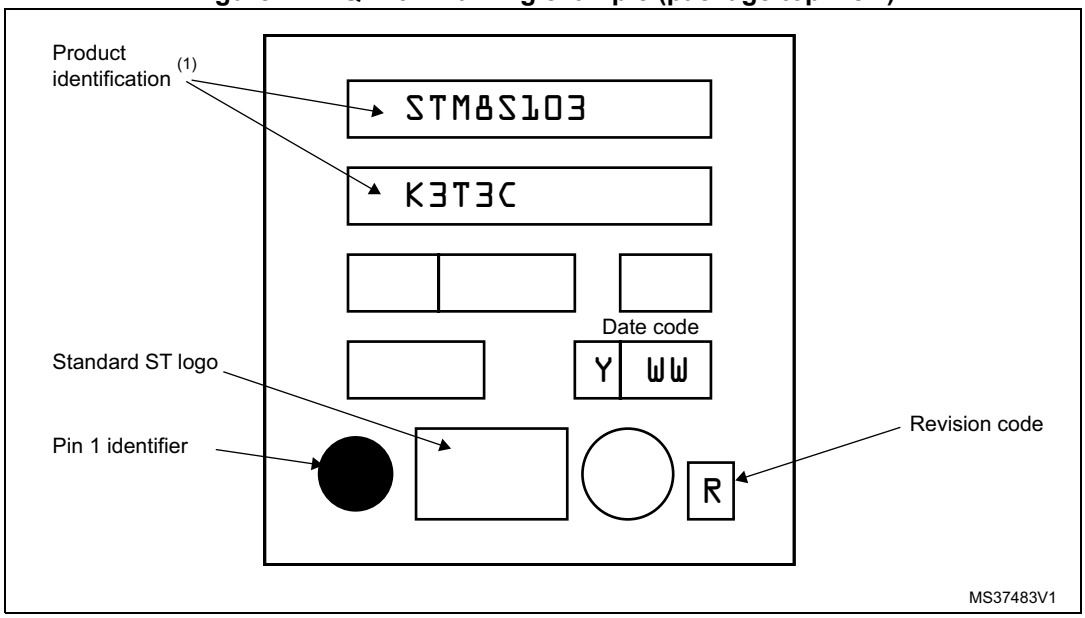
- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

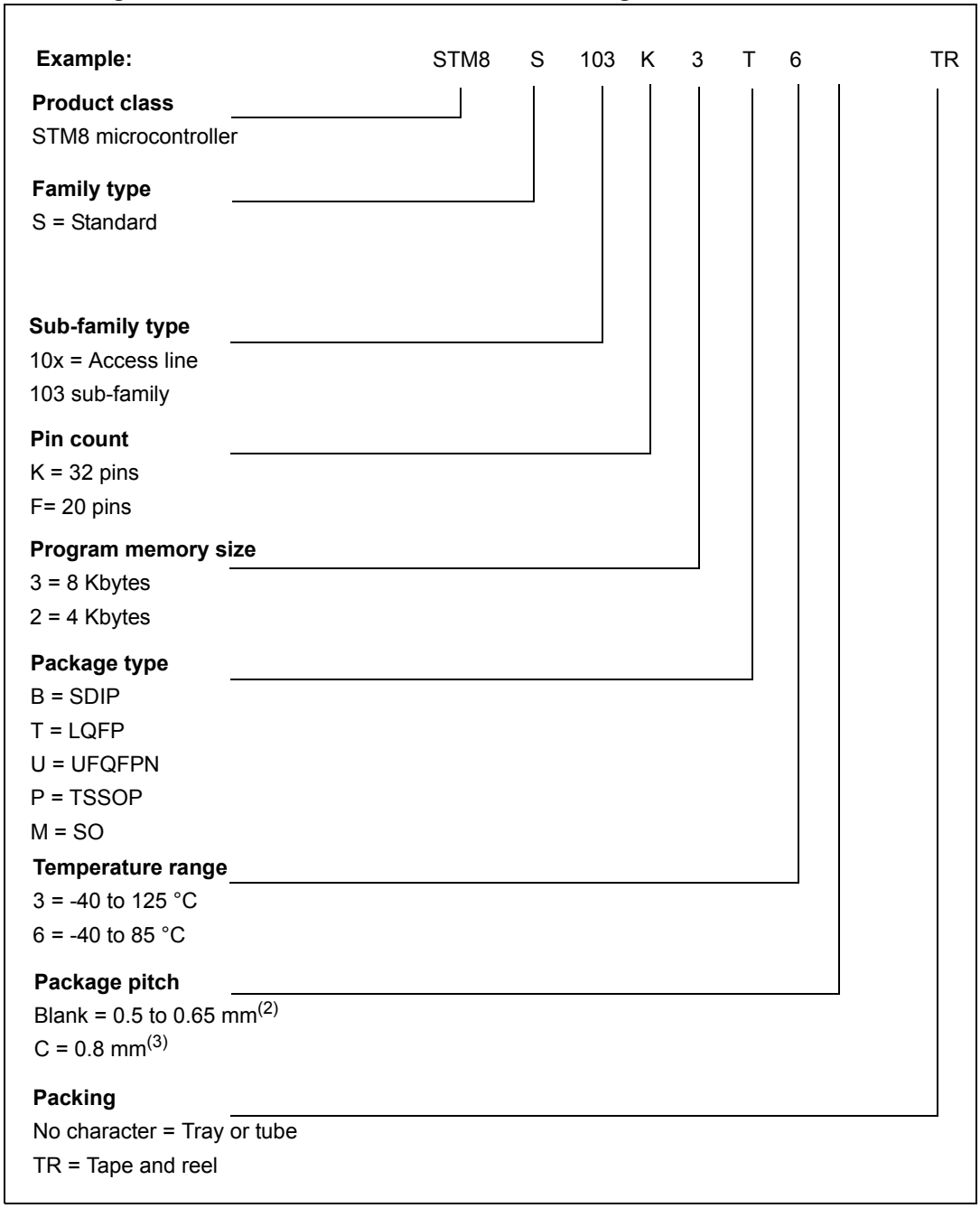
Figure 47. LQFP32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

13 Ordering information

Figure 63. STM8S103F2/x3 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....
Date:	.....
Signature:	.....

14 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

14.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

14.1.1 STice key features

- Occurrence and time profiling and code coverage (new features),
- Advanced breakpoints with up to 4 levels of conditions,
- Data breakpoints,
- Program and data trace recording up to 128 KB records,
- Read/write on the fly of memory during emulation,
- In-circuit debugging/programming via SWIM protocol,
- 8-bit probe analyzer,
- 1 input and 2 output triggers,
- Power supply follower managing application voltages between 1.62 to 5.5 V,
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements.
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.