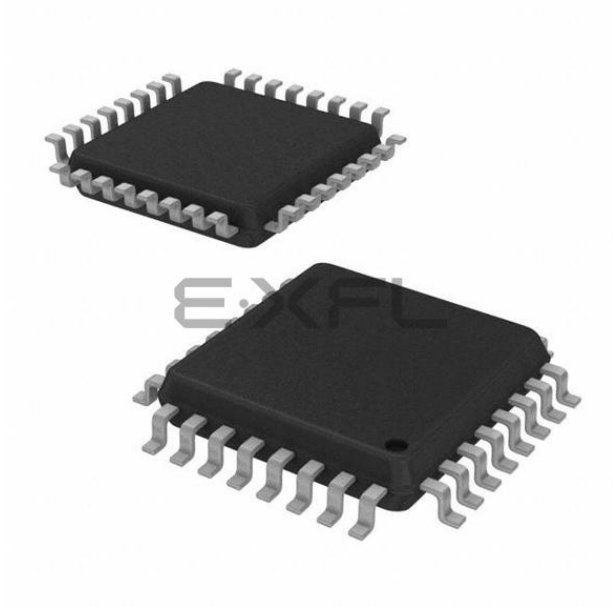

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103k3t6c

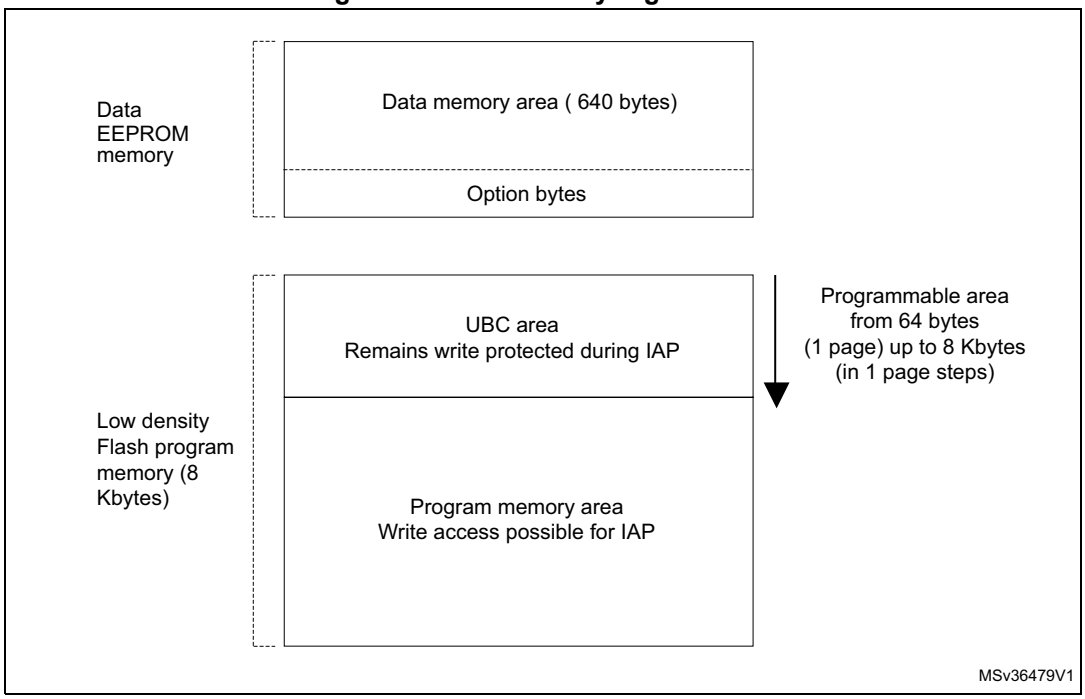
List of tables

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected Page 0 and 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory write-protected *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM:** High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

Table 17. Current characteristics (continued)

Symbol	Ratings	Max.(1)	Unit
$I_{INJ(PIN)}$ (3) (4)	Injected current on NRST pin	±4	mA
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(5)	±4	
ΣI_{INJ}(3)	Total injected current (sum of all I/O and control pins)(5)	±20	

1. Guaranteed by characterization results.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. I_{INJ} must never be exceeded. This condition is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

10.3 Operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 75 °C for suffix 6	TSSOP20	-	238	mW
		SO20W	-	220	
		UFQFPN20	-	220	
		LQFP32	-	330	
		UFQFPN32	-	526	
		SDIP32	-	330	

Table 19. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D(3)	Power dissipation at T_A = 125 °C for suffix 3	TSSOP20	-	59	mW
		SO20W	-	55	
		UFQFPN20	-	55	
		LQFP32	-	83	
		UFQFPN32	-	132	
		SDIP32	-	83	
T_A	Ambient temperature for suffix 6 version	Maximum power dissipation	-40	85	°C
T_A	Ambient temperature for suffix 3 version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version	-40	130	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax}- T_A)/\Theta_{JA}$ (see *Section 12: Thermal characteristics*) with the value for T_{Jmax} given in the previous table and the value for Θ_{JA} given in *Section 12: Thermal characteristics*

Figure 10. f_{CPUmax} versus V_{DD}

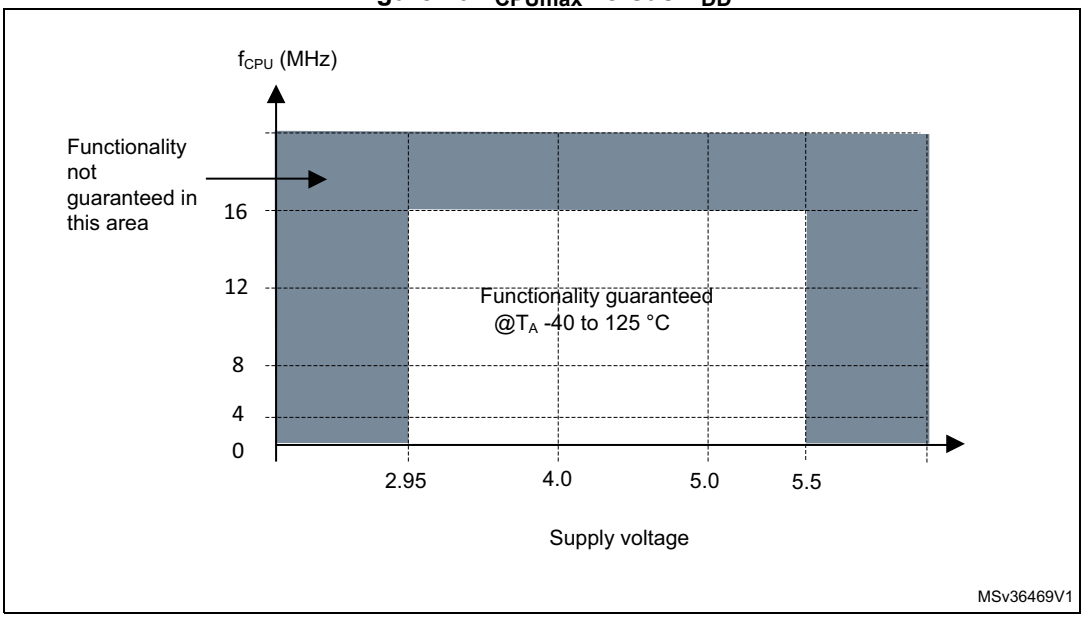


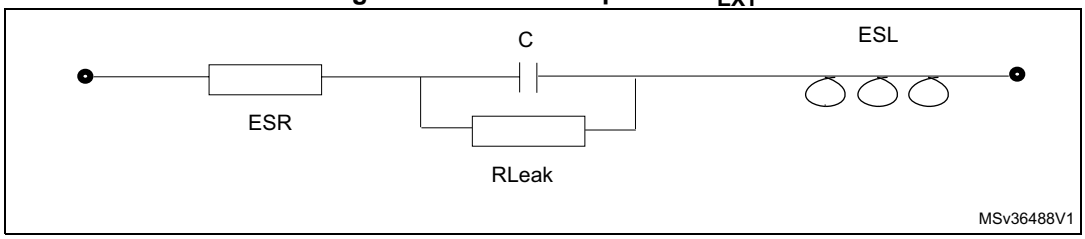
Table 20. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	∞	µs/V
	V_{DD} fall time rate(1)	-	2	-	∞	

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 19*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 9: Pin input voltage*.

Total supply current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 32. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source

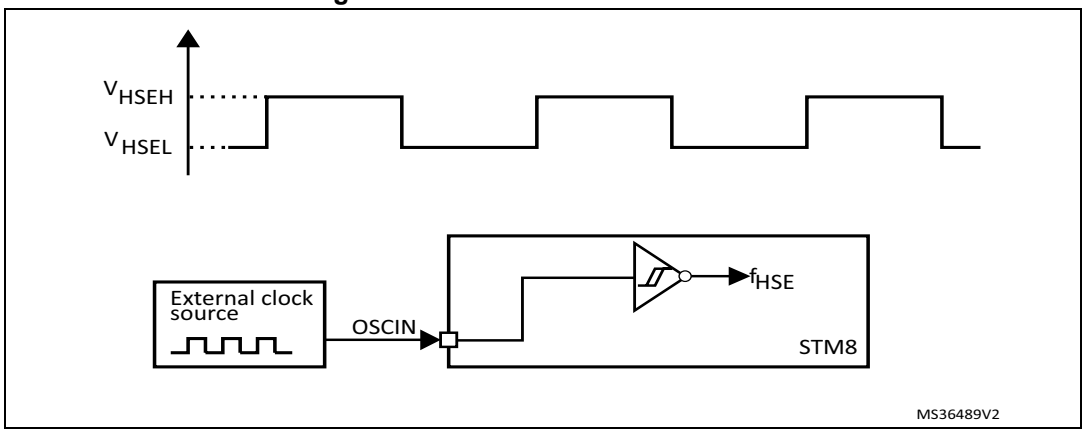


Figure 36. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

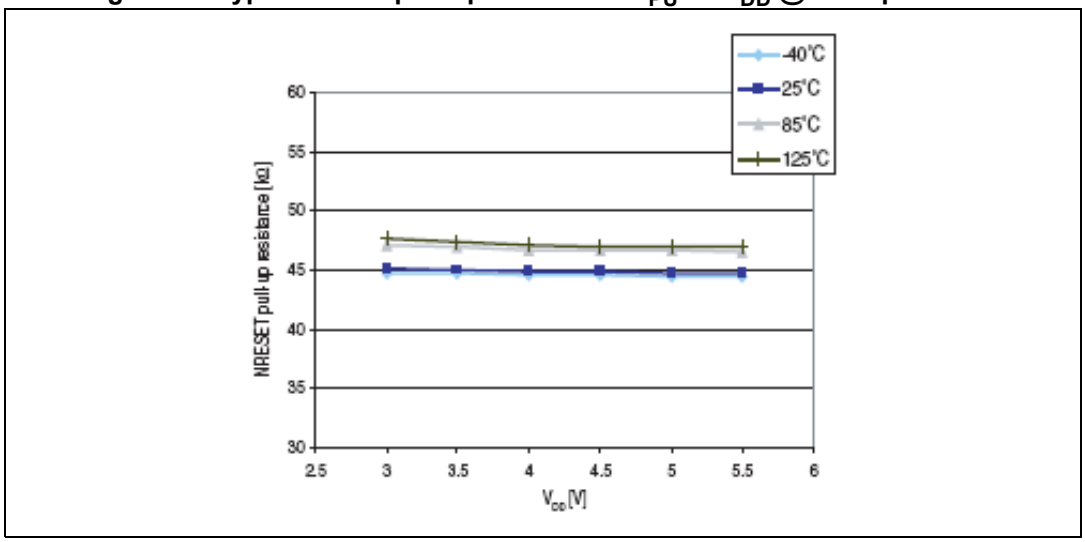
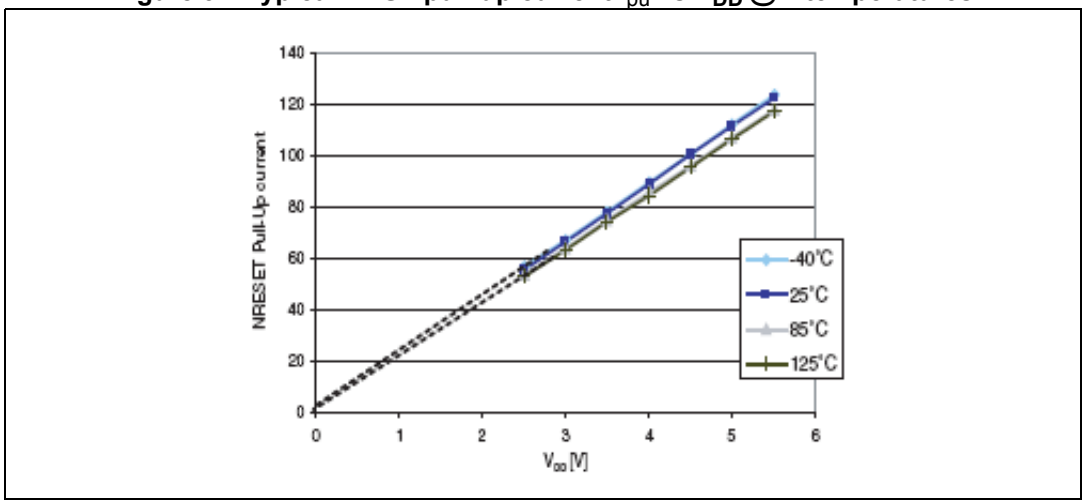


Figure 37. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 42: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.

Table 46. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	2.2	4	
		f_{ADC} = 6 MHz	2.4	4.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1.1	2.5	
		f_{ADC} = 4 MHz	1.5	3	
		f_{ADC} = 6 MHz	1.8	3	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.5	3	
		f_{ADC} = 4 MHz	2.1	3	
		f_{ADC} = 6 MHz	2.2	4	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	
		f_{ADC} = 6 MHz	0.8	2	

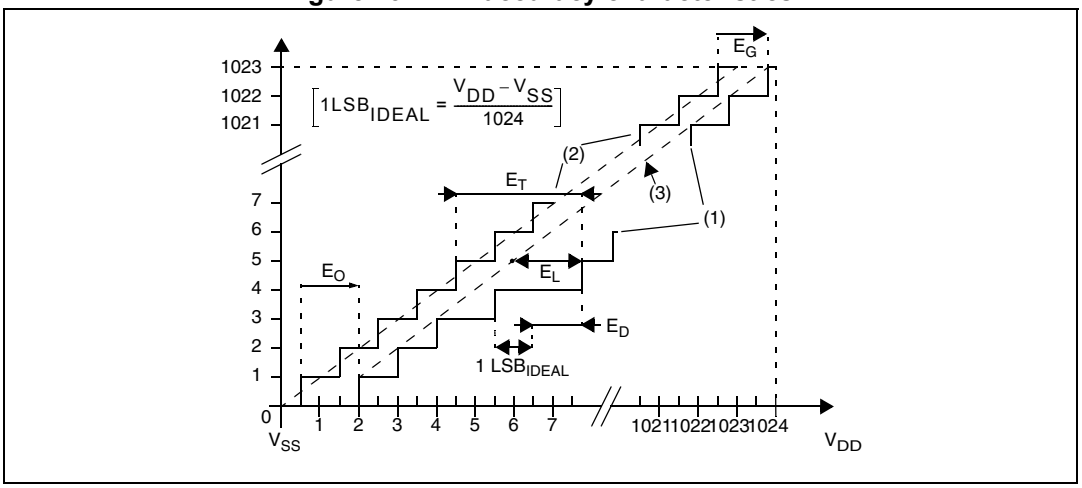
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Table 47. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

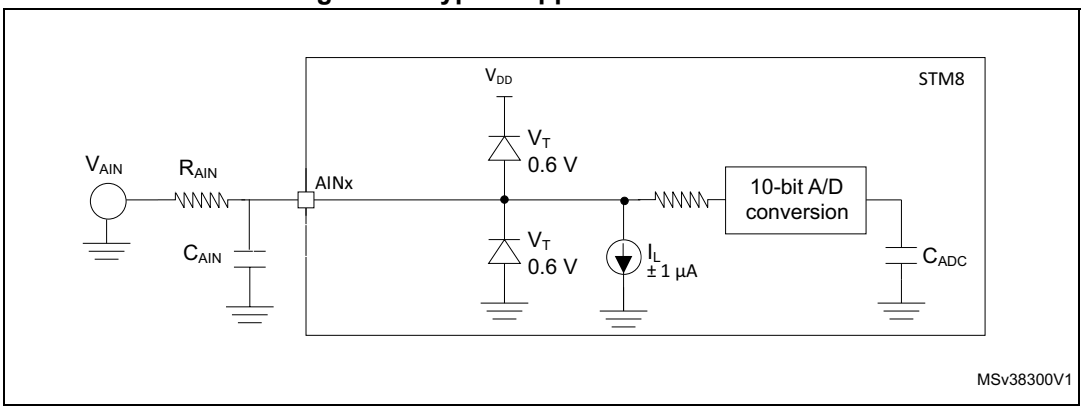
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Figure 43. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 44. Typical application with ADC



1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

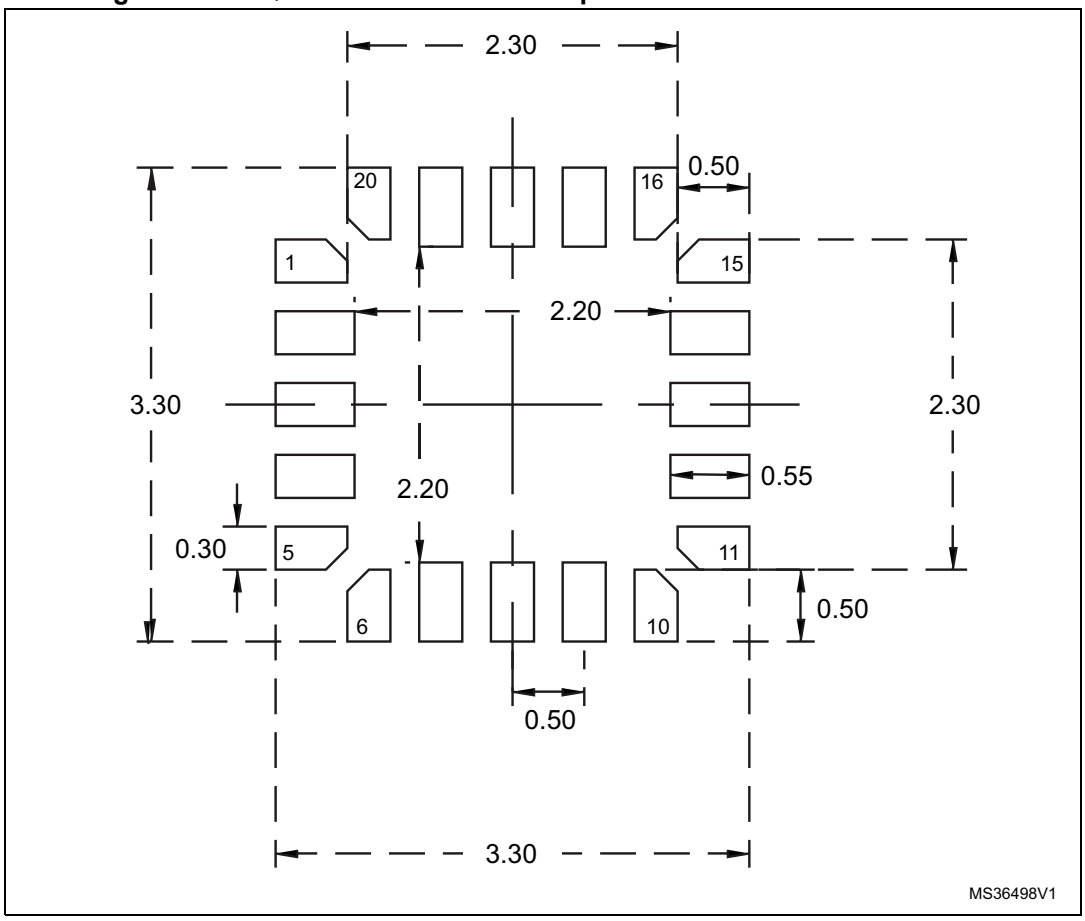
To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 48. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-4	4/A(1)

1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

Figure 62. UFQFPN recommended footprint without on-board emulation



12 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the device must never exceed the values specified in *Table 19: General operating conditions*, otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 58. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4.4mm	84	°C/W
	Thermal resistance junction-ambient SO20W (300 mils)	91	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm	90	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm	60	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm	38	
	Thermal resistance junction-ambient SDIP32 - 400 mils	60	

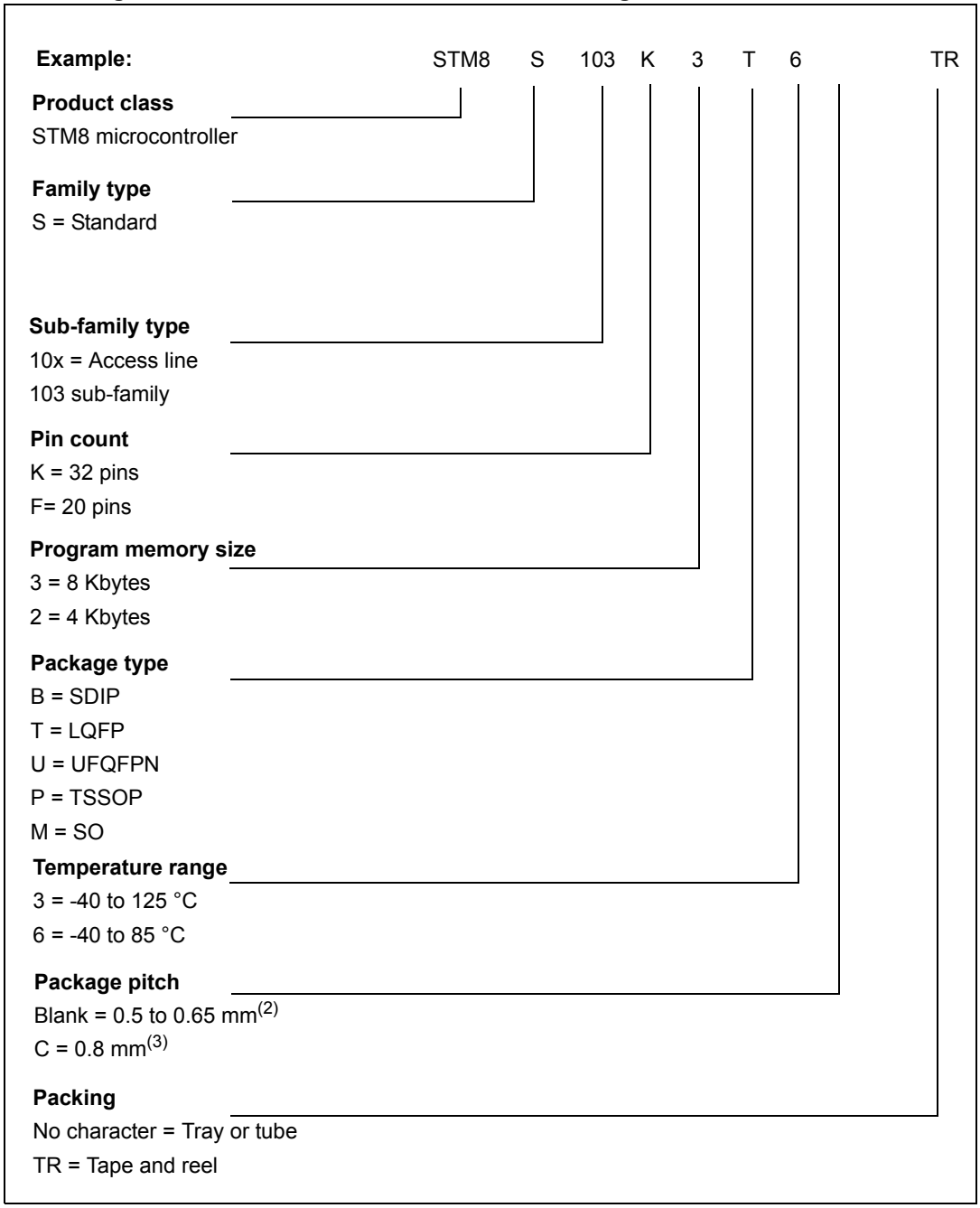
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

13 Ordering information

Figure 63. STM8S103F2/x3 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

Table 59. Document revision history

Date	Revision	Changes
16-Oct-1999	4	Replaced VFQFPN32 package by UFQFPN32 package. – *Section 4.5: Clock controller*: replaced TIM2 and TIM3 with reserved and TIM2 respectively in *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers* – *Total current consumption in halt mode*: changed the maximum current consumption limit at 125 °C (and VDD= 5 V) from 35 µA to 55 µA. – *Functional EMS (electromagnetic susceptibility)*: renamed ESD as FESD (functional); added name of AN1709; replaced EC 1000 with IEC 61000. – *Designing hardened software to avoid noise problems*: replaced IEC 1000 with IEC 61000, added title of AN1015, and added footnote to EMS data table. – *Electromagnetic interference (EMI)*: replaced J 1752/3 with IEC 61967-2 and updated data of the EMI data table. – *Section 12.2: Selecting the product temperature range*: changed the value of LQFP32 7x7 mm thermal resistance from 59 °C/W to 60 °C/W. Added *Section 13.1: STM8S103 FASTROM microcontroller option list*.
22-Apr-2010	5	Added VFQFPN32 and SO20 packages. Updated Px_IDR reset value in *Table 7: I/O port hardware register map*. – *Section 10.3: Operating conditions*: updated VCAP and ESR low limit, added ESL parameter, and Note 1 below *Table 19: General operating conditions* Updated ACCHSI in *Table 34: HSI oscillator characteristics*. Modified IDD(H)inand. Removed note 3 related to Accuracy of HSI oscillator. Updated maximum power dissipation in *Table 19: General operating conditions*. Updated *Section 12: Thermal characteristics* Replaced package pitch digit by VFQFPN/UFQFPN package digit in *Figure 63: STM8S103F2/x3 access line ordering information scheme*[(1)], and removed note 1.

Table 59. Document revision history

Date	Revision	Changes
09-Sep-2010	6	Removed VFQFPN32 package. Removed internal reference voltage from *Section 4.13: Analog-to-digital converter (ADC1)*. Updated the reset state information in *Table 4: Legend/abbreviations for pin description tables* in *Section 5: Pinout and pin description*. Added footnote to PD1/SWIM pin in *Table 5: STM8S103K3 pin descriptions*. Updated pins 14 and 19 (TSSOP20/SO20) / pins 11 and 16 (UFQFPN20) in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions*. Standardized all reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*. Updated AFR2 description of OPT 2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*s. Replaced 0.01 µF with 0.1 µf in *Figure 38: Recommended reset pin protection*. Added *Figure 42: Typical application with I^2C bus and timing diagram* and *Table 44: I^2C characteristics*. Updated footnote 1 in *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated the Special marking section in *Section 13.1: STM8S103 FASTROM microcontroller option list*: Updated AFR2 description of OTP2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices* Updated existing footnote and added three additional footnotes to *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*
12-Jul-2011	7	Updated the note related to true open-drain outputs in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* Removed CLK_CANCCR register from *Table 8: General hardware register map*. Added note for Px_IDR registers in *Table 7: I/O port hardware register map*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 38: Recommended reset pin protection*. Removed typical HSI accuracy curve in *Section 10.3.4: Internal clock sources and timing characteristics*. Renamed package type 2 into package pitch and added pitch code “C” in *Figure 63: STM8S103F2/x3 access line ordering information scheme(1)* and added UFQFPN20 in *Section 13.1: STM8S103 FASTROM microcontroller option list*. Updated the disclaimer.

Table 59. Document revision history

Date	Revision	Changes
04-Apr-2012	8	Updated notes related to V_{CAP} in *Table 19: General operating conditions*. Added values of t_R/t_F for 50 pF load capacitance, and updated note in *Table 38: I/O static characteristics*. Updated typical and maximum values of R_{PU} in *Table 38: I/O static characteristics* and *Table 42: NRST pin characteristics*. Changed SCK input to SCK output in *Section 10.3.8: SPI serial peripheral interface* Modified *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* to add package top view.
26-Jun-2012	9	Added *Section 11.4: SDIP32 package information*.
04-Feb-2015	10	Updated *Section 11.5: TSSOP20 package information* and *Section 11.3: UFQFPN20 package information*.
10-Mar-2015	11	Updated: – *Table 34: HSI oscillator characteristics*: corrected HSI oscillator accuracy (factory calibrated) for V_{DD} = 5 V and T_A = 25 °C. – *Table 38: I/O static characteristics*: corrected the max. value for T_R/T_F, Fast I/Os, Load = 50 pF. Added: – *Figure 23: Typical pull-up current vs V_{DD} @ 4 temperatures*, – the rows for T_R/T_F, Fast I/Os, Load = 20 pF in *Table 38: I/O static characteristics*, – *Figure 47: LQFP32 marking example (package top view)*, – *Figure 50: UFQFPN32 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 55: SDIP32 marking example (package top view)*, – *Figure 58: TSSOP20 marking example (package top view)*, – *Figure 60: SO20 marking example (package top view)*.
26-Mar-2015	12	Corrected the values for “b” dimensions in *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.

Table 59. Document revision history

Date	Revision	Changes
03-Oct-2016	13	Updated: – Name of “LQFP32 package” to “LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package” on *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 46: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint* – *Section 10.2: Absolute maximum ratings* – *Section 10.3.10: 10-bit ADC characteristics* – *Figure 40: SPI timing diagram where slave mode and CPHA = 1* – *Figure 41: SPI timing diagram - master mode* – *Figure 43: ADC accuracy characteristics* – *Figure 63: STM8S103F2/x3 access line ordering information scheme*(1): corrected package name from VFQFPN to UFQFPN – *Table 8: General hardware register map* – *Table 16: Voltage characteristics* – *Table 17: Current characteristics* – *Table 19: General operating conditions* – *Table 20: Operating conditions at power-up/power-down* – *Table 21: Total current consumption with code execution in run mode at V_{DD} = 5 V* – *Table 31: Peripheral current consumption* – *Table 49: EMI data* – Updated footnotes on *Table 18: Thermal characteristics*, *Table 38: I/O static characteristics*, *Table 43: SPI characteristics*, *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline*, *Figure 48: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*. – Updated all the “Device marking” sections on *Section 11: Package information*
13-Feb-2017	14	Updated: – *Section 10.2: Absolute maximum ratings* – *Section 11.3: UFQFPN20 package information* – *Table 5: STM8S103K3 pin descriptions* – *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* – *Table 21: Total current consumption with code execution in run mode at V_{DD} = 5 V* – Footnotes in all tables of *Section 10: Electrical characteristics* Added: – *Figure 52: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint*