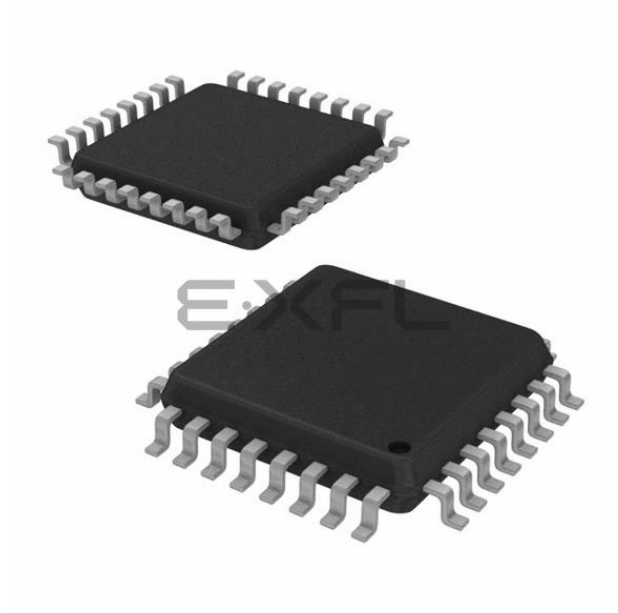


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 640 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.95V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103k3t6ctr |

# List of tables

# 1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

# 4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

## 4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

### Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

### Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

### Instruction set

- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

## 4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

### Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

**Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers**

| Bit | Peripheral clock | Bit | Peripheral clock | Bit | Peripheral clock | Bit | Peripheral clock |
|---|---|---|---|---|---|---|---|
| PCKEN17 | TIM1 | PCKEN13 | UART1 | PCKEN27 | Reserved | PCKEN23 | ADC |
| PCKEN16 | Reserved | PCKEN12 | Reserved | PCKEN26 | Reserved | PCKEN22 | AWU |
| PCKEN15 | TIM2 | PCKEN11 | SPI | PCKEN25 | Reserved | PCKEN21 | Reserved |
| PCKEN14 | TIM4 | PCKEN10 | I2C | PCKEN24 | Reserved | PCKEN20 | Reserved |

## 4.12 TIM4 - 8-bit basic timer

- 8-bit auto reload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

**Table 3. TIM timer features**

| Timer | Counter size (bits) | Prescaler | Counting mode | CAPCOM channels | Complementary outputs | Ext. trigger | Timer synchronization/ chaining |
|---|---|---|---|---|---|---|---|
| TIM1 | 16 | Any integer from 1 to 65536 | Up/down | 4 | 3 | Yes | No |
| TIM2 | 16 | Any power of 2 from 1 to 32768 | Up | 3 | 0 | No | |
| TIM4 | 8 | Any power of 2 from 1 to 128 | Up | 0 | 0 | No | |

## 4.13 Analog-to-digital converter (ADC1)

The STM8S103F2/x3 family products contain a 10-bit successive approximation A/D converter (ADC1) with up to 5 external multiplexed input channels and the following main features:

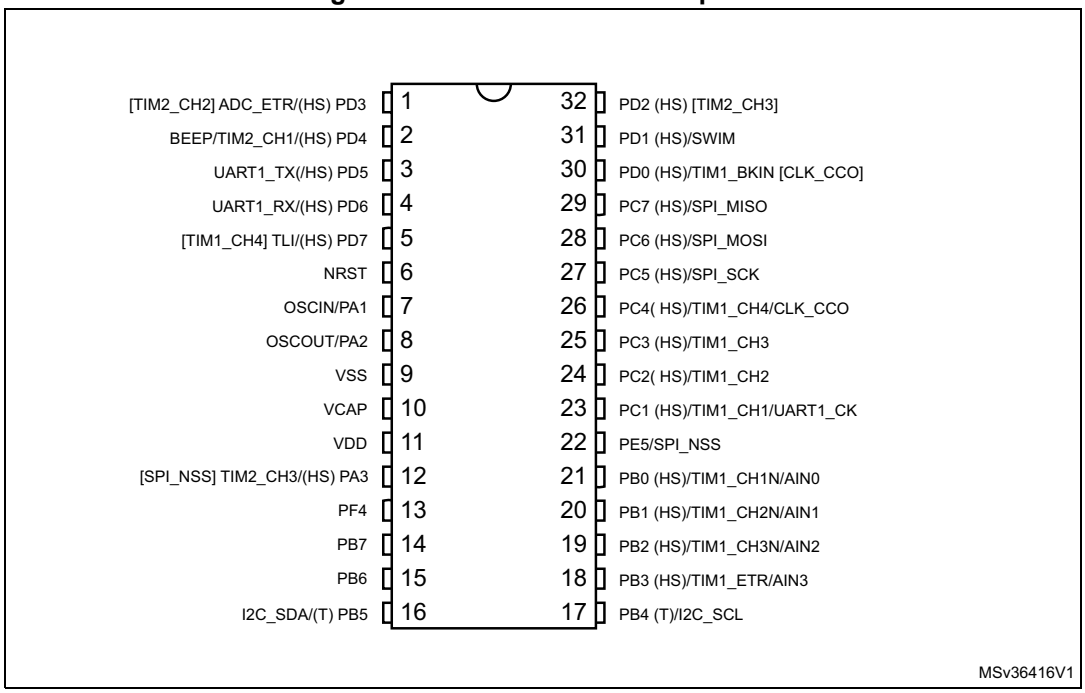
- Input voltage range: 0 to VDD
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

## 4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.1 master capability
- SPI: Full and half-duplex, 8 Mbit/s
- I²C: Up to 400 kbit/s

**Figure 4. STM8S103K3 SDIP32 pinout**




1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to $V_{DD}$ not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

**Table 5. STM8S103K3 pin descriptions**

| SDIP32 | LQFP/ UFQFP32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 6 | 1 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | - |
| 7 | 2 | PA1/ OSCIN(2) | I/O | **X** | X | X | - | O1 | X | X | Port A1 | Resonator/ crystal in | - |
| 8 | 3 | PA2/ OSCOUT | I/O | **X** | X | X | - | O1 | X | X | Port A2 | Resonator/ crystal out | - |
| 9 | 4 | VSS | S | - | - | - | - | - | - | - | Digital ground | | - |
| 10 | 5 | VCAP | S | - | - | - | - | - | - | | 1.8 V regulator capacitor | | - |
| 11 | 6 | VDD | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 12 | 7 | PA3/ TIM2_CH3 [SPI_NSS] | I/O | **X** | X | X | HS | O3 | X | X | Port A3 | Timer 2 channel 3 | SPI master/ slave select [AFR1] |
| 13 | 8 | PF4 | I/O | **X** | X | - | - | O1 | X | X | Port F4 | - | - |
| 14 | 9 | PB7 | I/O | **X** | X | X | - | O1 | X | X | Port B7 | - | - |

**Table 8. General hardware register map (continued)**

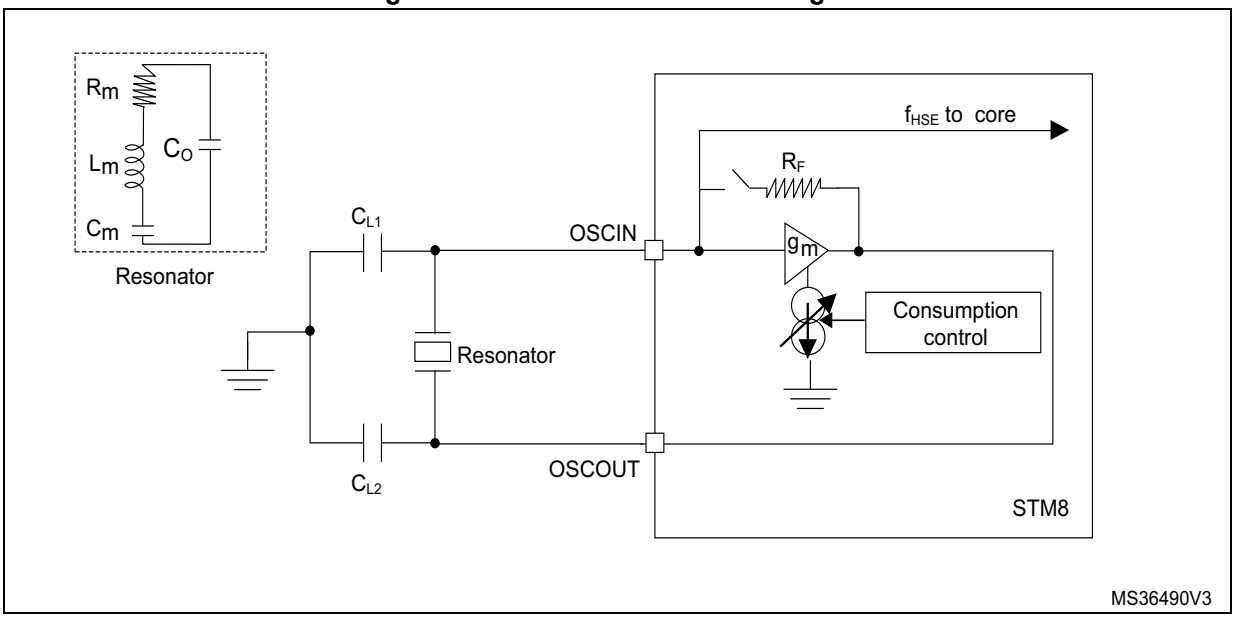
| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50C3 | CLK | CLK_CMSR | Clock master status register | 0xE1 |
| 0x00 50C4 | | CLK_SWR | Clock master switch register | 0xE1 |
| 0x00 50C5 | | CLK_SWCR | Clock switch control register | 0xXX |
| 0x00 50C6 | | CLK_CKDIVR | Clock divider register | 0x18 |
| 0x00 50C7 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0xFF |
| 0x00 50C8 | | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50C9 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50CA | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0xFF |
| 0x00 50CC | | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 |
| 0x00 50CE to 0x00 50D0 | Reserved area (3 byte) | | | |
| 0x00 50D1 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D3 to 00 50DF | Reserved area (13 byte) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX(2) |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 byte) | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/status register 1 | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 50FF | Reserved area (12 byte) | | | |
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 | | SPI_CRCPR | SPI CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI_RXCRCR | SPI Rx CRC register | 0xFF |
| 0x00 5207 | | SPI_TXCRCR | SPI Tx CRC register | 0xFF |

**Table 8. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5400 | ADC1 cont'd | ADC_CSR | ADC control/status register | 0x00 |
| 0x00 5401 | | ADC_CR1 | ADC configuration register 1 | 0x00 |
| 0x00 5402 | | ADC_CR2 | ADC configuration register 2 | 0x00 |
| 0x00 5403 | | ADC_CR3 | ADC configuration register 3 | 0x00 |
| 0x00 5404 | | ADC_DRH | ADC data register high | 0xXX |
| 0x00 5405 | | ADC_DRL | ADC data register low | 0xXX |
| 0x00 5406 | | ADC_TDRH | ADC Schmitt trigger disable register high | 0x00 |
| 0x00 5407 | | ADC_TDRL | ADC Schmitt trigger disable register low | 0x00 |
| 0x00 5408 | | ADC_HTRH | ADC high threshold register high | 0x03 |
| 0x00 5409 | | ADC_HTRL | ADC high threshold register low | 0xFF |
| 0x00 540A | | ADC_LTRH | ADC low threshold register high | 0x00 |
| 0x00 540B | | ADC_LTRL | ADC low threshold register low | 0x00 |
| 0x00 540C | | ADC_AWSRH | ADC analog watchdog status register high | 0x00 |
| 0x00 540D | | ADC_AWSRL | ADC analog watchdog status register low | 0x00 |
| 0x00 540E | | ADC _AWCRH | ADC analog watchdog control register high | 0x00 |
| 0x00 540F | | ADC_AWCRL | ADC analog watchdog control register low | 0x00 |
| 0x00 5410 to 0x00 57FF | Reserved area (1008 byte) | | | |

1. Depends on the previous reset source.
2. Write-only register.

**Figure 19. HSE oscillator circuit diagram**

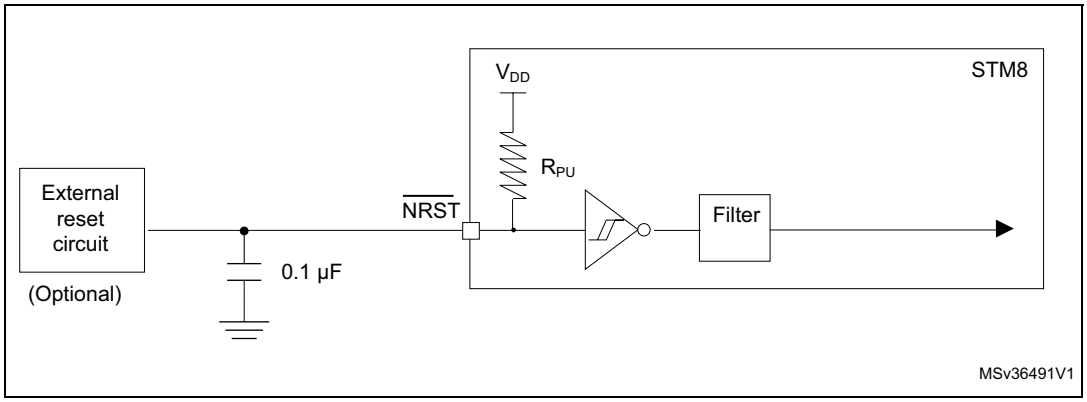



### HSE oscillator critical $g_m$ equation

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

$R_m$: Notional resistance (see crystal specification)
$L_m$: Notional inductance (see crystal specification)
$C_m$: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m \gg g_{mcrit}$

**Figure 38. Recommended reset pin protection**




### 10.3.8 SPI serial peripheral interface

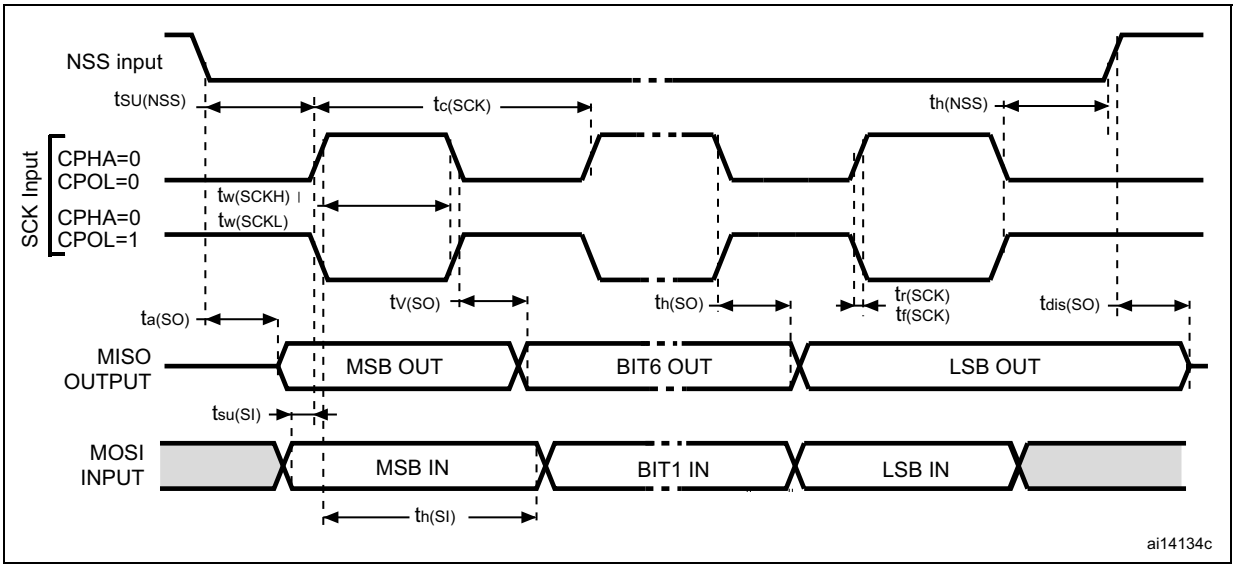
Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency and $V_{DD}$ supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 43. SPI characteristics**

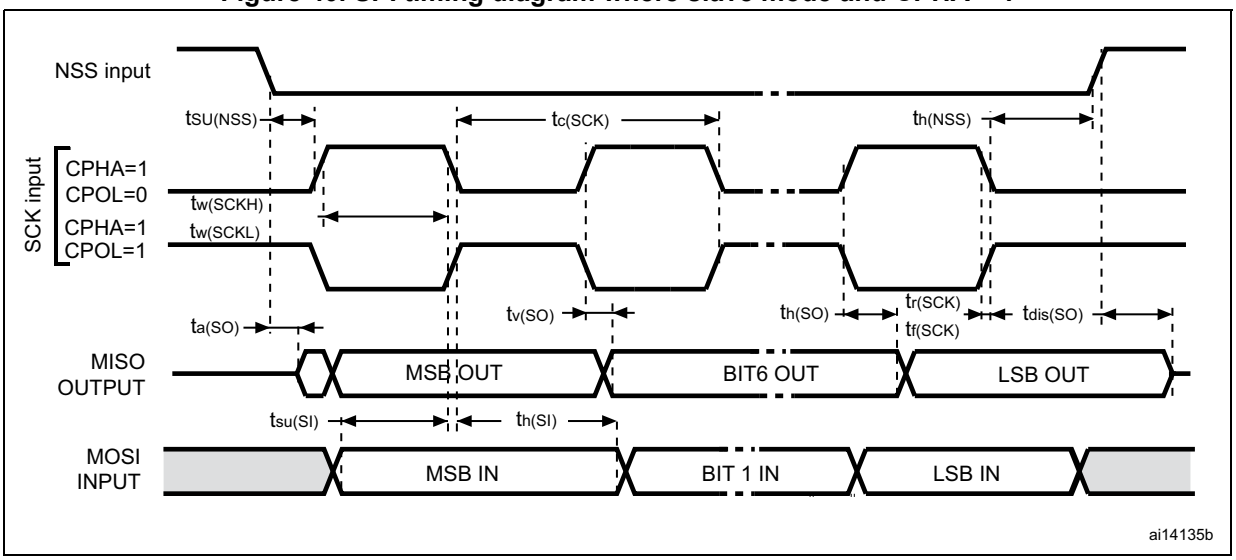
| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 7 | |

**Figure 39. SPI timing diagram where slave mode and CPHA = 0**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 40. SPI timing diagram where slave mode and CPHA = 1**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

## 10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

***Prequalification trials***

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

**Table 48. EMS data**

| Symbol | Parameter | Conditions | Level/class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$= 25 °C, $f_{MASTER}$ = 16 MHz (HSI clock), Conforms to IEC 61000-4-2 | 2/B(1) |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$= 25 °C, $f_{MASTER}$ = 16 MHz (HSI clock), Conforms to IEC 61000-4-4 | 4/A(1) |

1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 51. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = 25 °C | A |
| | | $T_A$ = 85 °C | |
| | | $T_A$ = 125 °C | |

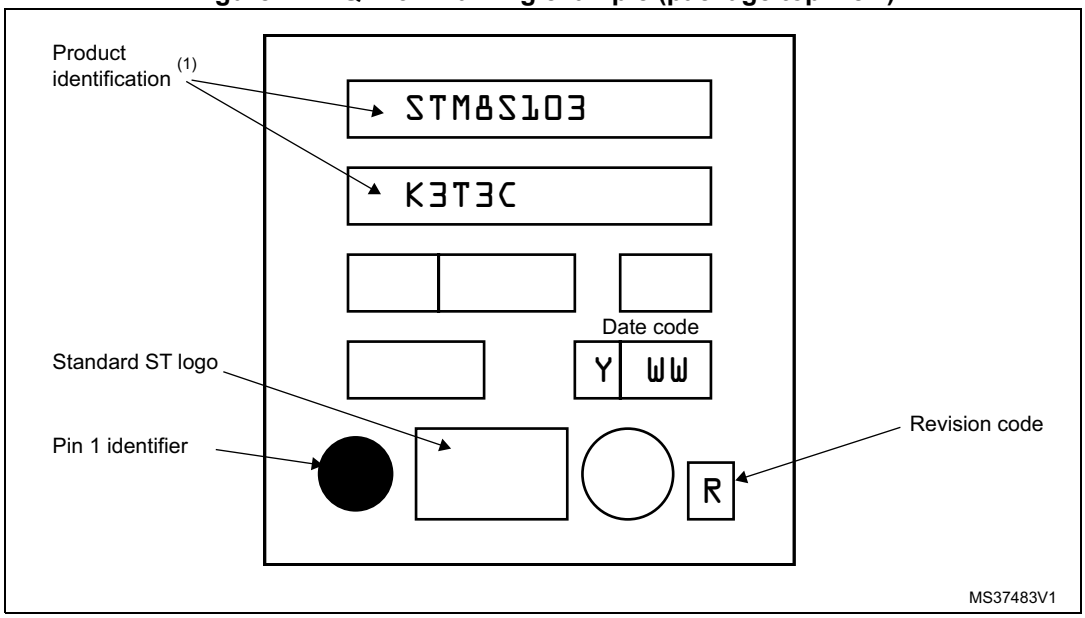
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 47. LQFP32 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

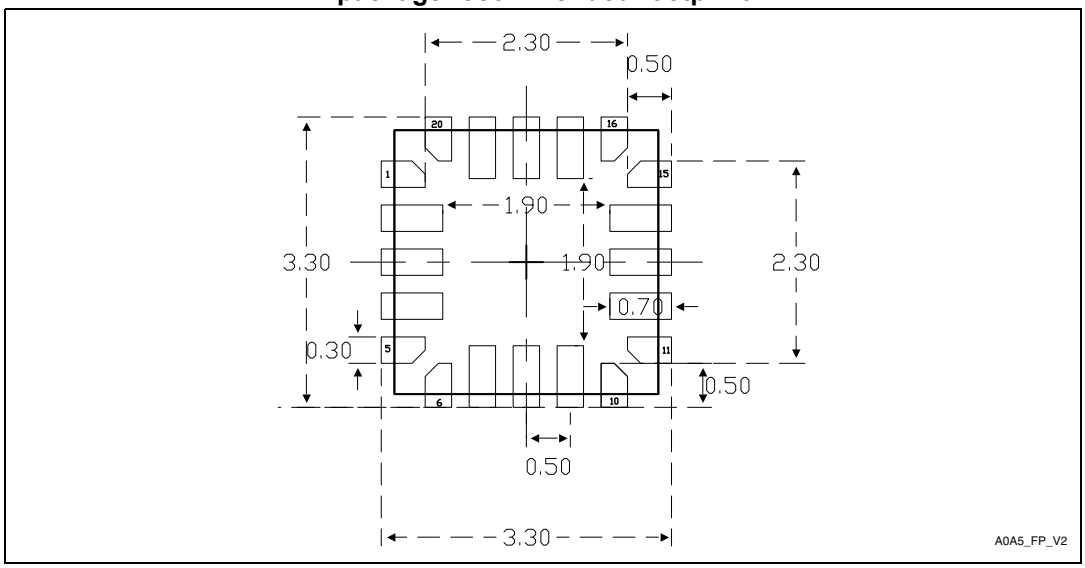
**Table 54. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)**

| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| L3 | - | 0.375 | - | - | 0.0148 | - |
| L4 | - | 0.200 | - | - | 0.0079 | - |
| L5 | - | 0.150 | - | - | 0.0059 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits

*Section 11.7: UFQFPN recommended footprint* shows the recommended footprints for UFQFPN with and without on-board emulation.

**Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**



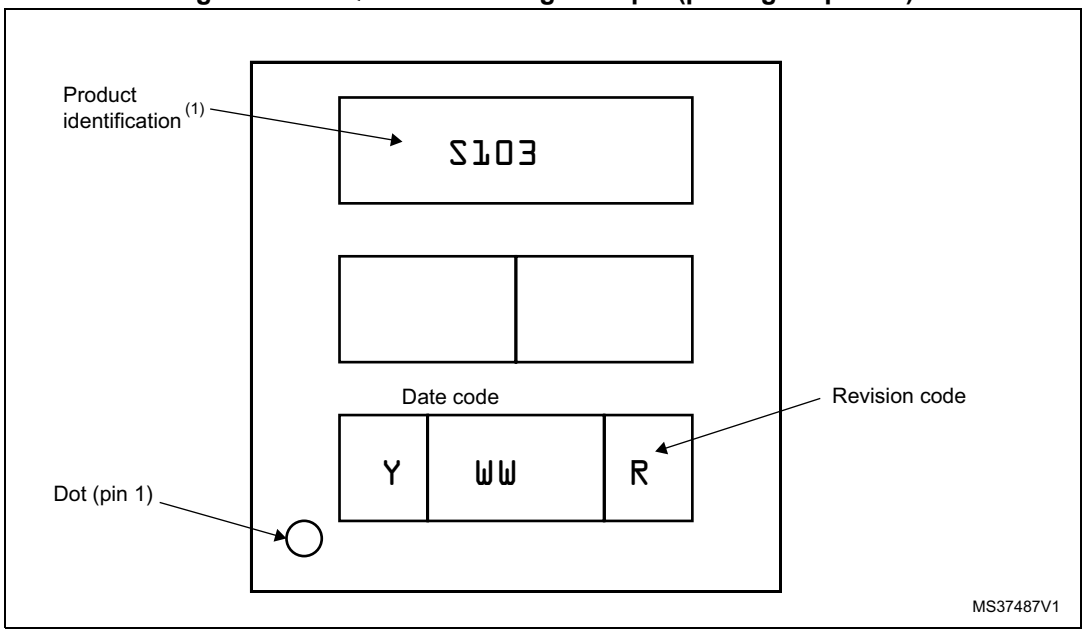

1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 53. UFQFPN20 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 55. SDIP32 package mechanical data (continued)**

| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| eB | - | - | 12.700 | - | - | 0.5000 |
| L | 2.540 | 3.048 | 3.810 | 0.1000 | 0.1200 | 0.1500 |

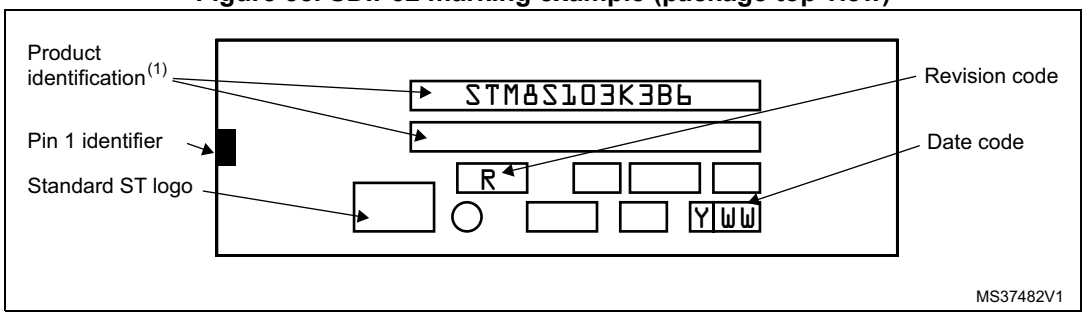
1. Values in inches are converted from mm and rounded to 4 decimal digits

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 55. SDIP32 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

## 13.1 STM8S103 FASTROM microcontroller option list

(last update: April 2010)

| | |
|---|---|
| Customer | ..... |
| Address | ..... |
| Contact | ..... |
| Phone number | ..... |
| FASTROM code reference(1) | ..... |

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

*Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.*

### Device type/memory size/package (check only one option)

| FASTROM device | 4 Kbyte | 8 Kbyte |
|---|---|---|
| LQFP32 | - | [ ] STM8S103K3 |
| UFQFPN20 | [ ] STM8S103F2 | [ ] STM8S103F3 |
| UFQFPN32 | - | [ ] STM8S103K3 |
| TSSOP20 | [ ] STM8S103F2 | [ ] STM8S103F3 |
| SO20W | [ ] STM8S103F2 | [ ] STM8S103F3 |

### Conditioning (check only one option)

[ ] Tape and reel or [ ] Tray

### Special marking (check only one option)

[ ] No [ ] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

UFQFPN20: 1 line of 4 characters max: “_ _ _ _”

UFQFPN32: 1 line of 7 characters max: “_ _ _ _ _ _ _”

LQFP32: 2 lines of 7 characters max: “_ _ _ _ _ _ _” and “_ _ _ _ _ _ _”

TSSOP20/SO20: 1 line of 10 characters max: “_ _ _ _ _ _ _ _ _ _”

Three characters are reserved for code identification.

**Table 59. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 09-Sep-2010 | 6 | Removed VFQFPN32 package.<br>Removed internal reference voltage from *Section 4.13: Analog-to-digital converter (ADC1)*.<br>Updated the reset state information in *Table 4: Legend/abbreviations for pin description tables* in *Section 5: Pinout and pin description*.<br>Added footnote to PD1/SWIM pin in *Table 5: STM8S103K3 pin descriptions*.<br>Updated pins 14 and 19 (TSSOP20/SO20) / pins 11 and 16 (UFQFPN20) in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions*.<br>Standardized all reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*.<br>Updated AFR2 description of OPT 2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*s.<br>Replaced 0.01 µF with 0.1 µf in *Figure 38: Recommended reset pin protection*.<br>Added *Figure 42: Typical application with $I^2C$ bus and timing diagram* and *Table 44: $I^2C$ characteristics*.<br>Updated footnote 1 in *Table 46: ADC accuracy with $R_{AIN}$< 10 kΩ $V_{DD}$= 5 V* and *Table 47: ADC accuracy with $R_{AIN}$< 10 kΩ $V_{DD}$= 3.3 V*.<br>Updated the Special marking section in *Section 13.1: STM8S103 FASTROM microcontroller option list*:<br>Updated AFR2 description of OTP2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*<br>Updated existing footnote and added three additional footnotes to *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data* |
| 12-Jul-2011 | 7 | Updated the note related to true open-drain outputs in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions*<br>Removed CLK_CANCCR register from *Table 8: General hardware register map*.<br>Added note for Px_IDR registers in *Table 7: I/O port hardware register map*.<br>Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 38: Recommended reset pin protection*.<br>Removed typical HSI accuracy curve in *Section 10.3.4: Internal clock sources and timing characteristics*.<br>Renamed package type 2 into package pitch and added pitch code “C” in *Figure 63: STM8S103F2/x3 access line ordering information scheme(1)* and added UFQFPN20 in *Section 13.1: STM8S103 FASTROM microcontroller option list*.<br>Updated the disclaimer. |

**Table 59. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 04-Apr-2012 | 8 | Updated notes related to $V_{CAP}$ in *Table 19: General operating conditions*.<br>Added values of $t_R/t_F$ for 50 pF load capacitance, and updated note in *Table 38: I/O static characteristics*.<br>Updated typical and maximum values of $R_{PU}$ in *Table 38: I/O static characteristics* and *Table 42: NRST pin characteristics*.<br>Changed SCK input to SCK output in *Section 10.3.8: SPI serial peripheral interface*<br>Modified *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* to add package top view. |
| 26-Jun-2012 | 9 | Added *Section 11.4: SDIP32 package information*. |
| 04-Feb-2015 | 10 | Updated *Section 11.5: TSSOP20 package information* and *Section 11.3: UFQFPN20 package information*. |
| 10-Mar-2015 | 11 | Updated:<br>– *Table 34: HSI oscillator characteristics*: corrected HSI oscillator accuracy (factory calibrated) for $V_{DD}$ = 5 V and $T_A$ = 25 °C.<br>– *Table 38: I/O static characteristics*: corrected the max. value for $T_R/T_F$, Fast I/Os, Load = 50 pF.<br>Added:<br>– *Figure 23: Typical pull-up current vs $V_{DD}$ @ 4 temperatures*,<br>– the rows for $T_R/T_F$, Fast I/Os, Load = 20 pF in *Table 38: I/O static characteristics*,<br>– *Figure 47: LQFP32 marking example (package top view)*,<br>– *Figure 50: UFQFPN32 marking example (package top view)*,<br>– *Figure 53: UFQFPN20 marking example (package top view)*,<br>– *Figure 55: SDIP32 marking example (package top view)*,<br>– *Figure 58: TSSOP20 marking example (package top view)*,<br>– *Figure 60: SO20 marking example (package top view)*. |
| 26-Mar-2015 | 12 | Corrected the values for “b” dimensions in *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*. |