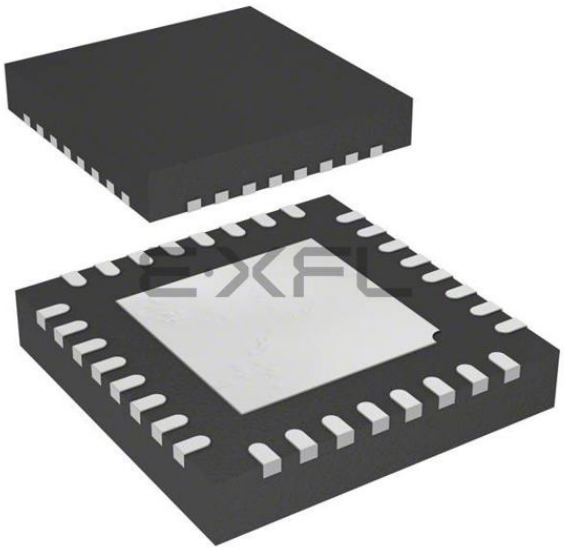

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s103k3u6

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2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8S103F2/x3 access line features

Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

Instruction set

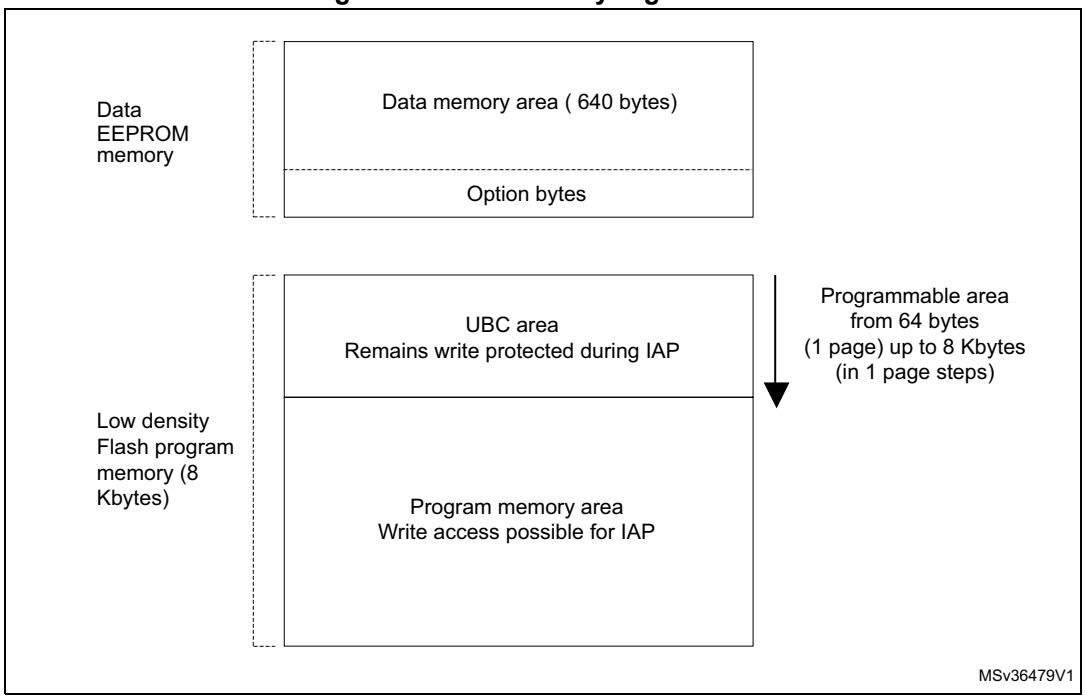
- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART1	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	Reserved	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I2C	PCKEN24	Reserved	PCKEN20	Reserved

Table 5. STM8S103K3 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
29	24	PC7/ SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	-
30	25	PD0/ TIM1_BKIN [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	Port D0	Timer 1 - break input	Configurable clock output [AFR5]
31	26	PD1/ SWIM(4)	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
32	27	PD2 [TIM2_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Timer 2 - channel 3[AFR1]
1	28	PD3/ TIM2_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Timer 2 - channel 2/ADC external trigger	-
2	29	PD4/BEEP/ TIM2_CH1	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output	-
3	30	PD5/ UART1_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	UART1 data transmit	-
4	31	PD6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	UART1 data receive	-
5	32	PD7/ TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10: Electrical characteristics*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 byte)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 00 50DF	Reserved area (13 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 byte)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		Reserved		
0x00 5302		Reserved		
0x00 5303		TIM2_IER	TIM2 Interrupt enable register	0x00
0x00 5304		TIM2_SR1	TIM2 status register 1	0x00
0x00 5305		TIM2_SR2	TIM2 status register 2	0x00
0x00 5306		TIM2_EGR	TIM2 event generation register	0x00
0x00 5307		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5308		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5309		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 530A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 530B		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530E		TIM2_PSCR	IM2 prescaler register	0x00
0x00 530F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5310		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5311		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5312		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5313		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5314		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5315		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5316		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			

7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	Reserved	-	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM2	TIM2 update/ overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/ compare	-	-	0x00 8040
15	Reserved	-	-	-	0x00 8044
16	Reserved	-	-	-	0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054
20	Reserved	-	-	-	0x00 8058

Table 10. Interrupt mapping (continued)

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
21	Reserved	-	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1.

8 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option byte can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option byte can also be modified ‘on the fly’ by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC [7:0]								0x00
0x4802		NOPT1	NUBC [7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805h	Misc. option	OPT3	Reserved			HSI TRIM	LSI _ EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI _ EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								0x00
0x480A		NOPT5	NHSECNT [7:0]								0xFF

Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected Page 0 and 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory write-protected *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM:** High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

Figure 16. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE external clock, V_{DD} = 5 V

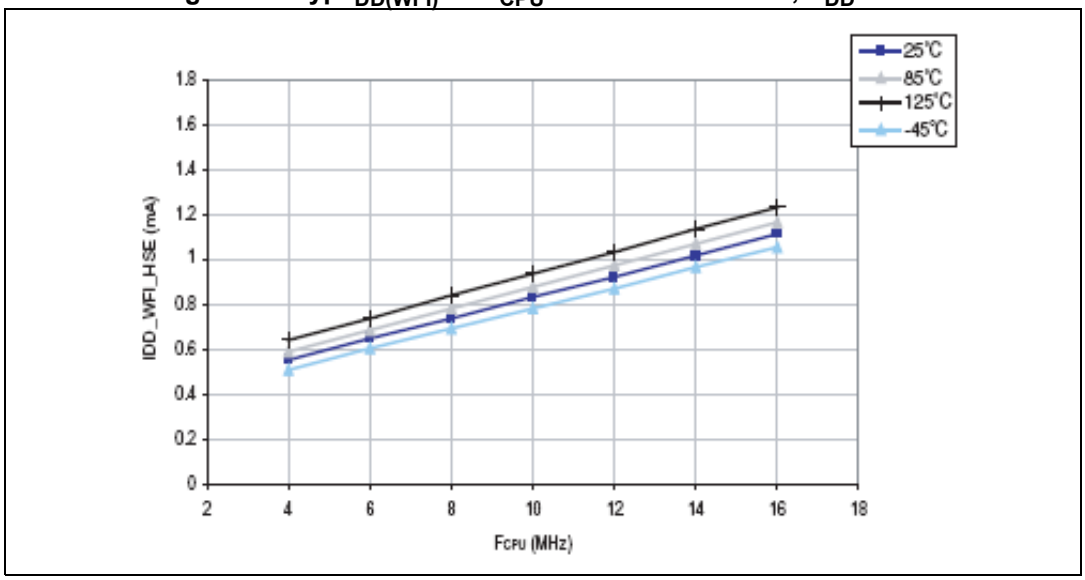
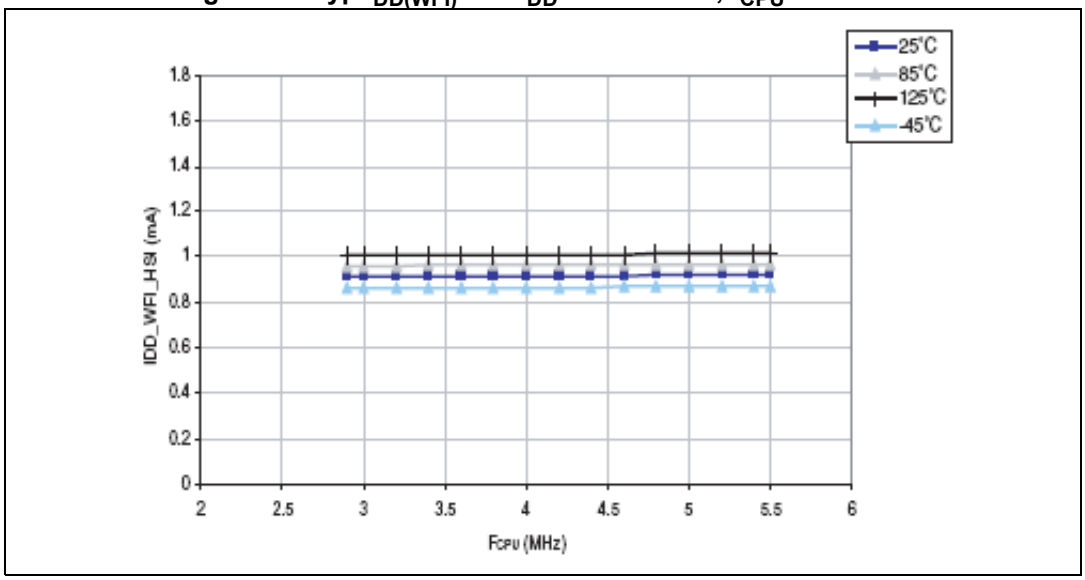


Figure 17. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator (HSI)

Table 34. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	Accuracy of HSI oscillator	User-trimmed with CLK_HSITRIMR register for given V_{DD} and T_A conditions(1)	-	-	1(2)	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C(3)	-1.0	-	1.0	
		V_{DD} = 5 V, -25°C ≤ T_A ≤ 85 °C	-2.0	-	2.0	
		2.95 V ≤ V_{DD} ≤ 5.5 V, -40°C ≤ T_A ≤ 125 °C	-3.0(3)	-	3.0(3)	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration	-	-	-	1.0(2)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250(3)	µA

1. Refer to application note.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.

Figure 20. Typical HSI frequency variation vs V_{DD} @ 4 temperatures

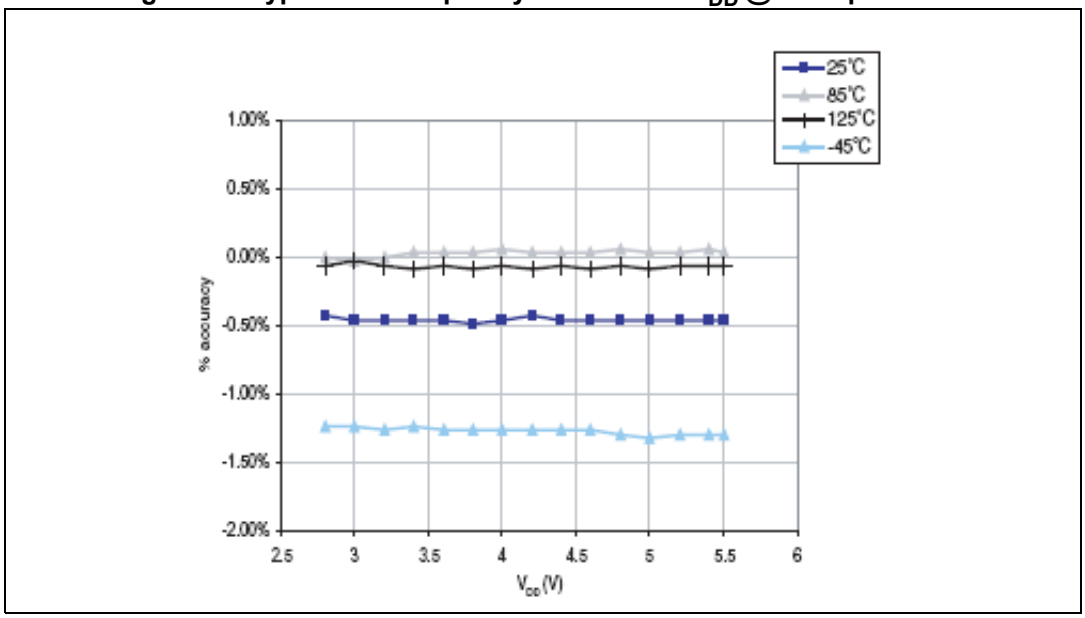


Figure 36. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

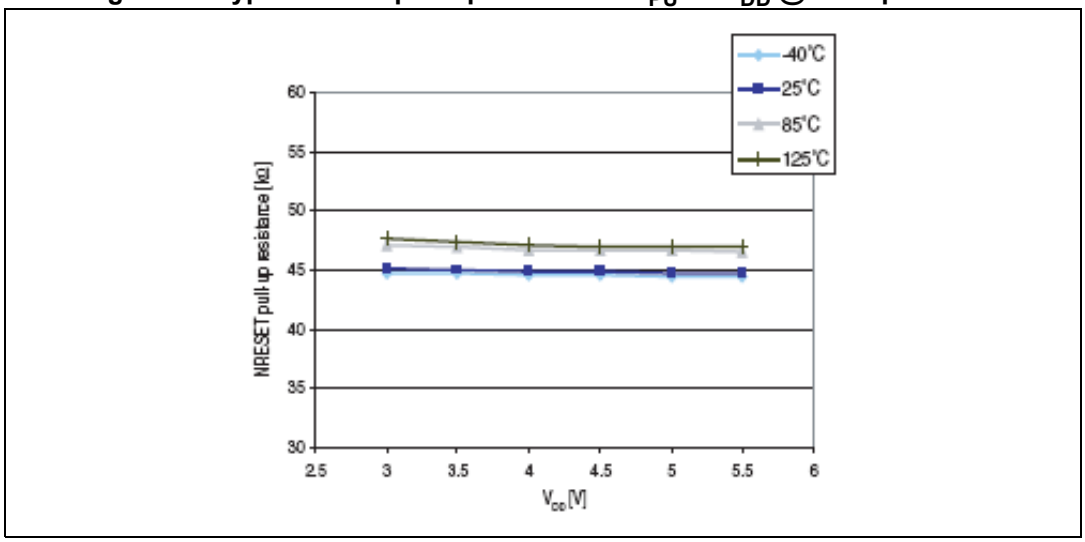
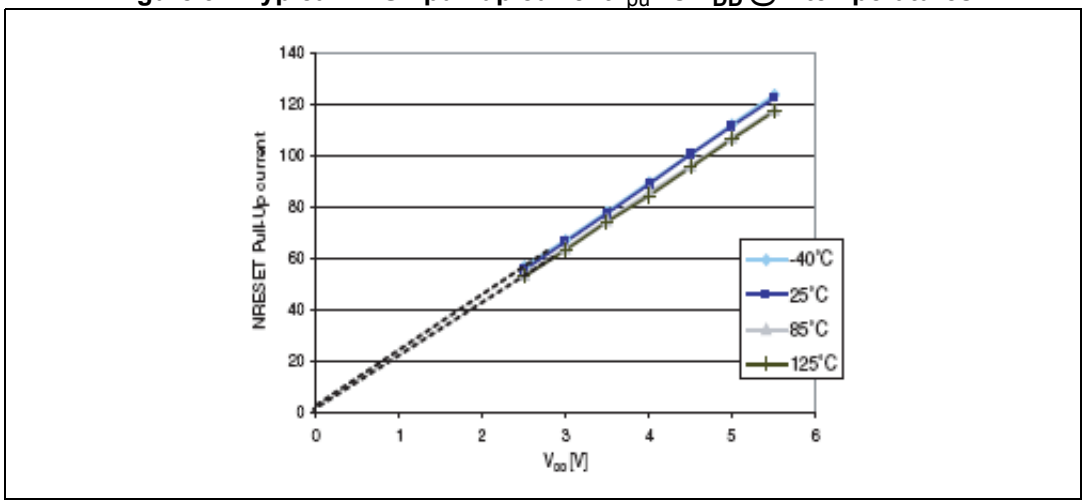


Figure 37. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures

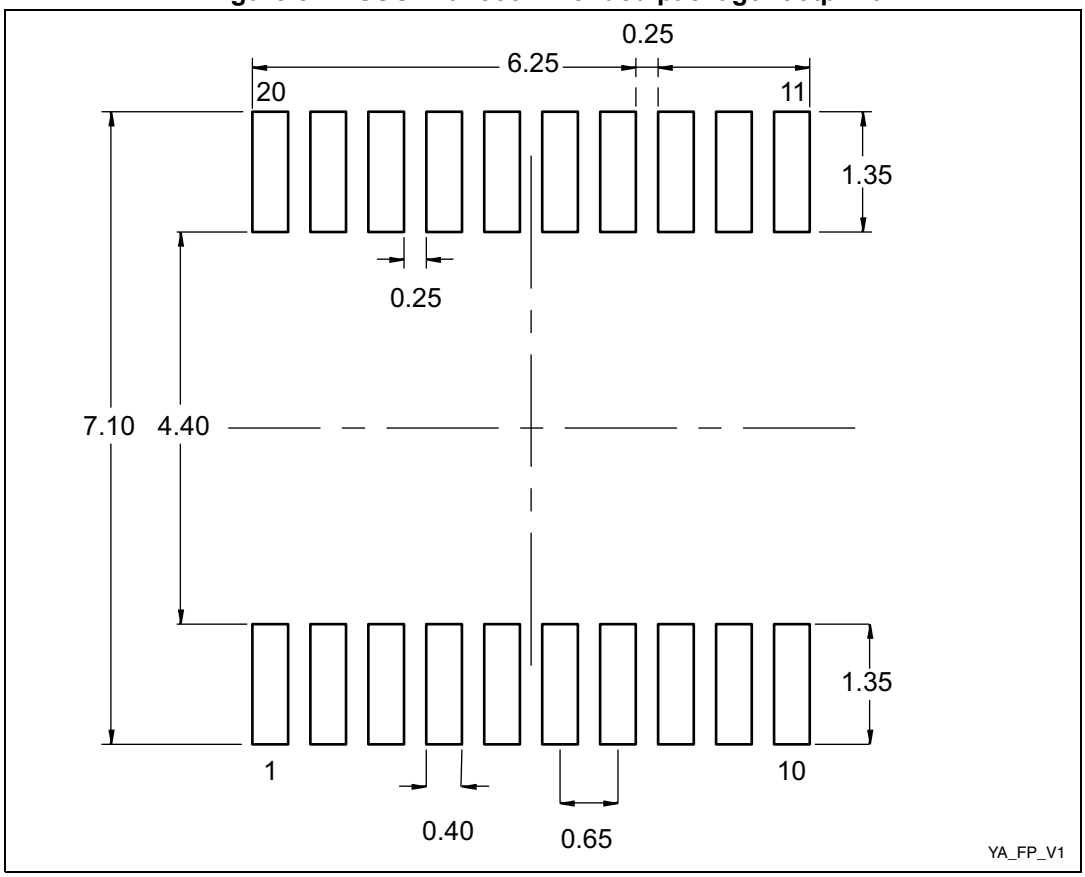


The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 42: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.

3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 57. TSSOP20 recommended package footprint



1. Dimensions are expressed in millimeters.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

13.1 STM8S103 FASTROM microcontroller option list

(last update: April 2010)

Customer	.....
Address	.....
Contact	.....
Phone number	.....
FASTROM code reference(1)	.....

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

Device type/memory size/package (check only one option)

FASTROM device	4 Kbyte	8 Kbyte
LQFP32	-	[ ] STM8S103K3
UFQFPN20	[ ] STM8S103F2	[ ] STM8S103F3
UFQFPN32	-	[ ] STM8S103K3
TSSOP20	[ ] STM8S103F2	[ ] STM8S103F3
SO20W	[ ] STM8S103F2	[ ] STM8S103F3

Conditioning (check only one option)

[ ] Tape and reel or [ ] Tray

Special marking (check only one option)

[ ] No [ ] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

UFQFPN20: 1 line of 4 characters max: “_ _ _ _”

UFQFPN32: 1 line of 7 characters max: “_ _ _ _ _ _ _”

LQFP32: 2 lines of 7 characters max: “_ _ _ _ _ _ _” and “_ _ _ _ _ _ _”

TSSOP20/SO20: 1 line of 10 characters max: “_ _ _ _ _ _ _ _ _ _”

Three characters are reserved for code identification.

Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set
UBC, bit6	[ ] 0: Reset [ ] 1: Set
UBC, bit7	[ ] 0: Reset [ ] 1: Set

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP2 alternate function remapping for STM8S103K

Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

14 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

14.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

14.1.1 STice key features

- Occurrence and time profiling and code coverage (new features),
- Advanced breakpoints with up to 4 levels of conditions,
- Data breakpoints,
- Program and data trace recording up to 128 KB records,
- Read/write on the fly of memory during emulation,
- In-circuit debugging/programming via SWIM protocol,
- 8-bit probe analyzer,
- 1 input and 2 output triggers,
- Power supply follower managing application voltages between 1.62 to 5.5 V,
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements.
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.