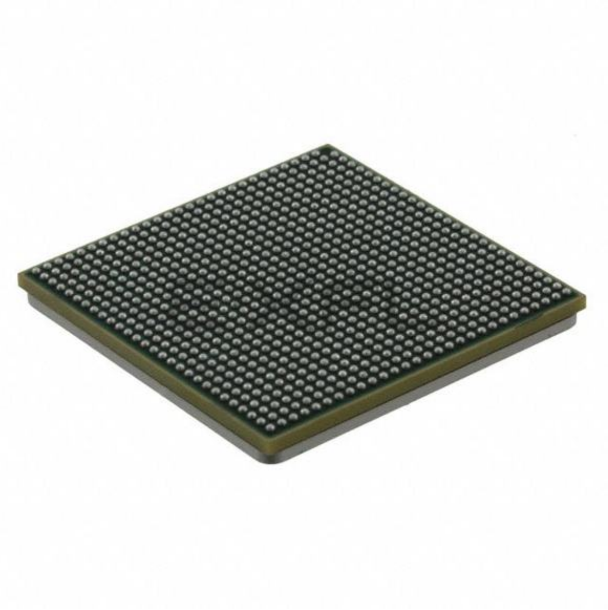


**Welcome to** E-XFL.COM

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8541epxaqf |

- Security Engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std 802.11i™, iSCSI, and IKE processing. The Security Engine contains 4 Crypto-channels, a Controller, and a set of crypto Execution Units (EUs). The Execution Units are:
  - Public Key Execution Unit (PKEU) supporting the following:
    - RSA and Diffie-Hellman
    - Programmable field size up to 2048-bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511-bits
  - Data Encryption Standard Execution Unit (DEU)
    - DES, 3DES
    - Two key (K1, K2) or Three Key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced Encryption Standard Unit (AESU)
    - Implements the Rinjdael symmetric key cipher
    - Key lengths of 128, 192, and 256 bits.Two key
    - ECB, CBC, CCM, and Counter modes
  - ARC Four execution unit (AFEU)
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message Digest Execution Unit (MDEU)
    - SHA with 160-bit or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random Number Generator (RNG)
  - 4 Crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 Bytes for each execution unit, with flow control for large data sizes
- High-performance RISC CPM
  - Two full-duplex fast communications controllers (FCCs) that support the following protocol:
    - IEEE Std 802.3™/Fast Ethernet (10/100)
  - Serial peripheral interface (SPI) support for master or slave
  - $I^2C$ bus controller
  - General-purpose parallel ports—16 parallel I/O lines with interrupt capability
- 256 Kbytes of on-chip memory
  - Can act as a 256-Kbyte level-2 cache
  - Can act as a 256-Kbyte or two 128-Kbyte memory-mapped SRAM arrays
  - Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
  - Full ECC support on 64-bit boundary in both cache and SRAM modes

- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
  - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses

- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI
    - Four inbound windows
    - Four outbound windows plus default translation for PCI
- DDR memory controller
  - Programmable timing supporting first generation DDR SDRAM
  - 64-bit data interface, up to MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Sleep mode support for self refresh DDR SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller

- Four global high resolution timers/counters that can generate interrupts
- Supports additional internal interrupt sources
- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source

- Two I$^2$C controllers (one is contained within the CPM, the other is a stand-alone controller which is not part of the CPM)
  - Two-wire interface
  - Multiple master support
  - Master or slave I$^2$C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the stand-alone I$^2$C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I$^2$C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (RXD, TXD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Two Three-speed (10/100/1000)Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z AC compliant controllers
  - Support for Ethernet physical interfaces:
    - 10/100/1000 Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII

# 3 Power Characteristics

The estimated typical power dissipation for this family of PowerQUICC III devices is shown in Table 4.

**Table 4. Power Dissipation(1) (2)**

| CCB Frequency (MHz) | Core Frequency (MHz) | $V_{DD}$ | Typical Power(3)(4) (W) | Maximum Power(5) (W) |
|---|---|---|---|---|
| 200 | 400 | 1.2 | 4.4 | 6.1 |
| | 500 | 1.2 | 4.7 | 6.5 |
| | 600 | 1.2 | 5.0 | 6.8 |
| 267 | 533 | 1.2 | 4.9 | 6.7 |
| | 667 | 1.2 | 5.4 | 7.2 |
| | 800 | 1.2 | 5.8 | 8.6 |
| 333 | 667 | 1.2 | 5.5 | 7.4 |
| | 833 | 1.2 | 6.0 | 8.8 |
| | 1000(6) | 1.3 | 9.0 | 12.2 |

**Notes:**

1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 degrees junction temperature is not exceeded on this device.
3. Typical power is based on a nominal voltage of $V_{DD}$ = 1.2V, a nominal process, a junction temperature of $T_j$ = 105° C, and a Dhrystone 2.1 benchmark application.
4. Thermal solutions likely need to design to a value higher than Typical Power based on the end application, $T_A$ target, and I/O power
5. Maximum power is based on a nominal voltage of $V_{DD}$ = 1.2V, worst case process, a junction temperature of $T_j$ = 105° C, and an artificial smoke test.
6. The nominal recommended $V_{DD}$ = 1.3V for this speed grade.

**Notes:**

1.
2.
3.
4.
5.
6.

# 4 Clock Timing

## 4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8541E.

**Table 6. SYSCLK AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | — | — | 166 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 6.0 | — | — | ns | — |
| SYSCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| SYSCLK duty cycle | $t_{KHK}/t_{SYSCLK}$ | 40 | — | 60 | % | 3 |
| SYSCLK jitter | — | — | — | +/- 150 | ps | 4, 5 |

**Notes:**

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are ±1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

## 4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8541E.

**Table 7. EC_GTX_CLK125 AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $f_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC_GTX_CLK125 rise time | $t_{G125R}$ | — | — | 1.0 | ns | 1 |
| EC_GTX_CLK125 fall time | $t_{G125F}$ | — | — | 1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle | $t_{G125H}/t_{G125}$ |  | — |  | % | 1, 2 |
| GMII, TBI |  | 45 |  | 55 |  |  |
| RGMII, RTBI |  | 47 |  | 53 |  |  |

**Notes:**

1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

Figure 6 provides the AC test load for the DDR bus.

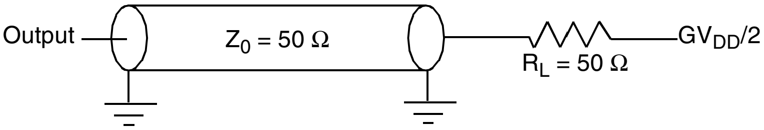


**Figure 6. DDR AC Test Load**

**Table 15. DDR SDRAM Measurement Conditions**

| Symbol | DDR | Unit | Notes |
|---|---|---|---|
| $V_{TH}$ | $MV_{REF}$ ± 0.31 V | V | 1 |
| $V_{OUT}$ | $0.5 \times GV_{DD}$ | V | 2 |

**Notes:**
1. Data input threshold measurement point.
2. Data output measurement point.

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8541E.

## 7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8541E.

**Table 16. DUART DC Electrical Characteristics**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or<br>$V_{OUT} \leq V_{OL}$ (max) | 2 | $OV_{DD} + 0.3$ | V |
| Low-level input voltage | $V_{IL}$ | | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $V_{IN}$ [1] = 0 V or $V_{IN} = V_{DD}$ | — | ±5 | μA |
| High-level output voltage | $V_{OH}$ | $OV_{DD}$ = min,<br>$I_{OH}$ = –100 μA | $OV_{DD} - 0.2$ | — | V |
| Low-level output voltage | $V_{OL}$ | $OV_{DD}$ = min, $I_{OL}$ = 100 μA | — | 0.2 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

**Table 21. GMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 40 | — | 60 | % |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0.5 | — | — | ns |
| RX_CLK clock rise and fall time | $t_{GRXR}$, $t_{GRXF}$ [2,3] | — | — | 1.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

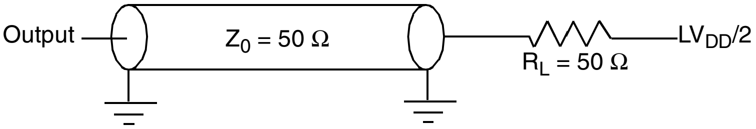


**Figure 8. TSEC AC Test Load**

Figure 9 shows the GMII receive AC timing diagram.

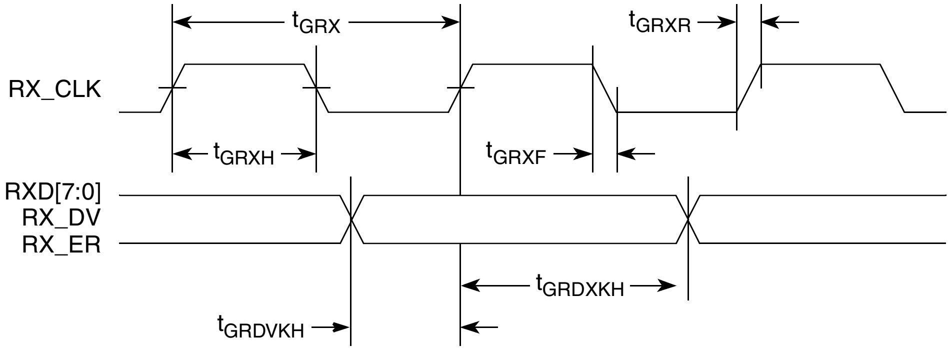


**Figure 9. GMII Receive AC Timing Diagram**

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.

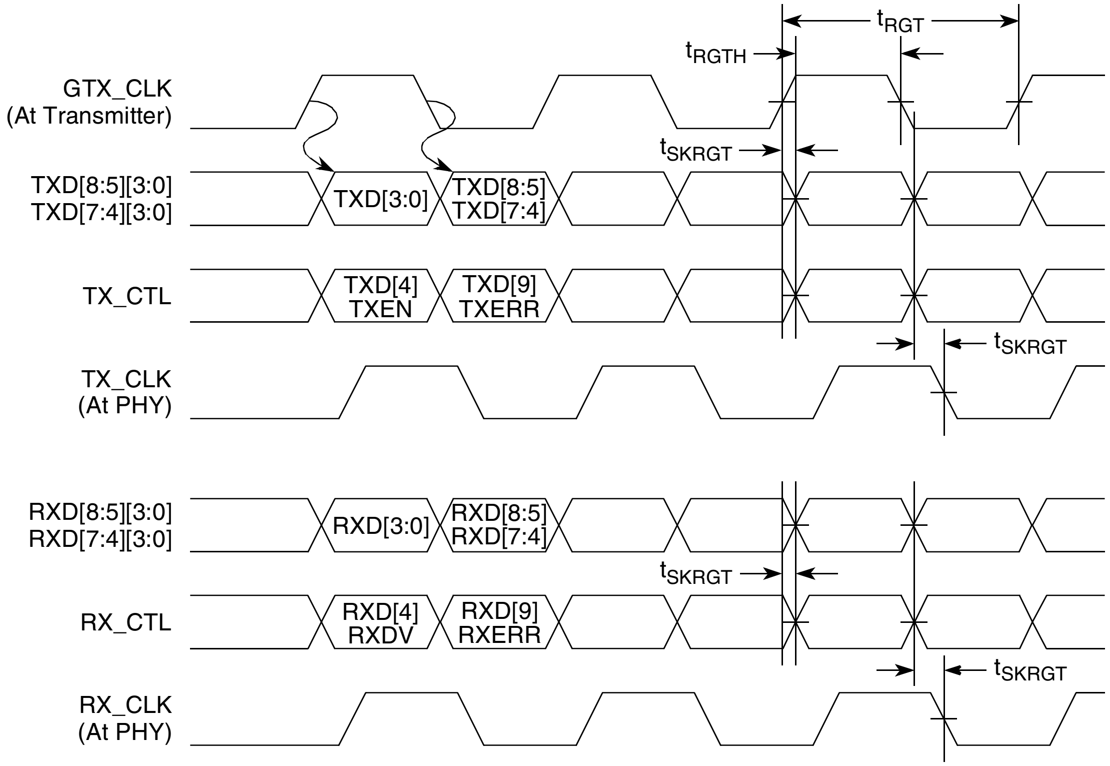


**Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

### 8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

**Table 27. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | — | | 3.13 | 3.47 | V |
| Output high voltage | $V_{OH}$ | $I_{OH} = -1.0$ mA | $LV_{DD}$ = Min | 2.10 | $LV_{DD} + 0.3$ | V |
| Output low voltage | $V_{OL}$ | $I_{OL} = 1.0$ mA | $LV_{DD}$ = Min | GND | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | | 1.70 | — | V |
| Input low voltage | $V_{IL}$ | — | | — | 0.90 | V |

# 10 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8541E.

## 10.1 CPM DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the CPM.

**Table 32. CPM DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | | 2.0 | 3.465 | V | 1 |
| Input low voltage | $V_{IL}$ | | GND | 0.8 | V | 1, 2 |
| Output high voltage | $V_{OH}$ | $I_{OH} = -8.0$ mA | 2.4 | — | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL} = 8.0$ mA | — | 0.5 | V | 1 |
| Output high voltage | $V_{OH}$ | $I_{OH} = -2.0$ mA | 2.4 | — | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL} = 3.2$ mA | — | 0.4 | V | 1 |

## 10.2 CPM AC Timing Specifications

Table 33 and Table 34 provide the CPM input and output AC timing specifications, respectively.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 33. CPM Input AC Timing Specifications [1]**

| Characteristic | Symbol [2] | Min[3] | Unit |
|---|---|---|---|
| FCC inputs—internal clock (NMSI) input setup time | $t_{FIIVKH}$ | 6 | ns |
| FCC inputs—internal clock (NMSI) hold time | $t_{FIIXKH}$ | 0 | ns |
| FCC inputs—external clock (NMSI) input setup time | $t_{FEIVKH}$ | 2.5 | ns |
| FCC inputs—external clock (NMSI) hold time | $t_{FEIXKH}b$ | 2 | ns |
| SPI inputs—internal clock (NMSI) input setup time | $t_{NIIVKH}$ | 6 | ns |
| SPI inputs—internal clock (NMSI) input hold time | $t_{NIIXKH}$ | 0 | ns |
| SPI inputs—external clock (NMSI) input setup time | $t_{NEIVKH}$ | 4 | ns |
| SPI inputs—external clock (NMSI) input hold time | $t_{NEIXKH}$ | 2 | ns |
| PIO inputs—input setup time | $t_{PIIVKH}$ | 8 | ns |

Figure 27 shows the SPI external clock.

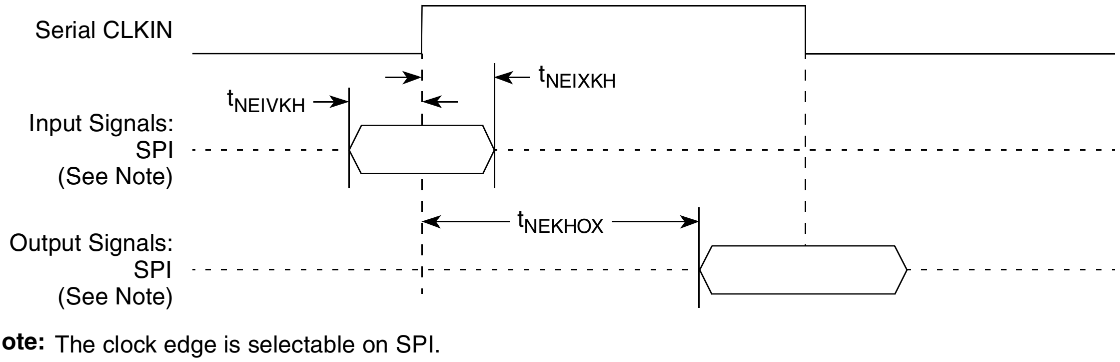


**Figure 27. SPI AC Timing External Clock Diagram**

Figure 28 shows the SPI internal clock.

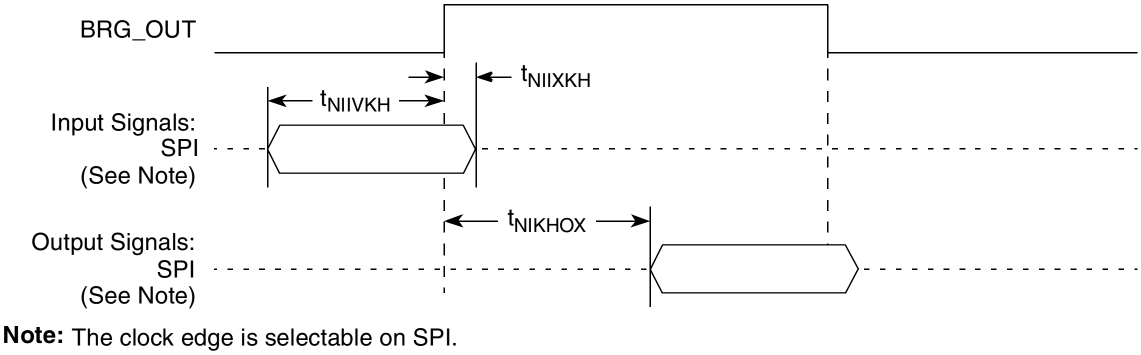


**Figure 28. SPI AC Timing Internal Clock Diagram**

### NOTE

[1] SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

[2] SPI AC timings refer always to SPICLK.

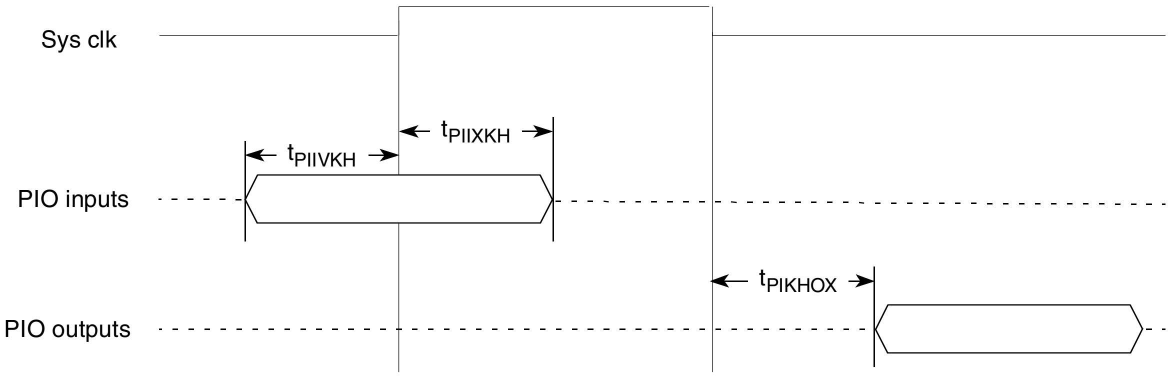


**Figure 29. PIO Signal Diagram**

### Table 43. MPC8541E Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{PCI2\_GNT}}$[1:4] | AD18, AE18, AE19, AD19 | O | $OV_{DD}$ | 5, 9 |
| PCI2_IDSEL | AC22 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI2\_IRDY}}$ | AD20 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI2\_PERR}}$ | AC20 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI2\_REQ}}$[0] | AD21 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI2\_REQ}}$[1:4] | AE21, AD22, AE22, AC23 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI2\_SERR}}$ | AE20 | I/O | $OV_{DD}$ | 2,4 |
| $\overline{\text{PCI2\_STOP}}$ | AC21 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI2\_TRDY}}$ | AC19 | I/O | $OV_{DD}$ | 2 |
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | N20, M20, L19, E19, C21, A21, G19, A19 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | L24, H28, F24, L21, E18, E16, G14, B13, M19 | O | $GV_{DD}$ | — |
| MDQS[0:8] | L26, J25, D25, A22, H18, F16, F14, C13, C20 | I/O | $GV_{DD}$ | — |
| MBA[0:1] | B18, B19 | O | $GV_{DD}$ | — |
| MA[0:14] | N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13 | O | $GV_{DD}$ | — |
| $\overline{\text{MWE}}$ | D17 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | F17 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | J16 | O | $GV_{DD}$ | — |
| $\overline{\text{MCS}}$[0:3] | H16, G16, J15, H15 | O | $GV_{DD}$ | — |
| MCKE[0:1] | E26, E28 | O | $GV_{DD}$ | 11 |
| MCK[0:5] | J20, H25, A15, D20, F28, K14 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | F20, G27, B15, E20, F27, L14 | O | $GV_{DD}$ | — |
| MSYNC_IN | M28 | I | $GV_{DD}$ | 22 |
| MSYNC_OUT | N28 | O | $GV_{DD}$ | 22 |
| **Local Bus Controller Interface** | | | | |
| LA[27] | U18 | O | $OV_{DD}$ | 5, 9 |

### Table 43. MPC8541E Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| GND | A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7 | — | — | — |
| $GV_{DD}$ | A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21 | Power for DDR DRAM I/O Voltage (2.5 V) | $GV_{DD}$ | — |
| $LV_{DD}$ | A4, C5, E7, H10 | Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V) | $LV_{DD}$ | — |
| $MV_{REF}$ | N27 | Reference Voltage Signal; DDR | $MV_{REF}$ | — |
| No Connects | AA24, AA25, AA3, AA4, AA7 AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3 | — | — | 16 |
| $OV_{DD}$ | D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4 | PCI, 10/100 Ethernet, and other Standard (3.3 V) | $OV_{DD}$ | — |
| RESERVED | C1, T11, U11, AF1 | — | — | 15 |
| SENSEVDD | L12 | Power for Core (1.2 V) | $V_{DD}$ | 13 |
| SENSEVSS | K12 | — | — | 13 |
| $V_{DD}$ | M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14 | Power for Core (1.2 V) | $V_{DD}$ | — |
| **CPM** | | | | |
| PA[8:31] | J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2 | I/0 | $OV_{DD}$ | — |

## 15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

**Table 47. e500 Core to CCB Ratio**

| Binary Value of LALE, LGPL2 Signals | Ratio Description |
|---|---|
| 00 | 2:1 e500 core:CCB |
| 01 | 5:2 e500 core:CCB |
| 10 | 3:1 e500 core:CCB |
| 11 | 7:2 e500 core:CCB |

## 15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

**Table 48. Frequency Options with Respect to Memory Bus Speeds**

| CCB to SYSCLK Ratio | SYSCLK (MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 17 | 25 | 33 | 42 | 67 | 83 | 100 | 111 | 133 |
| | Platform/CCB Frequency (MHz) | | | | | | | | |
| 2 | | | | | | | 200 | 222 | 267 |
| 3 | | | | | 200 | 250 | 300 | 333 | |
| 4 | | | | | 267 | 333 | | | |
| 5 | | | | 208 | 333 | | | | |
| 6 | | | 200 | 250 | | | | | |
| 8 | | 200 | 267 | 333 | | | | | |
| 9 | | 225 | 300 | | | | | | |
| 10 | | 250 | 333 | | | | | | |
| 12 | 200 | 300 | | | | | | | |
| 16 | 267 | | | | | | | | |

the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

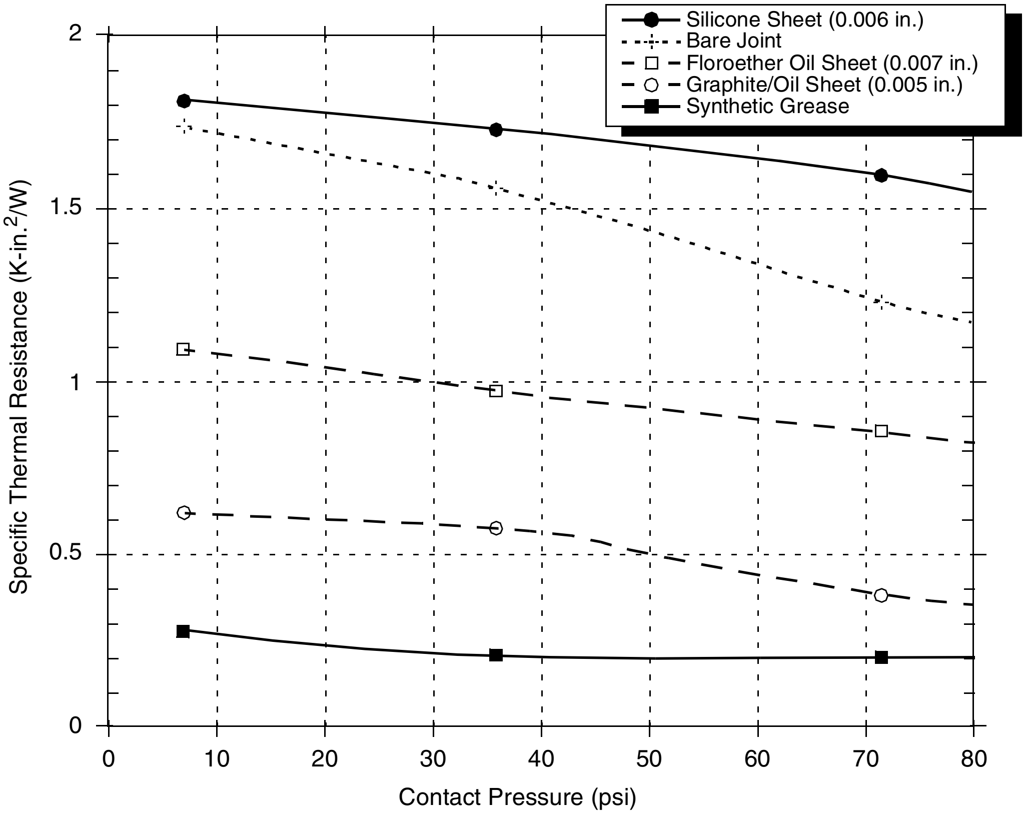
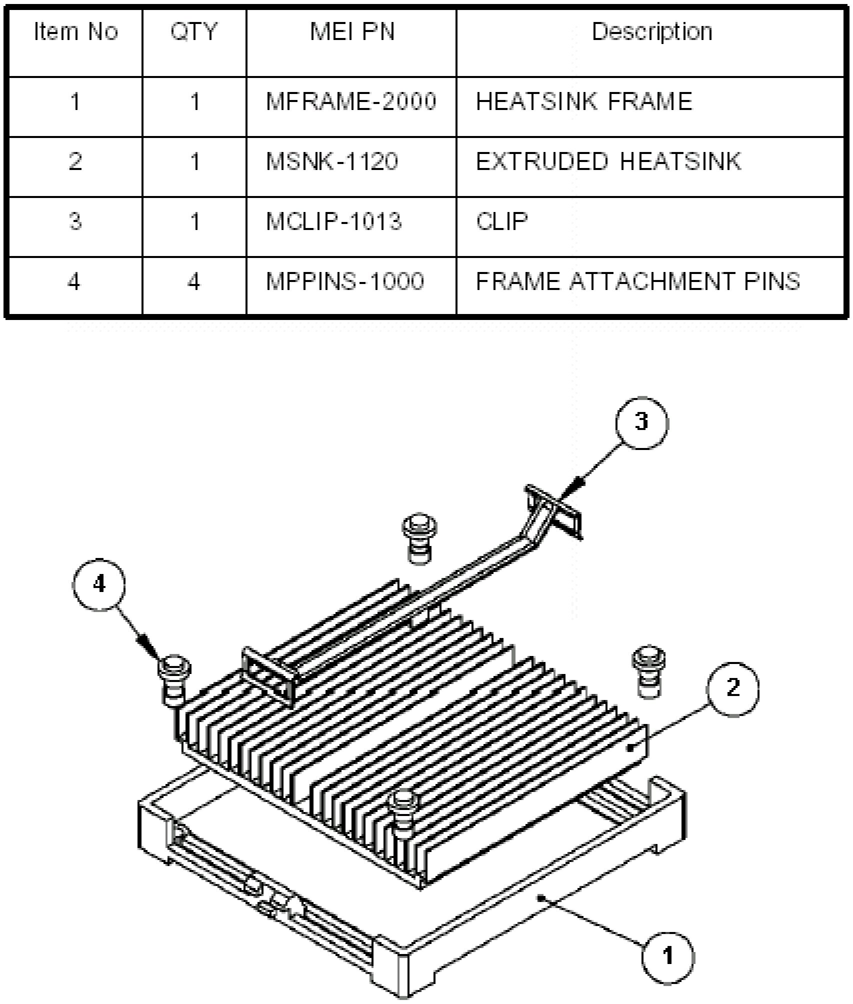


**Figure 45. Thermal Performance of Select Thermal Interface Materials**

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01888-4014<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Dow-Corning Electronic Materials<br>2200 W. Salzburg Rd.<br>Midland, MI 48686-0997<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company<br>18930 West 78th St. | 800-347-4572 |



| Item No | QTY | MEI PN | Description |
|---|---|---|---|
| 1 | 1 | MFRAME-2000 | HEATSINK FRAME |
| 2 | 1 | MSNK-1120 | EXTRUDED HEATSINK |
| 3 | 1 | MCLIP-1013 | CLIP |
| 4 | 4 | MPPINS-1000 | FRAME ATTACHMENT PINS |

Illustrative source provided by
Millennium Electronics (MEI)

**Figure 48. Exploded Views (2) of a Heat Sink Attachment using a Plastic Force**

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

# 17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8541E.

## 17.1 System Clocking

The MPC8541E includes five PLLs.

1. The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”
3. The CPM PLL ($AV_{DD}3$) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL ($AV_{DD}4$) generates the clocking for the first PCI bus.
5. The PCI2 PLL ($AV_{DD}5$) generates the clock for the second PCI bus.

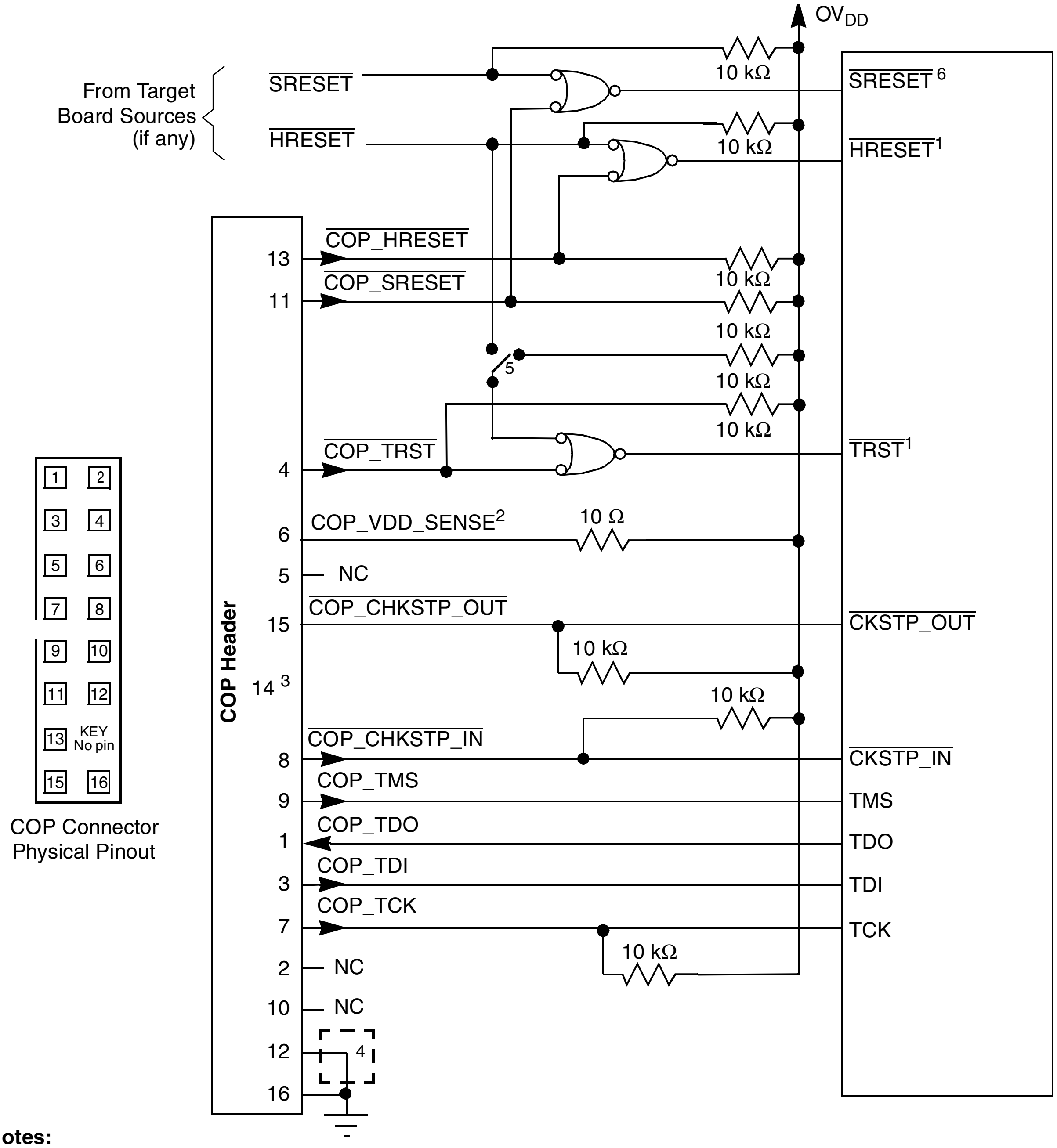
## 17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, and $AV_{DD}5$ respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 49, one to each of the five $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.



**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

**Figure 52. JTAG Interface Connection**

# 18 Document Revision History

Table 51 provides a revision history for this hardware specification.

**Table 51. Document Revision History**

| Rev. No. | Date | Substantive Change(s) |
|---|---|---|
| 4.2 | 1/2008 | Added "Note: Rise/Fall Time on CPM Input Pins" and following note text to Section 10.2, "CPM AC Timing Specifications." |
| 4.1 | 07/2007 | Inserted Figure 3, ""Maximum AC Waveforms on PCI interface for 3.3-V Signaling." |
| 4 | 12/2006 | Updated Section 2.1.2, "Power Sequencing."<br>Updated back page information. |
| 3.2 | 11/2006 | Updated Section 2.1.2, "Power Sequencing."<br>Replaced Section 17.8, "JTAG Configuration Signals." |
| 3.1 | 10/2005 | Table 4: Added footnote 2 about junction temperature.<br>Table 4: Added max. power values for 1000 MHz core frequency.<br>Removed Figure 3, "Maximum AC Waveforms on PCI Interface for 3.3-V Signaling."<br>Table 30: Modified note to $t_{LBKSKEW}$ from 8 to 9<br>Table 30: Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values.<br>Table 30: Added note 3 to $t_{LBKHOV1}$.<br>Table 30 and Table 31: Modified note 3.<br>Table 31: Added note 3 to $t_{LBKLOV1}$.<br>Table 31: Modified values for $t_{LBKHKT}$, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$.<br>Figure 21: Changed Input Signals: LAD[0:31]/LDP[0:3].<br>Table 43: Modified note for signal CLK_OUT.<br>Table 43: PCI1_CLK and PCI2_CLK changed from I/O to I.<br>Table 52: Added column for Encryption Acceleration. |
| 3 | 8/29/2005 | Table 4: Modified max. power values.<br>Table 43: Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL. |
| 2 | 8/2005 | Previous revision's history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 31 is now listed as Table 31.<br>Table 7: Added note 2.<br>Table 14: Modified min and max values for $t_{DDKHMP}$ |
| 1 | 6/2005 | Table 27: Changed $LV_{dd}$ to $OV_{dd}$ for the supply voltage Ethernet management interface.<br>Table 4: Modified footnote 4 and changed typical power for the 1000MHz core frequency.<br>Table 31: Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state. |
| 0 | 6/2005 | Initial Release. |

THIS PAGE INTENTIONALLY LEFT BLANK

### *How to Reach Us:*

**Home Page:**
www.freescale.com

**Web Support:**
http://www.freescale.com/support

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

**For Literature Requests Only:**
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license. IEEE 802.3 and 1149.1 are registered trademarks of the Institute of Electrical and Electronics Engineers, Inc. (IEEE). This product is not endorsed or approved by the IEEE. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2008. All rights reserved.

Document Number: MPC8541EEC
Rev. 4.2
1/2008

BUILT ON
Power™

freescale™
semiconductor