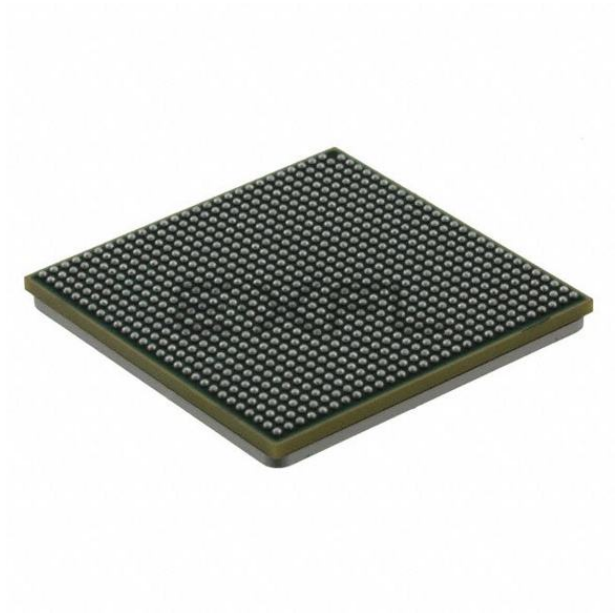

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 833MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8541pxapf |

  - Selectable hardware-enforced coherency
  - Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power save modes: doze, nap, and sleep
  - Employs dynamic power management
  - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783 FC-PBGA package

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8541E. The MPC8541E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings [1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.32<br>0.3 to 1.43 (for 1 GHz only) | V | |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 1.32<br>0.3 to 1.43 (for 1 GHz only) | V | |
| DDR DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 3.63 | V | |
| Three-speed Ethernet I/O, MII management voltage | | $LV_{DD}$ | –0.3 to 3.63<br>–0.3 to 2.75 | V | |
| CPM, PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | 3 |
| Input voltage | DDR DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | Three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 4, 5 |
| | CPM, Local bus, DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3)1 | V | 5 |
| | PCI | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 6 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | |

**Notes:**
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $LV_{IN}$ must not exceed $LV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. $OV_{IN}$ on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

### 2.1.2 Power Sequencing

The MPC8541Erequires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. $V_{DD}$, $AV_{DDn}$
2. $GV_{DD}$, $LV_{DD}$, $OV_{DD}$ (I/O supplies)

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8541E.

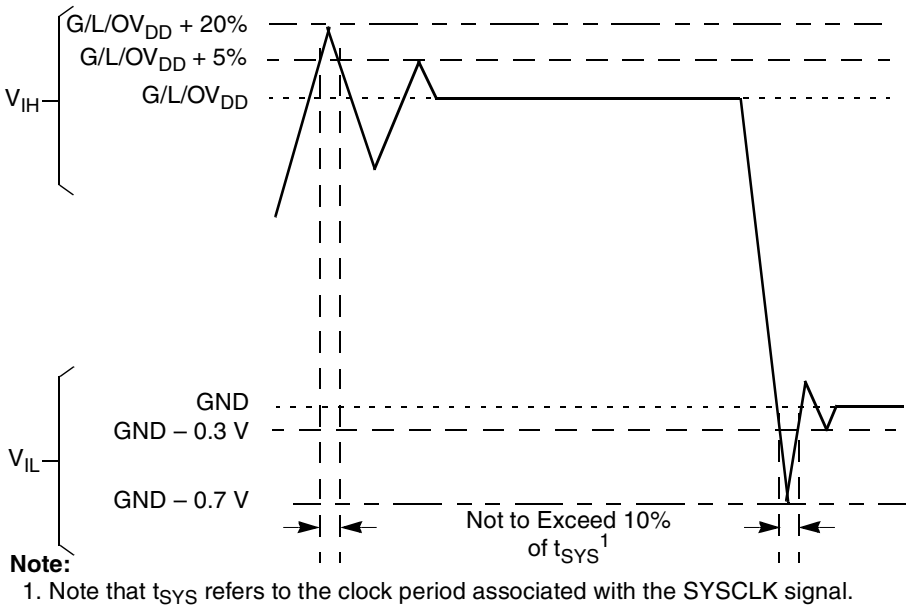



**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$**

The MPC8541E core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. $OV_{DD}$ and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied $MV_{REF}$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8541E for the 3.3-V signals, respectively.

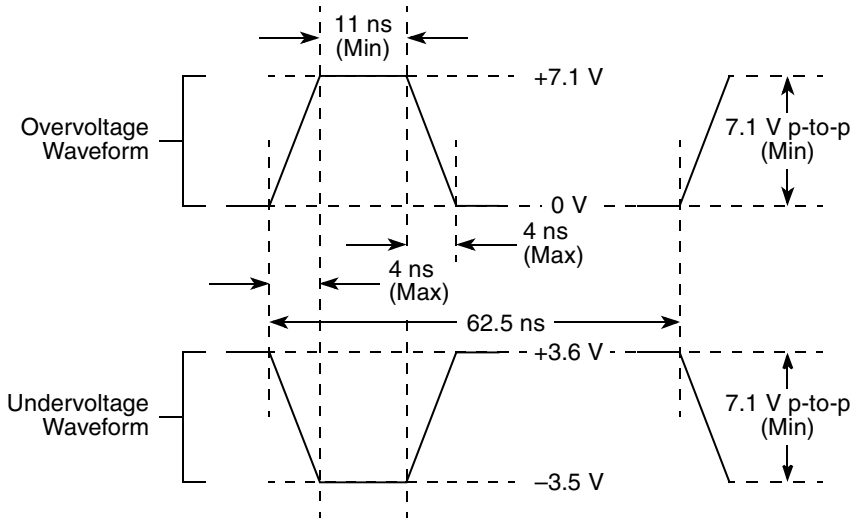



**Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling**

## 2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| Local bus interface utilities signals | 25 | $OV_{DD}$ = 3.3 V | 1 |
| | 42 (default) | | |
| PCI signals | 25 | | 2 |
| | 42 (default) | | |
| DDR signal | 20 | $GV_{DD}$ = 2.5 V | |
| TSEC/10/100 signals | 42 | $LV_{DD}$ = 2.5/3.3 V | |
| DUART, system control, I2C, JTAG | 42 | $OV_{DD}$ = 3.3 V | |

**Notes:**
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

### 6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 13. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.31 | $GV_{DD}$ + 0.3 | V | — |
| MDQS—MDQ/MECC input skew per byte<br>For DDR = 333 MHz<br>For DDR ≤ 266 MHz | $t_{DISKEW}$ | — | <br>750<br>1125 | ps | 1 |

**Note:**

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

### 6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

**Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode**

At recommended operating conditions with $GV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing) | $t_{MCK}$ | 6 | 10 | ns | 2 |
| Skew between any MCK to ADDR/CMD<br>333 MHz<br>266 MHz<br>200 MHz | $t_{AOSKEW}$ | <br>–1000<br>–1100<br>–1200 | <br>200<br>300<br>400 | ps | 3 |
| ADDR/CMD output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHAS}$ | <br>2.8<br>3.45<br>4.6 | — | ns | 4 |
| ADDR/CMD output hold with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHAX}$ | <br>2.0<br>2.65<br>3.8 | — | ns | 4 |
| $\overline{\text{MCS}}$(n) output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHCS}$ | <br>2.8<br>3.45<br>4.6 | — | ns | 4 |

## 8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

### 8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2 GMII Transmit AC Timing Specifications

Table 20 provides the GMII transmit AC timing specifications.

**Table 20. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTX}$ | — | 8.0 | — | ns |
| GTX_CLK duty cycle | $t_{GTXH}/t_{GTX}$ | 40 | — | 60 | % |
| GMII data TXD[7:0], TX_ER, TX_EN setup time | $t_{GTKHDV}$ | 2.5 | — | — | ns |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$ | 0.5 | — | 5.0 | ns |
| GTX_CLK data clock rise and fall times | $t_{GTXR}$[3], $t_{GTXR}$[2,4] | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

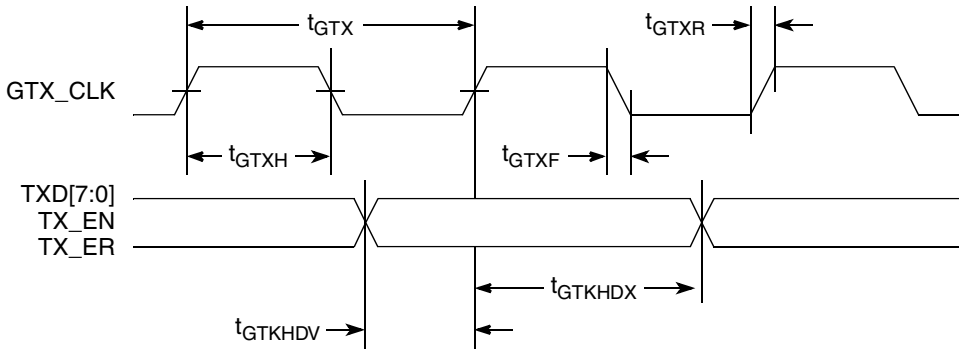



**Figure 7. GMII Transmit AC Timing Diagram**

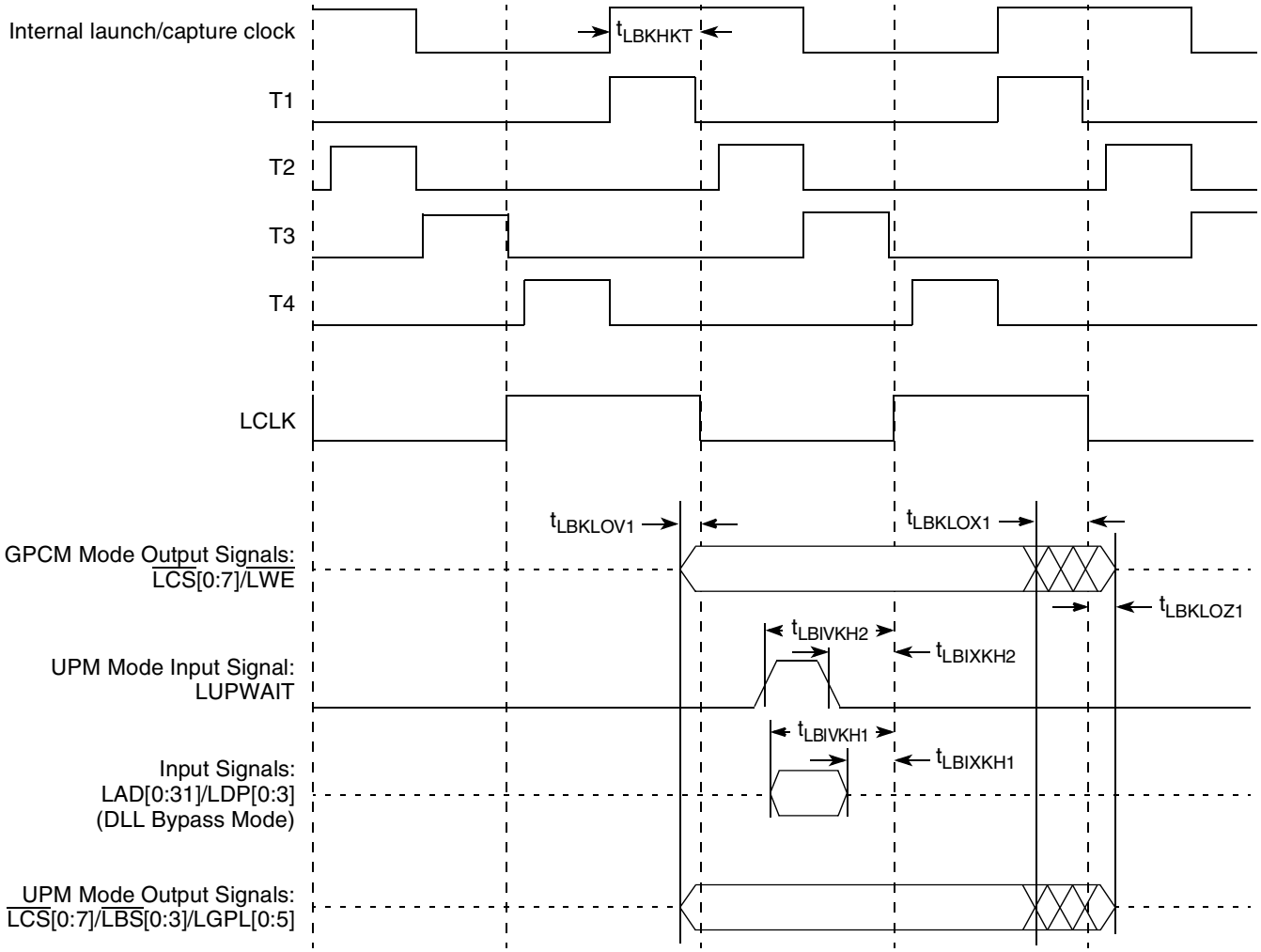



**Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)**

# 11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8541E.

Table 38 provides the JTAG AC timing specifications as defined in Figure 32 through Figure 35.

**Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | — |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>—<br>— | <br>—<br>— | ns | 5 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 31). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

Figure 35 provides the test access port timing diagram.

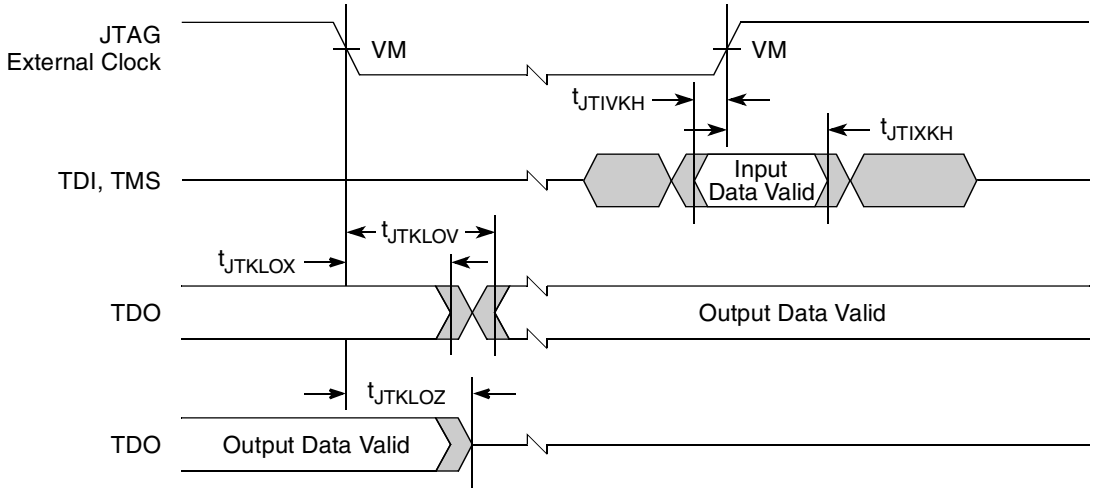



**Figure 35. Test Access Port Timing Diagram**

# 12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8541E.

## 12.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8541E.

**Table 39. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD}$+ 0.3 | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | $0.2 \times OV_{DD}$ | V | 1 |
| Output fall time from $V_{IH}$(min) to $V_{IL}$(max) with a bus capacitance from 10 to 400 pF | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –10 | 10 | μA | 4 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. $C_B$ = capacitance of one bus line in pF.
3. Refer to the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8541E, 783 FC-PBGA package.

**Table 43. MPC8541E Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI1 and PCI2 (one 64-bit or two 32-bit)** | | | | |
| PCI1_AD[63:32], PCI2_AD[31:0] | AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18 | I/O | $OV_{DD}$ | 17 |
| PCI1_AD[31:0] | AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13 | I/O | $OV_{DD}$ | 17 |
| $\overline{\text{PCI_C_BE64}}$[7:4] $\overline{\text{PCI2_C_BE}}$[3:0] | AG13, AH13, V14, W14 | I/O | $OV_{DD}$ | 17 |
| $\overline{\text{PCI_C_BE64}}$[3:0] $\overline{\text{PCI1_C_BE}}$[3:0] | AH8, AB10, AD11, AC12 | I/O | $OV_{DD}$ | 17 |
| PCI1_PAR | AA11 | I/O | $OV_{DD}$ | — |
| PCI1_PAR64/PCI2_PAR | Y14 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1_FRAME}}$ | AC10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1_TRDY}}$ | AG10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1_IRDY}}$ | AD10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1_STOP}}$ | V11 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1_DEVSEL}}$ | AH10 | I/O | $OV_{DD}$ | 2 |
| PCI1_IDSEL | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI1_REQ64}}$/$\overline{\text{PCI2_FRAME}}$ | AE13 | I/O | $OV_{DD}$ | 5, 10 |
| $\overline{\text{PCI1_ACK64}}$/$\overline{\text{PCI2_DEVSEL}}$ | AD13 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1_PERR}}$ | W11 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1_SERR}}$ | Y11 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{PCI1_REQ}}$[0] | AF5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1_REQ}}$[1:4] | AF3, AE4, AG4, AE5 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI1_GNT}}$[0] | AE6 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1_GNT}}$[1:4] | AG5, AH5, AF6, AG6 | O | $OV_{DD}$ | 5, 9 |
| PCI1_CLK | AH25 | I | $OV_{DD}$ | — |
| PCI2_CLK | AH27 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI2_GNT}}$[0] | AC18 | I/O | $OV_{DD}$ | — |

**Table 43. MPC8541E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| PCI2_GNT[1:4] | AD18, AE18, AE19, AD19 | O | $OV_{DD}$ | 5, 9 |
| PCI2_IDSEL | AC22 | I | $OV_{DD}$ | — |
| PCI2_IRDY | AD20 | I/O | $OV_{DD}$ | 2 |
| PCI2_PERR | AC20 | I/O | $OV_{DD}$ | 2 |
| PCI2_REQ[0] | AD21 | I/O | $OV_{DD}$ | — |
| PCI2_REQ[1:4] | AE21, AD22, AE22, AC23 | I | $OV_{DD}$ | — |
| PCI2_SERR | AE20 | I/O | $OV_{DD}$ | 2,4 |
| PCI2_STOP | AC21 | I/O | $OV_{DD}$ | 2 |
| PCI2_TRDY | AC19 | I/O | $OV_{DD}$ | 2 |
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | N20, M20, L19, E19, C21, A21, G19, A19 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | L24, H28, F24, L21, E18, E16, G14, B13, M19 | O | $GV_{DD}$ | — |
| MDQS[0:8] | L26, J25, D25, A22, H18, F16, F14, C13, C20 | I/O | $GV_{DD}$ | — |
| MBA[0:1] | B18, B19 | O | $GV_{DD}$ | — |
| MA[0:14] | N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13 | O | $GV_{DD}$ | — |
| MWE | D17 | O | $GV_{DD}$ | — |
| MRAS | F17 | O | $GV_{DD}$ | — |
| MCAS | J16 | O | $GV_{DD}$ | — |
| MCS[0:3] | H16, G16, J15, H15 | O | $GV_{DD}$ | — |
| MCKE[0:1] | E26, E28 | O | $GV_{DD}$ | 11 |
| MCK[0:5] | J20, H25, A15, D20, F28, K14 | O | $GV_{DD}$ | — |
| MCK[0:5] | F20, G27, B15, E20, F27, L14 | O | $GV_{DD}$ | — |
| MSYNC_IN | M28 | I | $GV_{DD}$ | 22 |
| MSYNC_OUT | N28 | O | $GV_{DD}$ | 22 |
| **Local Bus Controller Interface** | | | | |
| LA[27] | U18 | O | $OV_{DD}$ | 5, 9 |

**Table 43. MPC8541E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LA[28:31] | T18, T19, T20, T21 | O | $OV_{DD}$ | 5, 7, 9 |
| LAD[0:31] | AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26 | I/O | $OV_{DD}$ | — |
| LALE | V21 | O | $OV_{DD}$ | 5, 8, 9 |
| LBCTL | V20 | O | $OV_{DD}$ | 9 |
| LCKE | U23 | O | $OV_{DD}$ | — |
| LCLK[0:2] | U27, U28, V18 | O | $OV_{DD}$ | — |
| $\overline{\text{LCS}}$[0:4] | Y27, Y28, W27, W28, R27 | O | $OV_{DD}$ | — |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$ | R28 | I/O | $OV_{DD}$ | 1 |
| $\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$ | P27 | O | $OV_{DD}$ | 1 |
| $\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$ | P28 | O | $OV_{DD}$ | 1 |
| LDP[0:3] | AA27, AA28, T26, P21 | I/O | $OV_{DD}$ | — |
| LGPL0/LSDA10 | U19 | O | $OV_{DD}$ | 5, 9 |
| LGPL1/$\overline{\text{LSDWE}}$ | U22 | O | $OV_{DD}$ | 5, 9 |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$ | V28 | O | $OV_{DD}$ | 5, 8, 9 |
| LGPL3/$\overline{\text{LSDCAS}}$ | V27 | O | $OV_{DD}$ | 5, 9 |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE | V23 | I/O | $OV_{DD}$ | 21 |
| LGPL5 | V22 | O | $OV_{DD}$ | 5, 9 |
| LSYNC_IN | T27 | I | $OV_{DD}$ | — |
| LSYNC_OUT | T28 | O | $OV_{DD}$ | — |
| $\overline{\text{LWE}}$[0:1]/LSDDQM[0:1]/ $\overline{\text{LBS}}$[0:1] | AB28, AB27 | O | $OV_{DD}$ | 1, 5, 9 |
| $\overline{\text{LWE}}$[2:3]/LSDDQM[2:3]/ $\overline{\text{LBS}}$[2:3] | T23, P24 | O | $OV_{DD}$ | 1, 5, 9 |
| **DMA** | | | | |
| $\overline{\text{DMA\_DREQ}}$[0:1] | H5, G4 | I | $OV_{DD}$ | — |
| $\overline{\text{DMA\_DACK}}$[0:1] | H6, G5 | O | $OV_{DD}$ | — |
| $\overline{\text{DMA\_DDONE}}$[0:1] | H7, G6 | O | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| $\overline{\text{MCP}}$ | AG17 | I | $OV_{DD}$ | — |
| $\overline{\text{UDE}}$ | AG16 | I | $OV_{DD}$ | — |

# 15 Clocking

This section describes the PLL configuration of the MPC8541E. Note that the platform clock is identical to the CCB clock.

## 15.1 Clock Ranges

Table 44 provides the clocking specifications for the processor core and Table 44 provides the clocking specifications for the memory bus.

**Table 44. Processor Core Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 533 MHz | | 600 MHz | | 667 MHz | | 833 MHz | | 1000 MHz | | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 400 | 533 | 400 | 600 | 400 | 667 | 400 | 833 | 400 | 1000 | MHz | 1, 2, 3 |

**Notes**:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2. )The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. 1000 MHz frequency supports only a 1.3 V core.

**Table 45. Memory Bus Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | Unit | Notes |
|---|---|---|---|---|
| | 533, 600, 667, 883, 1000 MHz | | | |
| | Min | Max | | |
| Memory bus frequency | 100 | 166 | MHz | 1, 2, 3 |

**Notes:**

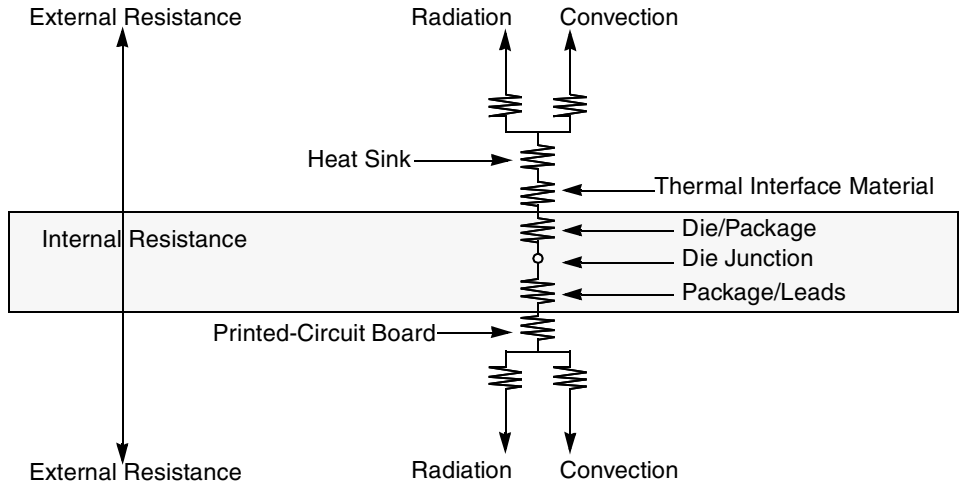
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. 1000 MHz frequency supports only a 1.3 V core.

### 16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 44 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.




(Note the internal versus external package resistance)

**Figure 44. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

### 16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 45 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 41). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

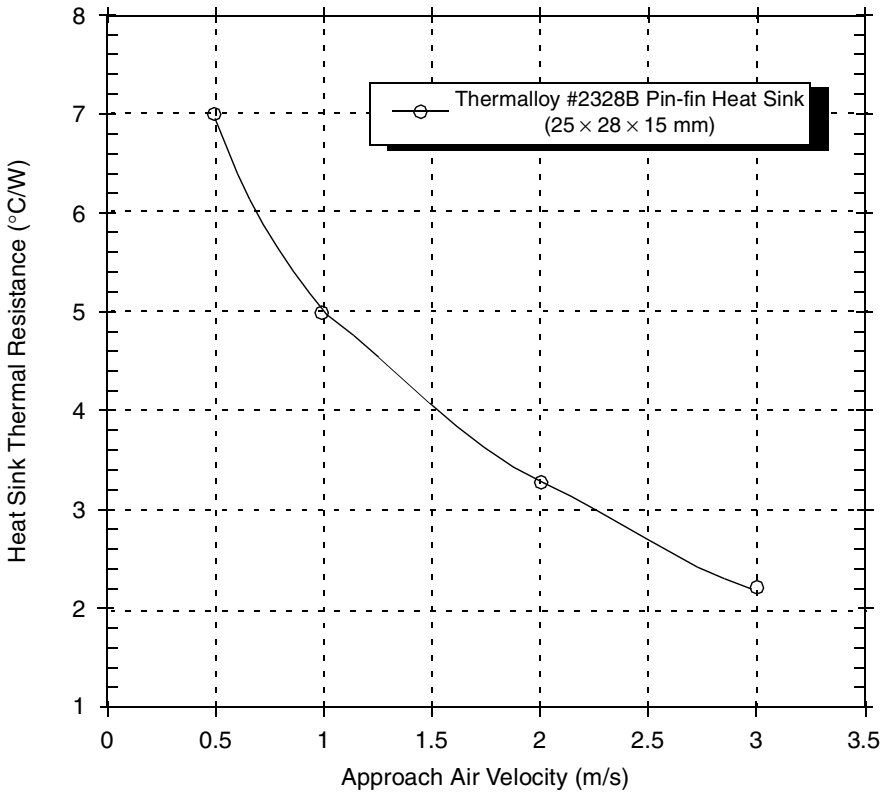



**Figure 46. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity**

### 16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in Table 49 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 47 and Figure 48. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 47 and provide exploded views of the plastic fence, heat sink, and spring clip.

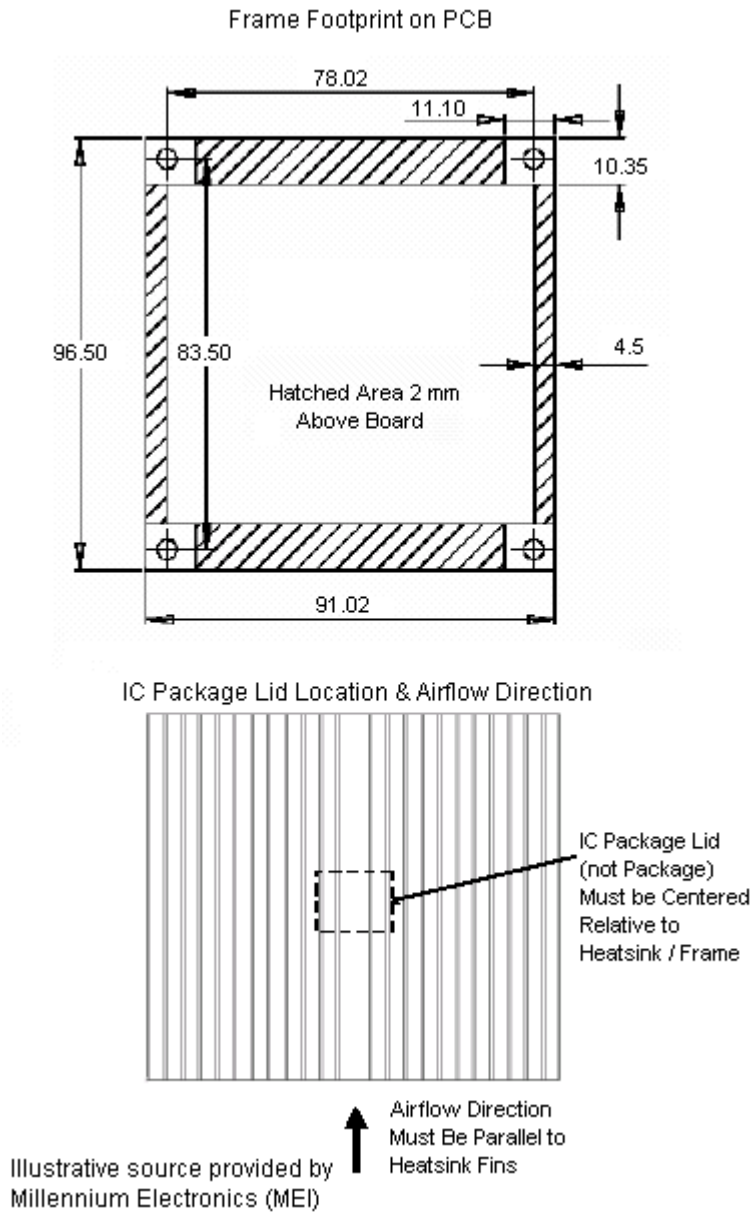



**Figure 47. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence**

When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

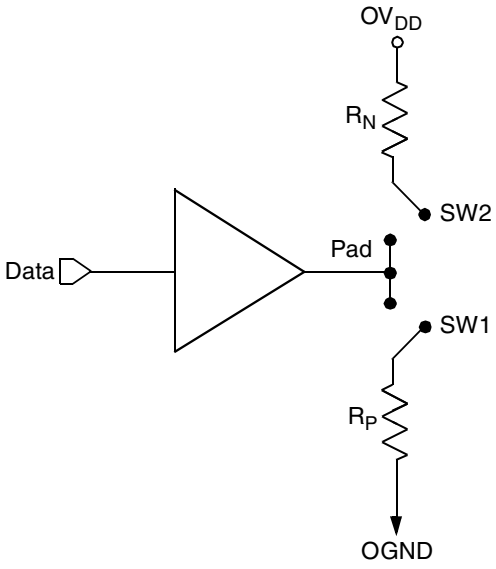



**Figure 50. Driver Impedance Measurement**

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value $R_{term}$. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 50 summarizes the signal impedance targets. The driver impedance are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 50. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 43 Target | 25 Target | 20 Target | $Z_0$ | Ω |
| $R_P$ | 43 Target | 25 Target | 20 Target | $Z_0$ | Ω |
| Differential | NA | NA | NA | $Z_{DIFF}$ | Ω |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

### 17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 52. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to $OV_{DD}$ through a 10 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

# 18 Document Revision History

Table 51 provides a revision history for this hardware specification.

**Table 51. Document Revision History**

| Rev. No. | Date | Substantive Change(s) |
|---|---|---|
| 4.2 | 1/2008 | Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.” |
| 4.1 | 07/2007 | Inserted Figure 3, ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.” |
| 4 | 12/2006 | Updated Section 2.1.2, “Power Sequencing.”<br>Updated back page information. |
| 3.2 | 11/2006 | Updated Section 2.1.2, “Power Sequencing.”<br>Replaced Section 17.8, “JTAG Configuration Signals.” |
| 3.1 | 10/2005 | Table 4: Added footnote 2 about junction temperature.<br>Table 4: Added max. power values for 1000 MHz core frequency.<br>Removed Figure 3, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.”<br>Table 30: Modified note to $t_{LBKSKEW}$ from 8 to 9<br>Table 30: Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values.<br>Table 30: Added note 3 to $t_{LBKHOV1}$.<br>Table 30 and Table 31: Modified note 3.<br>Table 31: Added note 3 to $t_{LBKLOV1}$.<br>Table 31: Modified values for $t_{LBKHKT}$, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$.<br>Figure 21: Changed Input Signals: LAD[0:31]/LDP[0:3].<br>Table 43: Modified note for signal CLK_OUT.<br>Table 43: PCI1_CLK and PCI2_CLK changed from I/O to I.<br>Table 52: Added column for Encryption Acceleration. |
| 3 | 8/29/2005 | Table 4: Modified max. power values.<br>Table 43: Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL. |
| 2 | 8/2005 | Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 31 is now listed as Table 31.<br>Table 7: Added note 2.<br>Table 14: Modified min and max values for $t_{DDKHMP}$ |
| 1 | 6/2005 | Table 27: Changed $LV_{dd}$ to $OV_{dd}$ for the supply voltage Ethernet management interface.<br>Table 4: Modified footnote 4 and changed typical power for the 1000MHz core frequency.<br>Table 31: Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state. |
| 0 | 6/2005 | Initial Release. |

# 19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, “Nomenclature of Parts Fully Addressed by this Document.”

## 19.1 Nomenclature of Parts Fully Addressed by this Document

Table 52 provides the Freescale part numbering nomenclature for the MPC8541E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 52. Part Numbering Nomenclature**

| MPC | *nnnn* | | *t* | *pp* | *aa* | *a* | *r* |
|---|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Encryption Acceleration** | **Temperature Range[1]** | **Package [2]** | **Processor Frequency [3]** | **Platform Frequency** | **Revision Level[4]** |
| MPC | 8541 | Blank = not included<br>E = included | Blank = 0 to 105°C<br>C = –40 to 105°C | PX = FC-PBGA<br>VT = FC-PBGA (lead free) | AJ = 533 MHz<br>AK = 600 MHz<br>AL = 667 MHz<br>AP = 833 MHz<br>AQ = 1000 MHZ | D = 266 MHz<br>E = 300 MHz<br>F = 333 MHz | |

**Notes:**

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.
2. See Section 14, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. Contact you local Freescale field applications engineer (FAE).