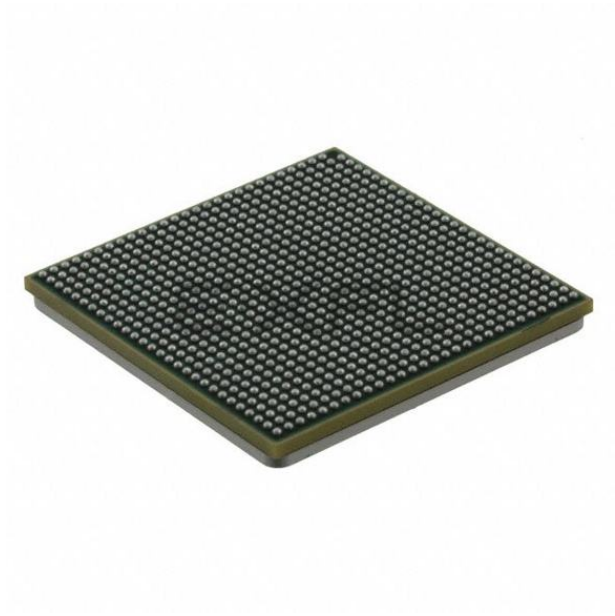

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8541cpxajd

- Security Engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std 802.11i™, iSCSI, and IKE processing. The Security Engine contains 4 Crypto-channels, a Controller, and a set of crypto Execution Units (EUs). The Execution Units are:
  - Public Key Execution Unit (PKEU) supporting the following:
    - RSA and Diffie-Hellman
    - Programmable field size up to 2048-bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511-bits
  - Data Encryption Standard Execution Unit (DEU)
    - DES, 3DES
    - Two key (K1, K2) or Three Key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced Encryption Standard Unit (AESU)
    - Implements the Rinjdael symmetric key cipher
    - Key lengths of 128, 192, and 256 bits.Two key
    - ECB, CBC, CCM, and Counter modes
  - ARC Four execution unit (AFEU)
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message Digest Execution Unit (MDEU)
    - SHA with 160-bit or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random Number Generator (RNG)
  - 4 Crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 Bytes for each execution unit, with flow control for large data sizes
- High-performance RISC CPM
  - Two full-duplex fast communications controllers (FCCs) that support the following protocol:
    - IEEE Std 802.3™/Fast Ethernet (10/100)
  - Serial peripheral interface (SPI) support for master or slave
  - I^2C bus controller
  - General-purpose parallel ports—16 parallel I/O lines with interrupt capability
- 256 Kbytes of on-chip memory
  - Can act as a 256-Kbyte level-2 cache
  - Can act as a 256-Kbyte or two 128-Kbyte memory-mapped SRAM arrays
  - Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
  - Full ECC support on 64-bit boundary in both cache and SRAM modes

4 Clock Timing

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8541E.

Table 6. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are ±1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8541E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise time	t_{G125R}	—	—	1.0	ns	1
EC_GTX_CLK125 fall time	t_{G125F}	—	—	1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	—
MDQS—MDQ/MECC input skew per byte For DDR = 333 MHz For DDR ≤ 266 MHz	t_{DISKEW}	—	 750 1125	ps	1

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	 –1000 –1100 –1200	 200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	 2.8 3.45 4.6	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	 2.0 2.65 3.8	—	ns	4
$\overline{\text{MCS}}$(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	 2.8 3.45 4.6	—	ns	4

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{MCS}$(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCX}	 2.0 2.65 3.8	—	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHMH}	 –0.9 –1.1 –1.2	 0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 900 1200	—	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 900 1200	—	ps	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.9$	$-0.5 \times t_{MCK} + 0.3$	ns	7
MDQS epilogue end	t_{DDKLME}	–0.9	0.3	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{MCK}$ can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle. The MCSx pins are separated from the ADDR/CMD (address and command) bus in the HW spec. This was separated because the MCSx pins typically have different loadings than the rest of the address and command bus, even though they have the same timings.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). In the source synchronous mode, MDQS can launch later than MCK by 0.3 ns at the maximum. However, MCK may launch later than MDQS by as much as 0.9 ns. t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this typically is set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8541E.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8541E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 provides the AC test load for the DDR bus.

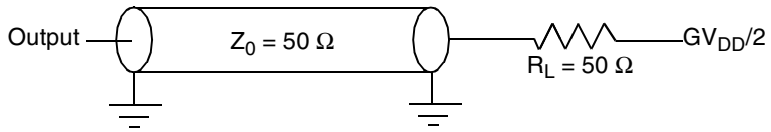


Figure 6. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:
1. Data input threshold measurement point.
2. Data output measurement point.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8541E.

7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8541E.

Table 16. DUART DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

Table 21. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} [2,3]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

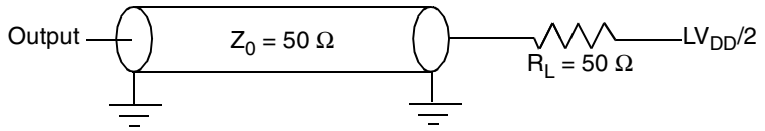


Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

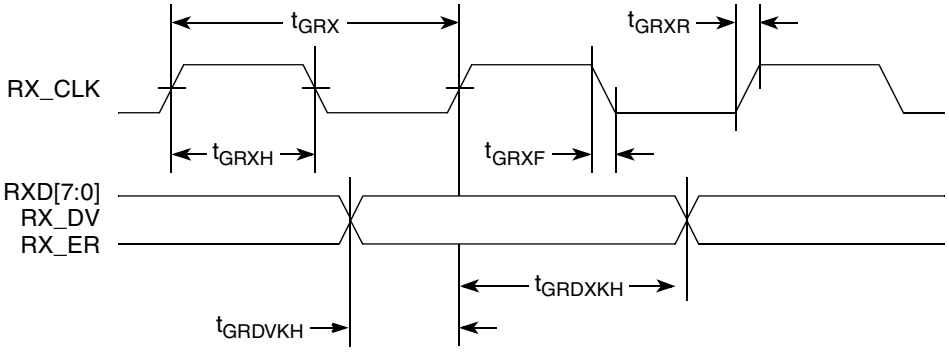


Figure 9. GMII Receive AC Timing Diagram

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.

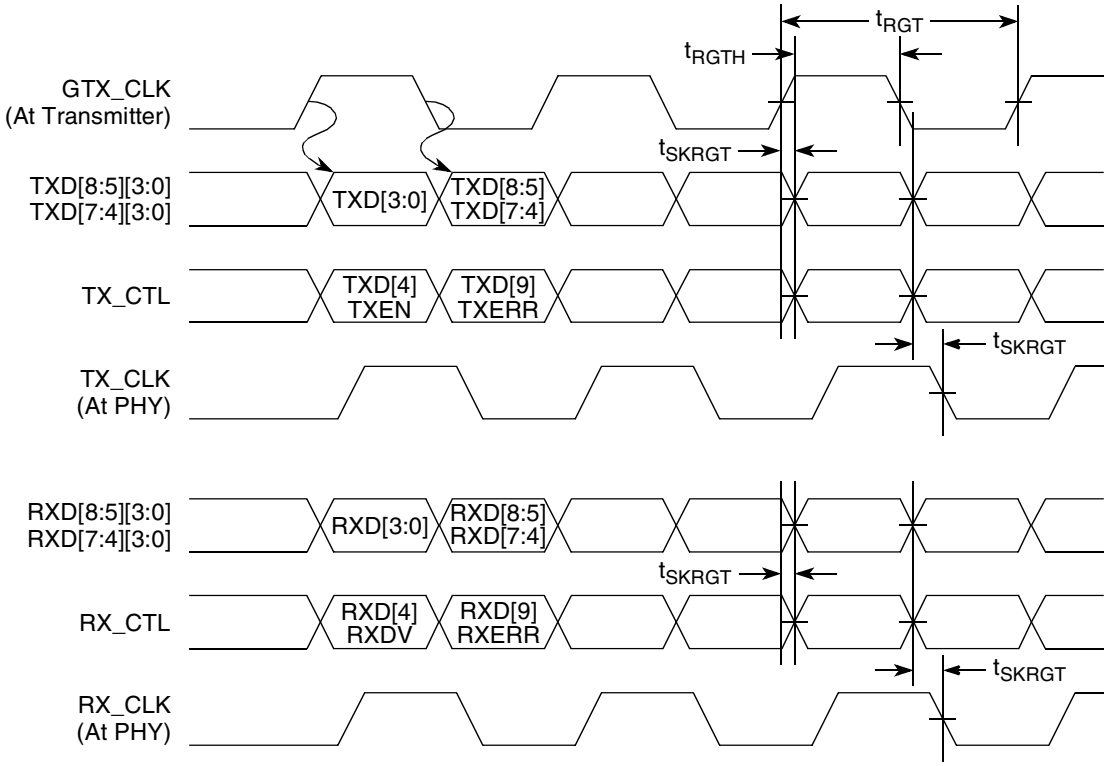


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		1.70	—	V
Input low voltage	V_{IL}	—		—	0.90	V

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8541E with the DLL enabled.

Table 30. Local Bus General Timing Parameters—DLL Enabled

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	—	ns	3, 4, 8
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5	—	ns	3, 4, 8
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV1}$	—	2.3	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			3.8		
Local bus clock to data valid for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV2}$	—	2.5	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			4.0		
Local bus clock to address valid for LAD	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV3}$	—	2.6	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			4.1		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOX1}$	0.7	—	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)		1.6			
Output hold from local bus clock for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOX2}$	0.7	—	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)		1.6			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOZ1}$	—	2.8	ns	5, 9
	$\overline{LWE[0:1]}$ = 11 (default)			4.2		

Table 30. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOZ2}$	—	2.8	ns	5, 9
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			4.2		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8541E with the DLL bypassed.

Table 31. Local Bus General Timing Parameters—DLL Bypassed

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay	—	t_{LBKHKT}	1.8	3.4	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	5.2	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	5.1	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	–1.3	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	–0.8	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOV1}$	—	0.5	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.0		
Local bus clock to data valid for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOV2}$	—	0.7	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.2		

Figure 17 to Figure 22 show the local bus signals.

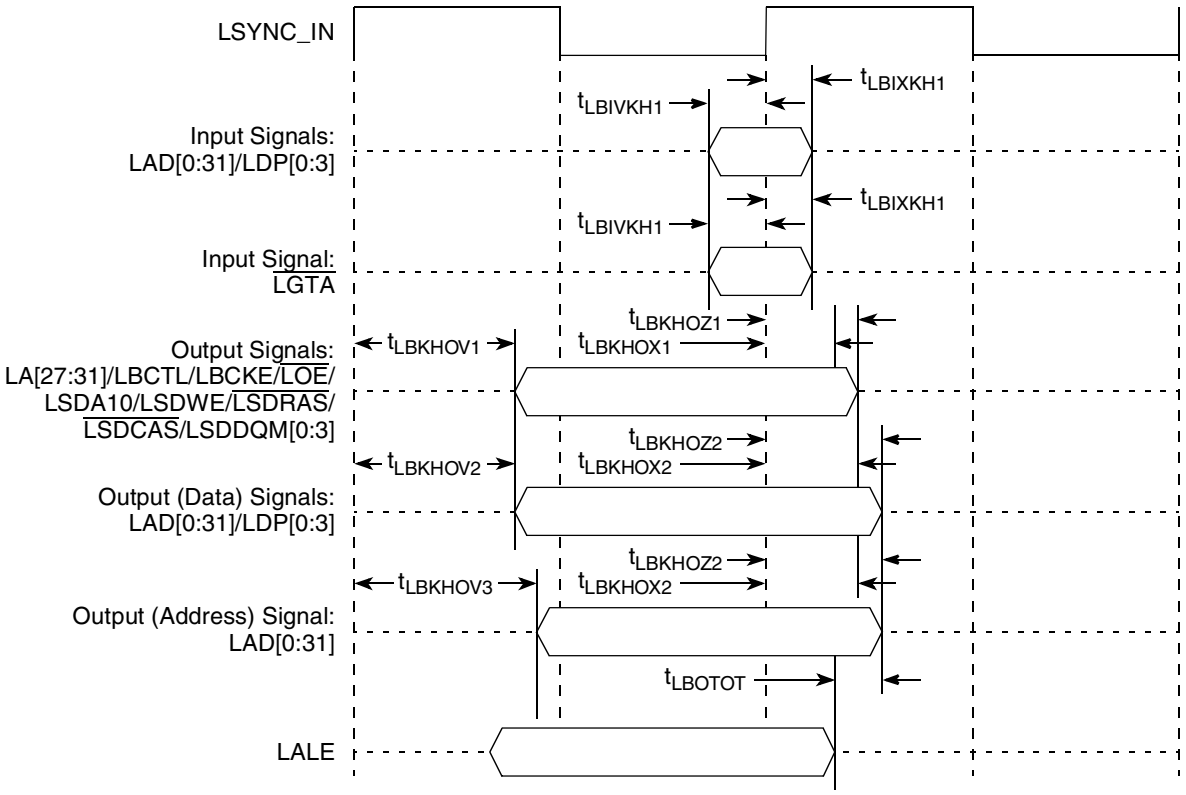


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

10.3 CPM I2C AC Specification

Table 35. I2C Timing

Characteristic	Expression	All Frequencies		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	0	F_{MAX}(1)	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	1/(2.2 * f_{SCL})	—	s
Low period of SCL	t_{SCLCH}	1/(2.2 * f_{SCL})	—	s
High period of SCL	t_{SCHCL}	1/(2.2 * f_{SCL})	—	s
Start condition setup time[2]	t_{SCHDL}	2/(divider * f_{SCL})	(2)	s
Start condition hold time[2]	t_{SDLCL}	3/(divider * f_{SCL})	—	s
Data hold time [2]	t_{SCLDX}	2/(divider * f_{SCL})	—	s
Data setup time[2]	t_{SDVCH}	3/(divider * f_{SCL})	—	s
SDA/SCL rise time	t_{SRISE}	—	1/(10 * f_{SCL})	s
SDA/SCL fall time	t_{SFALL}	—	1/(33 * f_{SCL})	s
Stop condition setup time	t_{SCHDH}	2/(divider * f_{SCL})	—	s

Notes:

1. F_{MAX} = BRGCLK/(min_divider*prescale. Where prescaler=25-I2MODE[PDIV]; and min_divider=12 if digital filter disabled and 18 if enabled.
   Example #1: if I2MODE[PDIV]=11 (prescaler=4) and I2MODE[FLT]=0 (digital filter disabled) then FMAX=BRGCLK/48
   Example #2: if I2MODE[PDIV]=00 (prescaler=32) and I2MODE[FLT]=1 (digital filter enabled) then FMAX=BRGCLK/576
2. divider = f_{SCL}/prescaler.
   In master mode: divider=BRGCLK/(f_{SCL}*prescaler)=2*(I2BRG[DIV]+3)
   In slave mode: divider=BRGCLK/(f_{SCL}*prescaler)

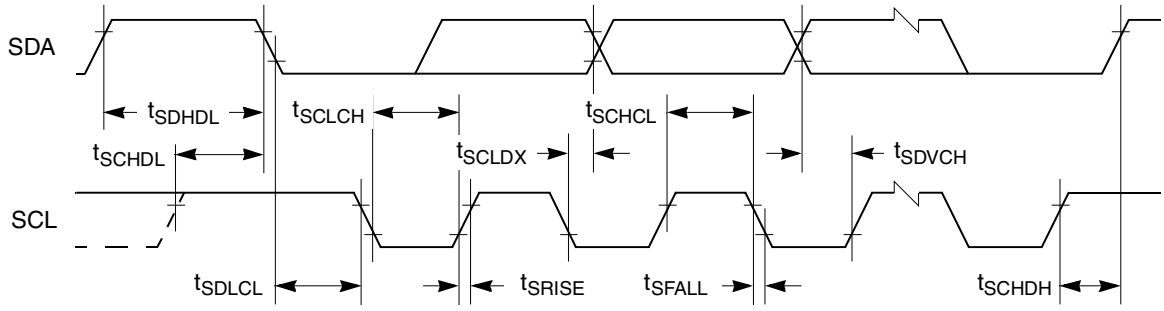


Figure 30. CPM I2C Bus Timing Diagram

The following two tables are examples of I2C AC parameters at I2C clock value of 100k and 400k respectively.

Table 36. CPM I2C Timing (f_{SCL}=100 kHz)

Characteristic	Expression	Frequency = 100 kHz		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	—	100	kHz
SCL clock frequency (master)	f_{SCL}	—	100	kHz
Bus free time between transmissions	t_{SDHDL}	4.7	—	µs
Low period of SCL	t_{SCLCH}	4.7	—	µs
High period of SCL	t_{SCHCL}	4	—	µs
Start condition setup time	t_{SCHDL}	2	—	µs
Start condition hold time	t_{SDLCL}	3	—	µs
Data hold time	t_{SCLDX}	2	—	µs
Data setup time	t_{SDVCH}	3	—	µs
SDA/SCL rise time	t_{SRISE}	—	1	µs
SDA/SCL fall time (master)	t_{SFALL}	—	303	ns
Stop condition setup time	t_{SCHDH}	2	—	µs

Table 37. CPM I2C Timing (f_{SCL}=400 kHz)

Characteristic	Expression	Frequency = 400 kHz		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	—	400	kHz
SCL clock frequency (master)	f_{SCL}	—	400	kHz
Bus free time between transmissions	t_{SDHDL}	1.2	—	µs
Low period of SCL	t_{SCLCH}	1.2	—	µs
High period of SCL	t_{SCHCL}	1	—	µs
Start condition setup time	t_{SCHDL}	420	—	ns
Start condition hold time	t_{SDLCL}	630	—	ns
Data hold time	t_{SCLDX}	420	—	ns
Data setup time	t_{SDVCH}	630	—	ns
SDA/SCL rise time	t_{SRISE}	—	250	ns
SDA/SCL fall time	t_{SFALL}	—	75	ns
Stop condition setup time	t_{SCHDH}	420	—	ns

12.2 I^2C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I^2C interface of the MPC8541E.

Table 40. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [6]	1.3	—	μs
High period of the SCL clock	t_{I2CH} [6]	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} [6]	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [6]	0.6	—	μs
Data setup time	t_{I2DVKH} [6]	100	—	ns
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8541E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. Guaranteed by design.

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV_{DD}	—
IRQ8	AB20	I	OV_{DD}	9
IRQ9/$\overline{\text{DMA\_DREQ3}}$	Y20	I	OV_{DD}	1
IRQ10/$\overline{\text{DMA\_DACK3}}$	AF26	I/O	OV_{DD}	1
IRQ11/$\overline{\text{DMA\_DDONE3}}$	AH24	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV_{DD}	5, 9
EC_MDIO	E1	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV_{DD}	—
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV_{DD}	9, 18
TSEC1_TX_EN	C8	O	LV_{DD}	11
TSEC1_TX_ER	B8	O	LV_{DD}	—
TSEC1_TX_CLK	C6	I	LV_{DD}	—
TSEC1_GTX_CLK	B6	O	LV_{DD}	—
TSEC1_CRS	C3	I	LV_{DD}	—
TSEC1_COL	G7	I	LV_{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV_{DD}	—
TSEC1_RX_DV	D2	I	LV_{DD}	—
TSEC1_RX_ER	E5	I	LV_{DD}	—
TSEC1_RX_CLK	D6	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV_{DD}	—
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV_{DD}	5, 9, 18
TSEC2_TX_EN	B11	O	LV_{DD}	11
TSEC2_TX_ER	D11	O	LV_{DD}	—
TSEC2_TX_CLK	D10	I	LV_{DD}	—
TSEC2_GTX_CLK	C10	O	LV_{DD}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AF21	I	OV_{DD}	—
TDI	AG21	I	OV_{DD}	12
TDO	AF19	O	OV_{DD}	11
TMS	AF23	I	OV_{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV_{DD}	12
DFT				
$\overline{\text{LSSD\_MODE}}$	AG19	I	OV_{DD}	20
L1_TSTCLK	AB22	I	OV_{DD}	20
L2_TSTCLK	AG22	I	OV_{DD}	20
TEST_SEL0	AH20	I	OV_{DD}	3
TEST_SEL1	AG26	I	OV_{DD}	3
Thermal Management				
THERM0	AG2	—	—	14
THERM1	AH3	—	—	14
Power Management				
ASLEEP	AG18	—	—	9, 18
Power and Ground Signals				
$AV_{DD}1$	AH19	Power for e500 PLL (1.2 V)	$AV_{DD}1$	—
$AV_{DD}2$	AH18	Power for CCB PLL (1.2 V)	$AV_{DD}2$	—
$AV_{DD}3$	AH17	Power for CPM PLL (1.2 V)	$AV_{DD}3$	—
$AV_{DD}4$	AF28	Power for PCI1 PLL (1.2 V)	$AV_{DD}4$	—
$AV_{DD}5$	AE28	Power for PCI2 PLL (1.2 V)	$AV_{DD}5$	—

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 46.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 46. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

Table 47. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 48. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	17	25	33	42	67	83	100	111	133
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

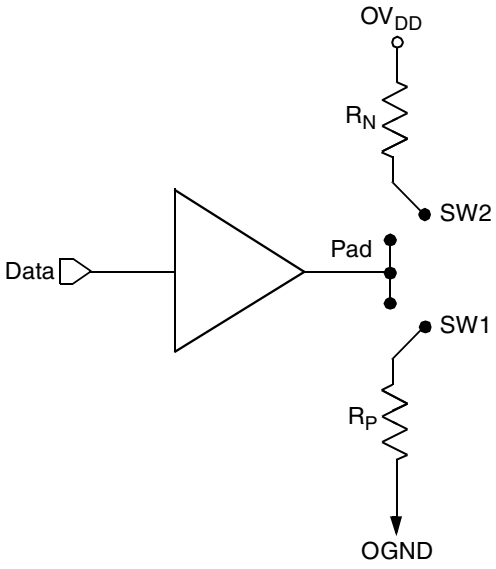


Figure 50. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 50 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 50. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	Ω
R_P	43 Target	25 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 51 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 51, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 51 is common to all known emulators.

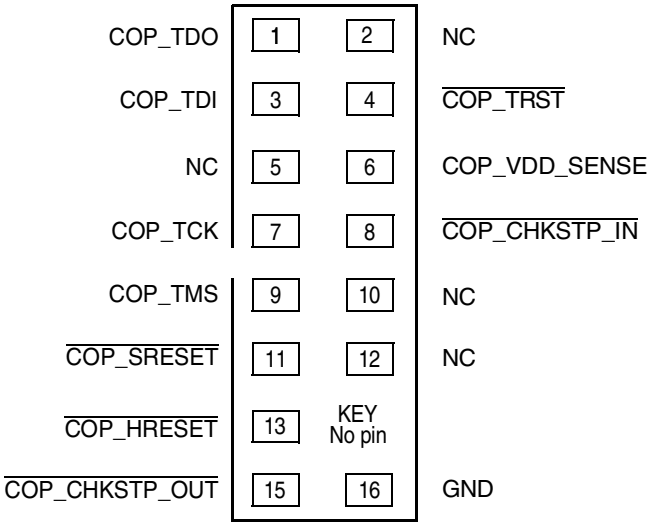
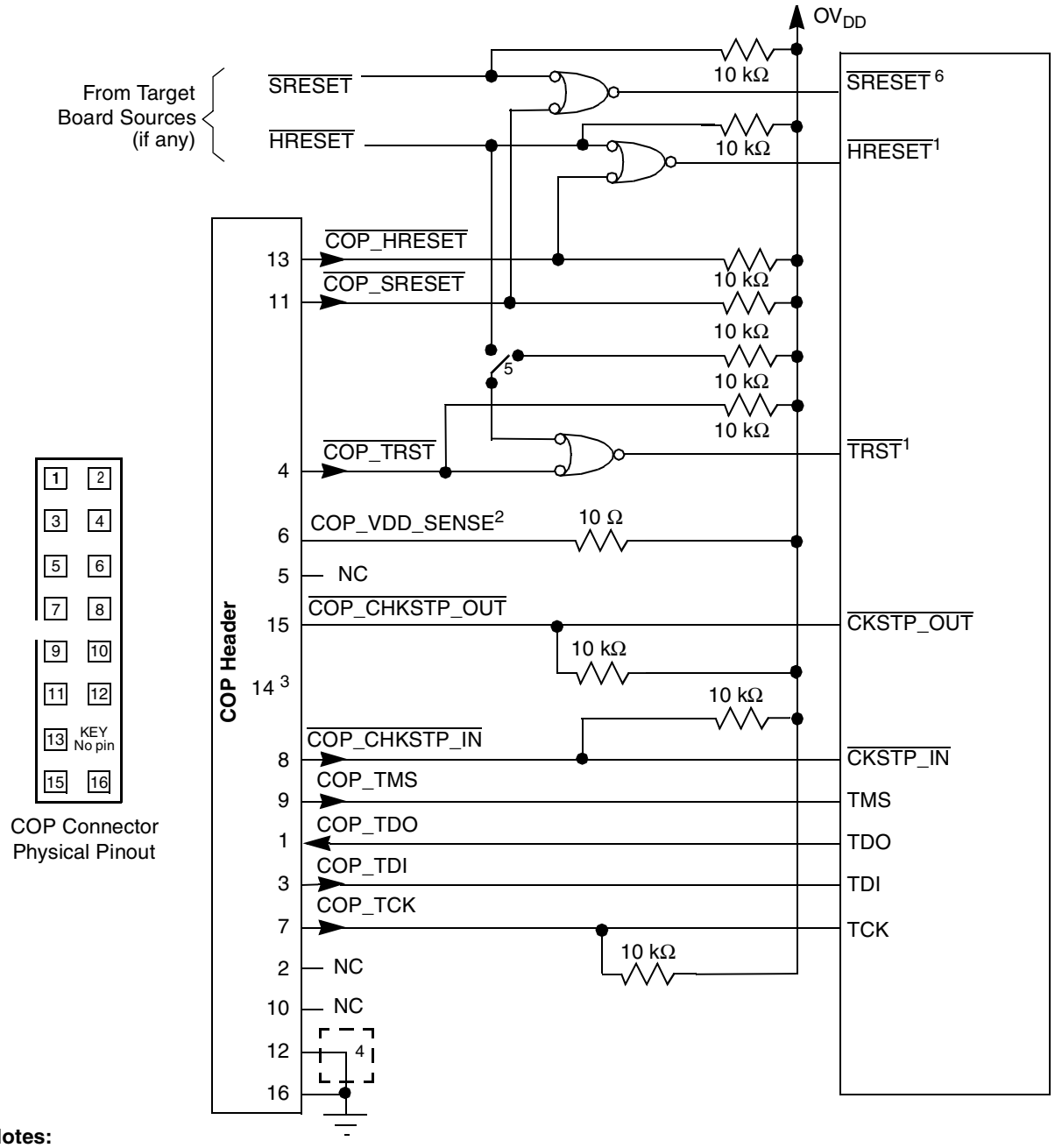


Figure 51. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 52. JTAG Interface Connection