



Welcome to E-XFL.COM

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8541epxapf

- Four global high resolution timers/counters that can generate interrupts
- Supports additional internal interrupt sources
- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- Two I²C controllers (one is contained within the CPM, the other is a stand-alone controller which is not part of the CPM)
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the stand-alone I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (RXD, TXD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 166 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Two Three-speed (10/100/1000)Ethernet controllers (TSECs)
 - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z AC compliant controllers
 - Support for Ethernet physical interfaces:
 - 10/100/1000 Mbps IEEE 802.3 GMII
 - 10/100 Mbps IEEE 802.3 MII
 - 10 Mbps IEEE 802.3 MII

4 Clock Timing

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8541E.

Table 6. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- For spread spectrum clocking, guidelines are $\pm 1\%$ of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8541E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise time	t_{G125R}	—	—	1.0	ns	1
EC_GTX_CLK125 fall time	t_{G125F}	—	—	1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI	$t_{\text{G125H}}/t_{\text{G125}}$	45 47	—	55 53	%	1, 2

Notes:

- Timing is guaranteed by design and characterization.
- EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

 At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHGX}	2.0 2.65 3.8	—	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKMHM}	-0.9 -1.1 -1.2	0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	900 900 1200	—	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	900 900 1200	—	ps	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.9$	$-0.5 \times t_{MCK} + 0.3$	ns	7
MDQS epilogue end	t_{DDKLME}	-0.9	0.3	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals $\pm 0.1\text{ V}$.
- In the source synchronous mode, MCK/ \overline{MCK} can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except \overline{MCK} , \overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle. The MCSx pins are separated from the ADDR/CMD (address and command) bus in the HW spec. This was separated because the MCSx pins typically have different loadings than the rest of the address and command bus, even though they have the same timings.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). In the source synchronous mode, MDQS can launch later than MCK by 0.3 ns at the maximum. However, MCK may launch later than MDQS by as much as 0.9 ns. t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this typically is set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8541E.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8541E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2 GMII Transmit AC Timing Specifications

Table 20 provides the GMII transmit AC timing specifications.

Table 20. GMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise and fall times	$t_{GTXR}^3, t_{GTXF}^{2,4}$	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

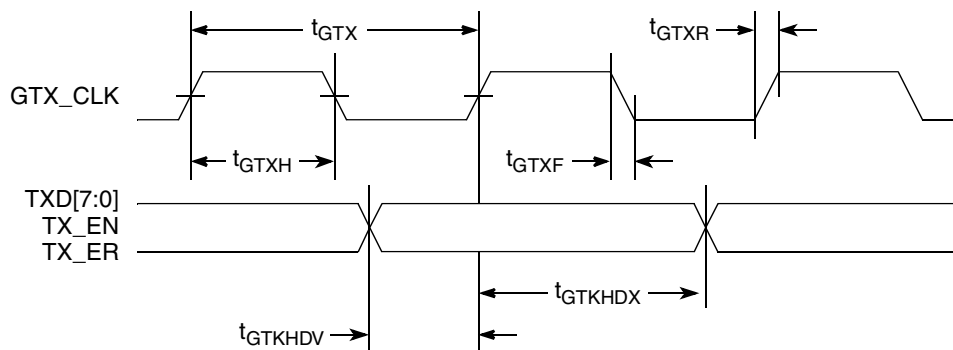


Figure 7. GMII Transmit AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. TBI Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR} , t_{TTXF} ^{2,3}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}(reference)(state)$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

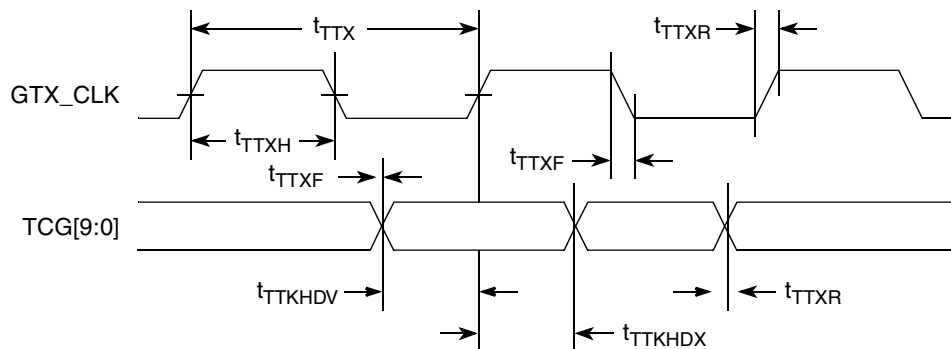


Figure 12. TBI Transmit AC Timing Diagram

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.

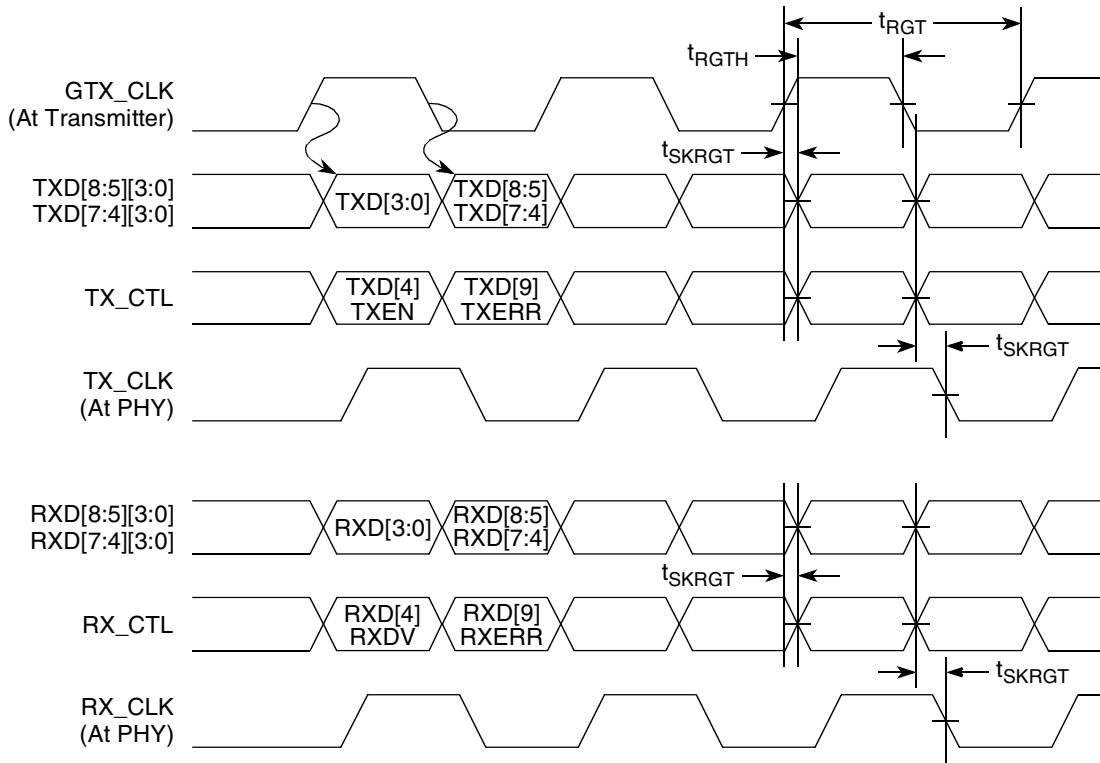


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, “Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	$LV_{DD} = \text{Min}$	2.10	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—		1.70	—	V
Input low voltage	V_{IL}	—		—	0.90	V

Table 27. MII Management DC Electrical Characteristics (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input high current	I_{IH}	$LV_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	μA
Input low current	I_{IL}	$LV_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	-600	—	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is $3.3 \text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHDV}			$2^*[1/(f_{ccb_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2^*[1/(f_{ccb_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
- This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
- Guaranteed by design.

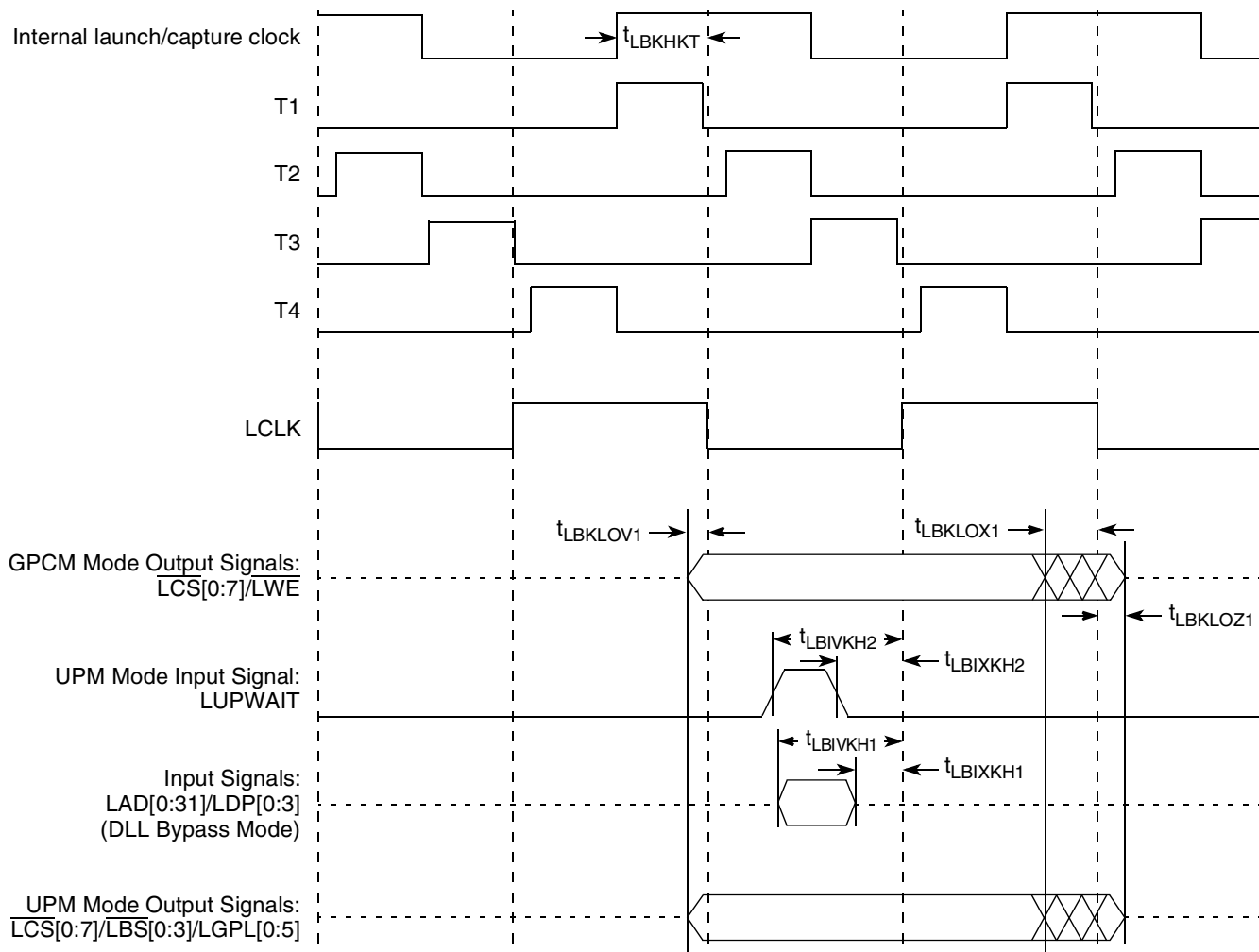
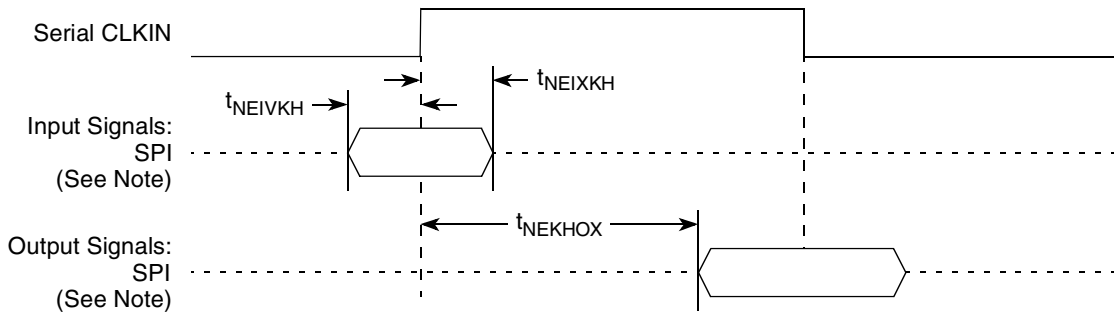


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

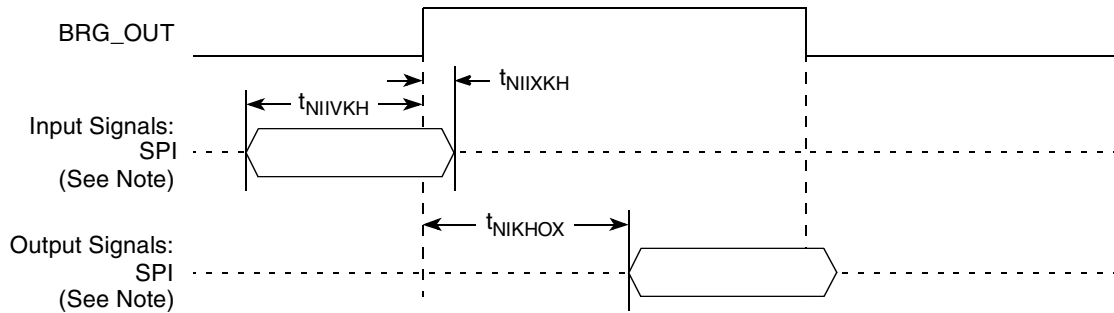
Figure 27 shows the SPI external clock.



Note: The clock edge is selectable on SPI.

Figure 27. SPI AC Timing External Clock Diagram

Figure 28 shows the SPI internal clock.



Note: The clock edge is selectable on SPI.

Figure 28. SPI AC Timing Internal Clock Diagram

NOTE

¹ SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

² SPI AC timings refer always to SPICLK.

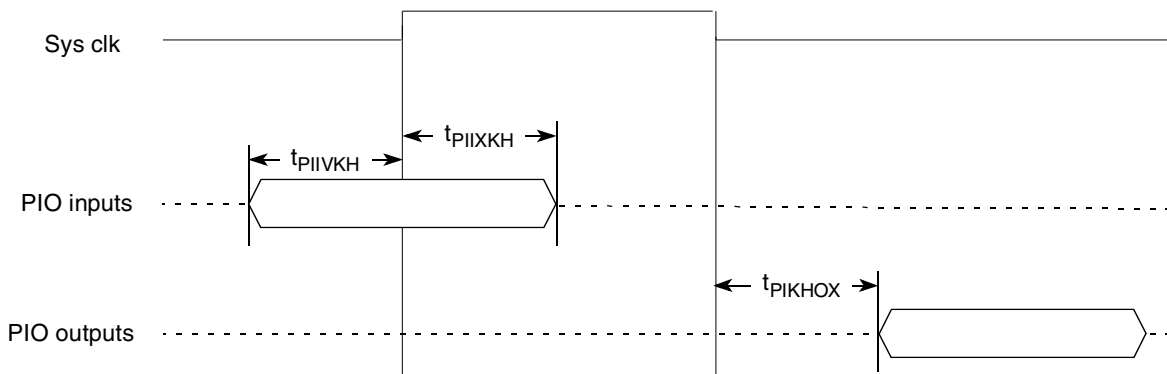


Figure 29. PIO Signal Diagram

Figure 16 provides the AC test load for the I²C.

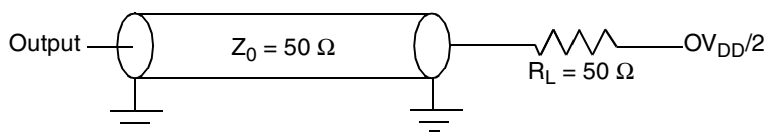


Figure 36. I²C AC Test Load

Figure 37 shows the AC timing diagram for the I²C bus.

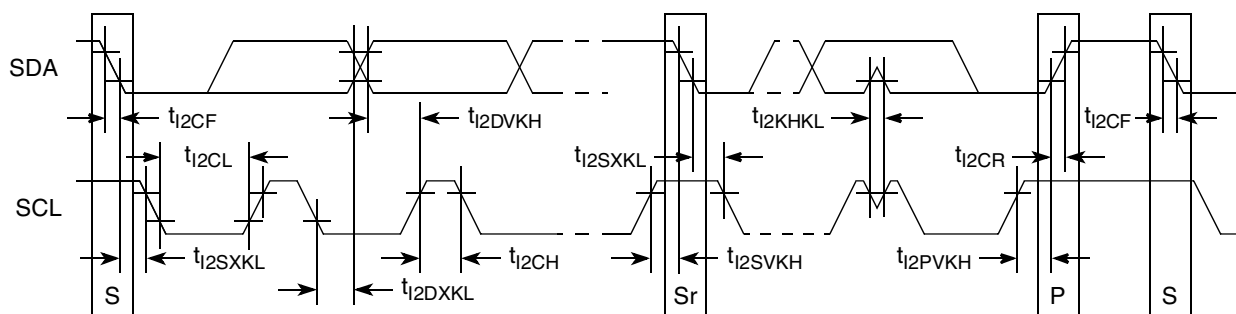


Figure 37. I²C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8541E.

13.1 PCI DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI interface of the MPC8541E.

Table 41. PCI DC Electrical Characteristics ¹

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} (\text{min})$ or	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} (\text{max})$	-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^2 = 0 \text{ V}$ or $V_{IN} = V_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min}$, $I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min}$, $I_{OL} = 100 \mu\text{A}$	—	0.2	V

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications.
2. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 39 shows the PCI input AC timing conditions.

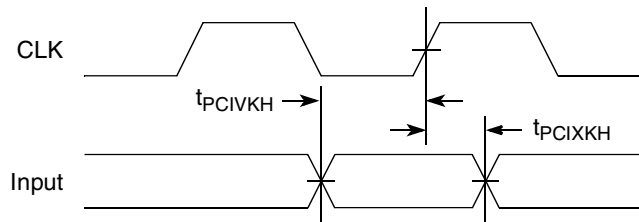


Figure 39. PCI Input AC Timing Measurement Conditions

Figure 40 shows the PCI output AC timing conditions.

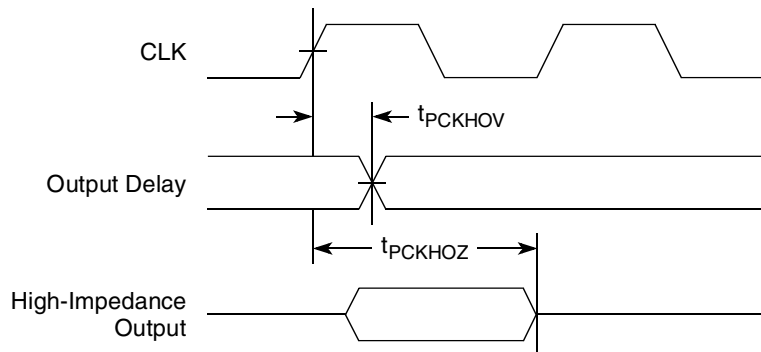


Figure 40. PCI Output AC Timing Measurement Condition

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8541E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	8.7 mm × 9.3 mm × 0.75 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8541E, 783 FC-PBGA package.

Table 43. MPC8541E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (one 64-bit or two 32-bit)				
PCI1_AD[63:32], PCI2_AD[31:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV _{DD}	17
PCI_C_BE64[7:4] PCI2_C_BE[3:0]	AG13, AH13, V14, W14	I/O	OV _{DD}	17
PCI_C_BE64[3:0] PCI1_C_BE[3:0]	AH8, AB10, AD11, AC12	I/O	OV _{DD}	17
PCI1_PAR	AA11	I/O	OV _{DD}	—
PCI1_PAR64/PCI2_PAR	Y14	I/O	OV _{DD}	—
PCI1_FRAME	AC10	I/O	OV _{DD}	2
PCI1_TRDY	AG10	I/O	OV _{DD}	2
PCI1_IRDY	AD10	I/O	OV _{DD}	2
PCI1_STOP	V11	I/O	OV _{DD}	2
PCI1_DEVSEL	AH10	I/O	OV _{DD}	2
PCI1_IDSEL	AA9	I	OV _{DD}	—
PCI1_REQ64/PCI2_FRAME	AE13	I/O	OV _{DD}	5, 10
PCI1_ACK64/PCI2_DEVSEL	AD13	I/O	OV _{DD}	2
PCI1_PERR	W11	I/O	OV _{DD}	2
PCI1_SERR	Y11	I/O	OV _{DD}	2, 4
PCI1_REQ[0]	AF5	I/O	OV _{DD}	—
PCI1_REQ[1:4]	AF3, AE4, AG4, AE5	I	OV _{DD}	—
PCI1_GNT[0]	AE6	I/O	OV _{DD}	—
PCI1_GNT[1:4]	AG5, AH5, AF6, AG6	O	OV _{DD}	5, 9
PCI1_CLK	AH25	I	OV _{DD}	—
PCI2_CLK	AH27	I	OV _{DD}	—
PCI2_GNT[0]	AC18	I/O	OV _{DD}	—

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in [Table 46](#).

There is no default for this PLL ratio; these signals must be pulled to the desired values.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 46. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

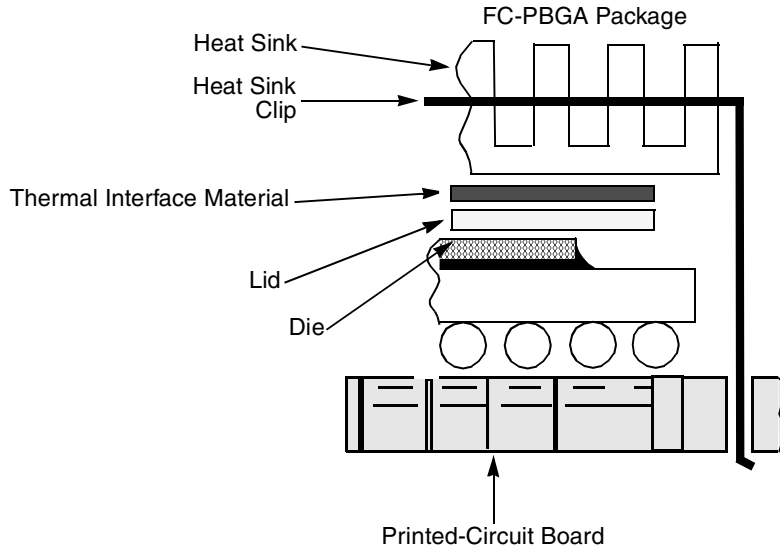


Figure 42. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8541E. There are several commercially-available heat sinks from the following vendors:

- | | |
|--|--------------|
| Aavid Thermalloy
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com | 603-224-9988 |
| Alpha Novatech
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI)
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-millennium.com | 408-436-8770 |
| Tyco Electronics
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com | 603-635-5102 |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that allows the MPC8541E to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8541E thermal model is shown in Figure 44. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

Conductivity	Value	Unit
Lid (11 × 11 × 1 mm)		
k_x	360	W/(m × K)
k_y	360	
k_z	360	
Lid Adhesive—Collapsed resistance (8.7 × 9.3 × 0.05 mm)		
k_z	1.07	
Die (8.7 × 9.3 × 0.75 mm)		
Bump/Underfill—Collapsed resistance (8.7 × 9.3 × 0.07 mm)		
k_z	4.4	
Substrate and Solder Balls (25 × 25 × 1.6 mm)		
k_x	14.2	
k_y	14.2	
k_z	1.2	

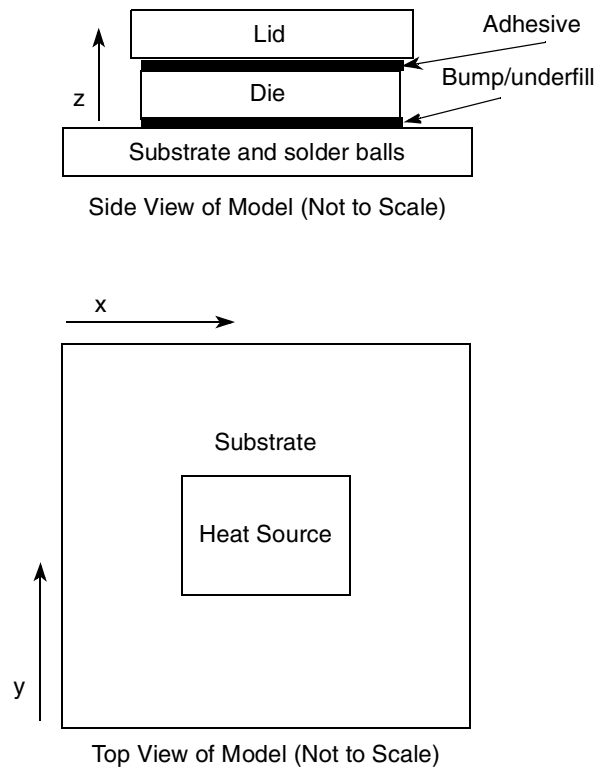


Figure 43. MPC8541E Thermal Model

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 44 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

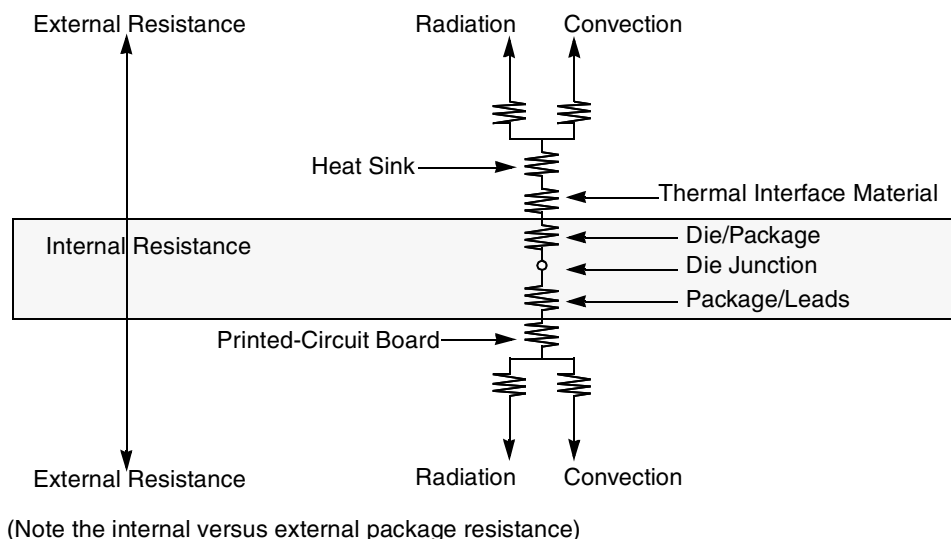


Figure 44. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 45 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 41). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 47 and provide exploded views of the plastic fence, heat sink, and spring clip.

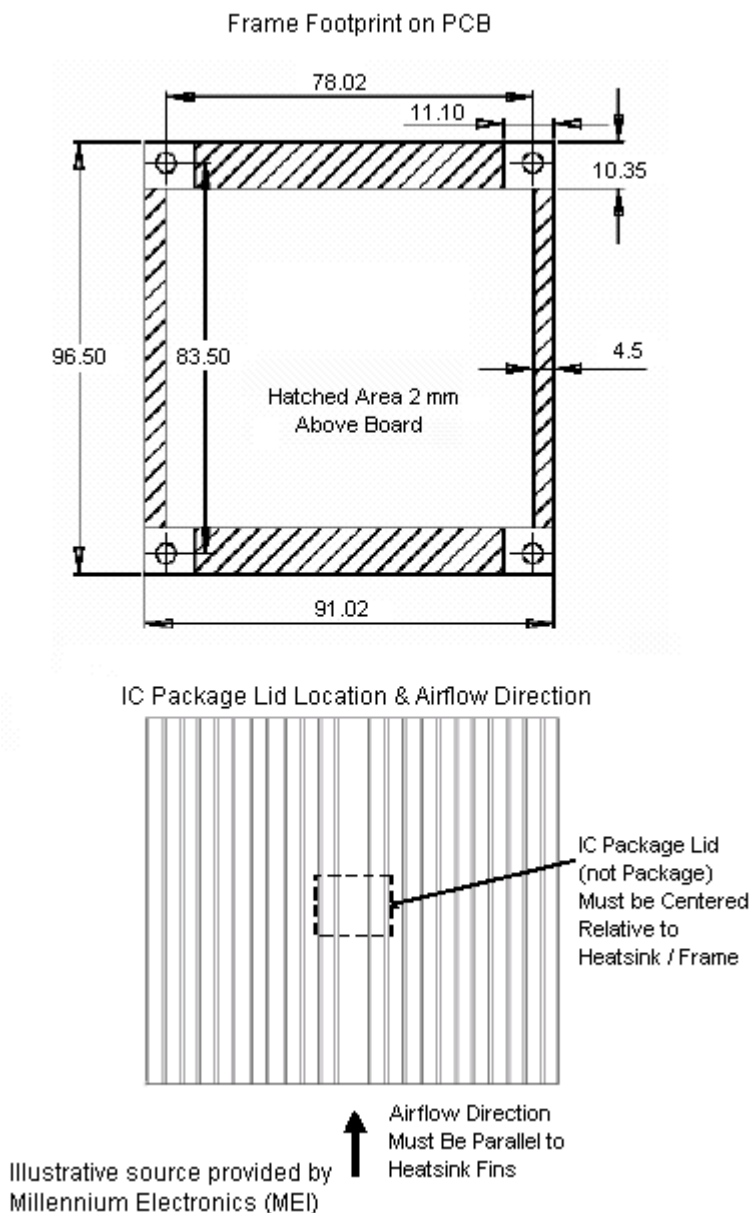


Figure 47. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 52](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added "Note: Rise/Fall Time on CPM Input Pins" and following note text to Section 10.2, "CPM AC Timing Specifications."
4.1	07/2007	Inserted Figure 3 , "Maximum AC Waveforms on PCI interface for 3.3-V Signaling."
4	12/2006	Updated Section 2.1.2, "Power Sequencing." Updated back page information.
3.2	11/2006	Updated Section 2.1.2, "Power Sequencing." Replaced Section 17.8, "JTAG Configuration Signals."
3.1	10/2005	Table 4 : Added footnote 2 about junction temperature. Table 4 : Added max. power values for 1000 MHz core frequency. Removed Figure 3 , "Maximum AC Waveforms on PCI Interface for 3.3-V Signaling." Table 30 : Modified note to $t_{LBKSKEW}$ from 8 to 9 Table 30 : Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values. Table 30 : Added note 3 to $t_{LBKHOV1}$. Table 30 and Table 31 : Modified note 3. Table 31 : Added note 3 to $t_{LBKLOV1}$. Table 31 : Modified values for t_{LBKHKT} , $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$. Figure 21 : Changed Input Signals: LAD[0:31]/LDP[0:3]. Table 43 : Modified note for signal CLK_OUT. Table 43 : PCI1_CLK and PCI2_CLK changed from I/O to I. Table 52 : Added column for Encryption Acceleration.
3	8/29/2005	Table 4 : Modified max. power values. Table 43 : Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL.
2	8/2005	Previous revision's history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 31 is now listed as Table 31 . Table 7 : Added note 2. Table 14 : Modified min and max values for t_{DDKHMP}
1	6/2005	Table 27 : Changed V_{DD} to V_{DD} for the supply voltage Ethernet management interface. Table 4 : Modified footnote 4 and changed typical power for the 1000MHz core frequency. Table 31 : Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state.
0	6/2005	Initial Release.

THIS PAGE INTENTIONALLY LEFT BLANK