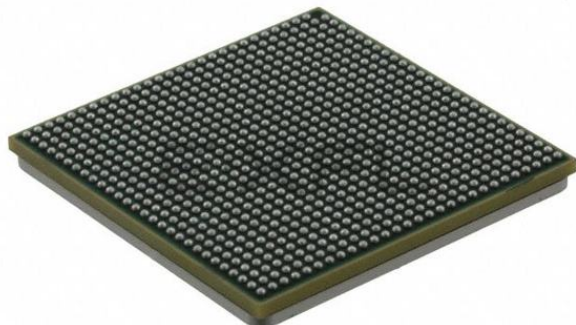




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8541evtake

- 1000 Mbps IEEE 802.3z TBI
 - 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking
- OCeaN switch fabric
 - Three-port crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no-snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI Controllers
 - PCI 2.2 compatible
 - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
 - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes
 - PCI 3.3-V compatible

- Selectable hardware-enforced coherency
- Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
 - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
 - Supports power save modes: doze, nap, and sleep
 - Employs dynamic power management
 - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8541E. The MPC8541E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay does not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8541E may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8541E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		V_{DD}	1.2 V $\pm$ 60 mV 1.3 V $\pm$ 50 mV (for 1 GHz only)	V
PLL supply voltage		AV_{DD}	1.2 V $\pm$ 60 mV 1.3 V $\pm$ 50 mV (for 1 GHz only)	V
DDR DRAM I/O voltage		GV_{DD}	2.5 V $\pm$ 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V $\pm$ 165 mV 2.5 V $\pm$ 125 mV	V
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	3.3 V $\pm$ 165 mV	V
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI, local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction Temperature		T_j	0 to 105	°C

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8541E.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8541E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	-10	10	μA	4
Output high current ($V_{OUT} = 1.95$ V)	I_{OH}	-15.2	—	mA	—
Output low current ($V_{OUT} = 0.35$ V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	5	μA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

Table 18. GMII, MII, and TBI DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	1.70	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	40	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-600	—	μA

Note:

- The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 19. GMII, MII, RGMII RTBI, and TBI DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	2.37	2.63	V
Output high voltage ($LV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.00	$LV_{DD} + 0.3$	V
Output low voltage ($LV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	$\text{GND} - 0.3$	0.40	V
Input high voltage ($LV_{DD} = \text{Min}$)	V_{IH}	1.70	$LV_{DD} + 0.3$	V
Input low voltage ($LV_{DD} = \text{Min}$)	V_{IL}	-0.3	0.70	V
Input high current ($V_{IN}^1 = LV_{DD}$)	I_{IH}	—	10	μA
Input low current ($V_{IN}^1 = \text{GND}$)	I_{IL}	-15	—	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. TBI Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	t_{TTKHdV}	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHdX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR} , t_{TTXF} ^{2,3}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHdV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHdX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

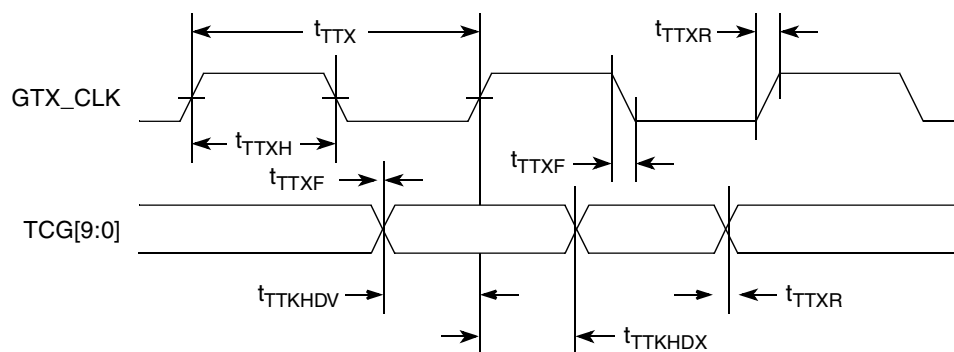


Figure 12. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 25 provides the TBI receive AC timing specifications.

Table 25. TBI Receive AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRX}		16.0		ns
RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising RX_CLK	t_{TRDXKH}	1.5	—	—	ns
RX_CLK clock rise time and fall time	t_{TRXR}, t_{TRXF} ^{2,3}	0.7	—	2.4	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Guaranteed by design.

Figure 13 shows the TBI receive AC timing diagram.

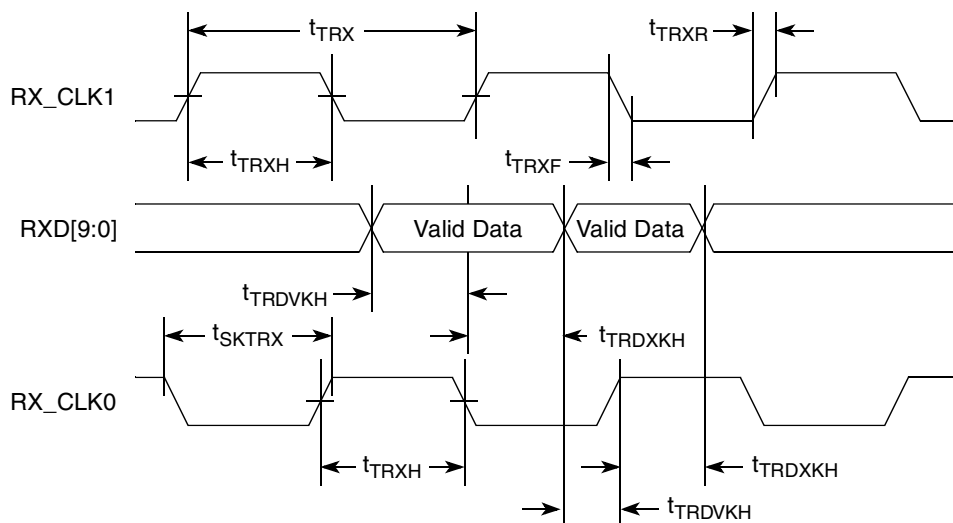


Figure 13. TBI Receive AC Timing Diagram

Table 27. MII Management DC Electrical Characteristics (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input high current	I_{IH}	$LV_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	μA
Input low current	I_{IL}	$LV_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	−600	—	μA

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is $3.3 \text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHVD}			$2 \cdot [1/(f_{ccb_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2 \cdot [1/(f_{ccb_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
- This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
- Guaranteed by design.

Figure 35 provides the test access port timing diagram.

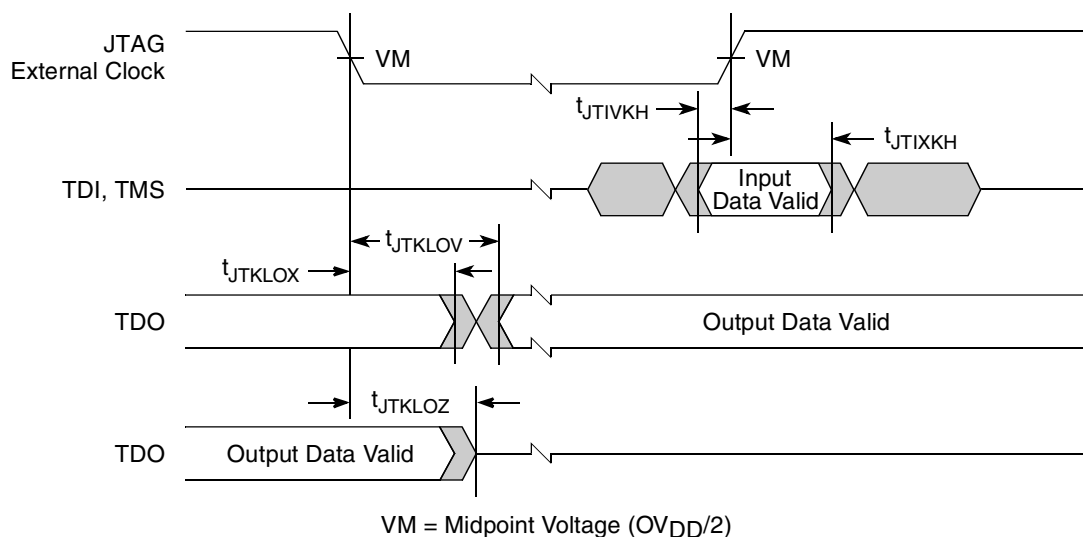


Figure 35. Test Access Port Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8541E.

12.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8541E.

Table 39. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}(\text{max})$)	I_I	-10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I²C interface of the MPC8541E.

Table 40. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} ⁶	1.3	—	μs
High period of the SCL clock	t_{I2CH} ⁶	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} ⁶	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} ⁶	0.6	—	μs
Data setup time	t_{I2DVKH} ⁶	100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0 ²	— 0.9 ³	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1 C_b$ ⁴	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1 C_b$ ⁴	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8541E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_b = capacitance of one bus line in pF.
- Guaranteed by design.

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[28:31]	T18, T19, T20, T21	O	OV _{DD}	5, 7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV _{DD}	—
LALE	V21	O	OV _{DD}	5, 8, 9
LBCTL	V20	O	OV _{DD}	9
LCKE	U23	O	OV _{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV _{DD}	—
LCS[0:4]	Y27, Y28, W27, W28, R27	O	OV _{DD}	—
LCS5/DMA_DREQ2	R28	I/O	OV _{DD}	1
LCS6/DMA_DACK2	P27	O	OV _{DD}	1
LCS7/DMA_DDONE2	P28	O	OV _{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV _{DD}	—
LGPL0/LSDA10	U19	O	OV _{DD}	5, 9
LGPL1/LSDWE	U22	O	OV _{DD}	5, 9
LGPL2/LOE/LSDRAS	V28	O	OV _{DD}	5, 8, 9
LGPL3/LSDCAS	V27	O	OV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	V23	I/O	OV _{DD}	21
LGPL5	V22	O	OV _{DD}	5, 9
LSYNC_IN	T27	I	OV _{DD}	—
LSYNC_OUT	T28	O	OV _{DD}	—
LWE[0:1]/LSDDQM[0:1]/LBS[0:1]	AB28, AB27	O	OV _{DD}	1, 5, 9
LWE[2:3]/LSDDQM[2:3]/LBS[2:3]	T23, P24	O	OV _{DD}	1, 5, 9
DMA				
DMA_DREQ[0:1]	H5, G4	I	OV _{DD}	—
DMA_DACK[0:1]	H6, G5	O	OV _{DD}	—
DMA_DDONE[0:1]	H7, G6	O	OV _{DD}	—
Programmable Interrupt Controller				
MCP	AG17	I	OV _{DD}	—
UDE	AG16	I	OV _{DD}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AF21	I	OV _{DD}	—
TDI	AG21	I	OV _{DD}	12
TDO	AF19	O	OV _{DD}	11
TMS	AF23	I	OV _{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV _{DD}	12
DFT				
LSSD_MODE	AG19	I	OV _{DD}	20
L1_TSTCLK	AB22	I	OV _{DD}	20
L2_TSTCLK	AG22	I	OV _{DD}	20
TEST_SEL0	AH20	I	OV _{DD}	3
TEST_SEL1	AG26	I	OV _{DD}	3
Thermal Management				
THERM0	AG2	—	—	14
THERM1	AH3	—	—	14
Power Management				
ASLEEP	AG18	—	—	9, 18
Power and Ground Signals				
AV _{DD1}	AH19	Power for e500 PLL (1.2 V)	AV _{DD1}	—
AV _{DD2}	AH18	Power for CCB PLL (1.2 V)	AV _{DD2}	—
AV _{DD3}	AH17	Power for CPM PLL (1.2 V)	AV _{DD3}	—
AV _{DD4}	AF28	Power for PCI1 PLL (1.2 V)	AV _{DD4}	—
AV _{DD5}	AE28	Power for PCI2 PLL (1.2 V)	AV _{DD5}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11, C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV _{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV _{DD}	—
LV _{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV _{DD}	—
MV _{REF}	N27	Reference Voltage Signal; DDR	MV _{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7, AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV _{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV _{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V _{DD}	13
SENSEVSS	K12	—	—	13
V _{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V _{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/O	OV _{DD}	—

15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

Table 47. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

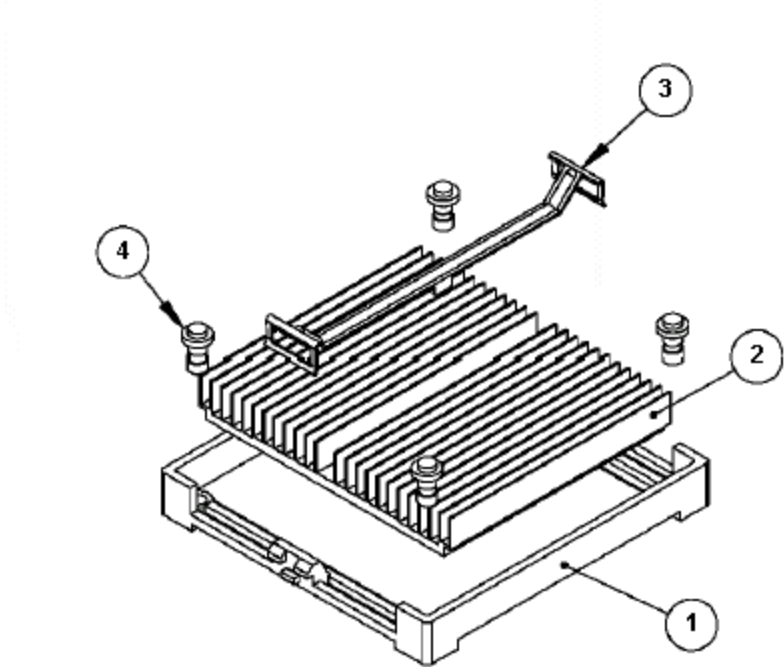
15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 48. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	17	25	33	42	67	83	100	111	133
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

Item No	QTY	MEI PN	Description
1	1	MFRAME-2000	HEATSINK FRAME
2	1	MSNK-1120	EXTRUDED HEATSINK
3	1	MCLIP-1013	CLIP
4	4	MPPINS-1000	FRAME ATTACHMENT PINS



Illustrative source provided by
Millennium Electronics (MEI)

Figure 48. Exploded Views (2) of a Heat Sink Attachment using a Plastic Force

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 52](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	07/2007	Inserted Figure 3 , ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Table 4 : Added footnote 2 about junction temperature. Table 4 : Added max. power values for 1000 MHz core frequency. Removed Figure 3 , “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Table 30 : Modified note to $t_{LBKSKEW}$ from 8 to 9 Table 30 : Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values. Table 30 : Added note 3 to $t_{LBKHOV1}$. Table 30 and Table 31 : Modified note 3. Table 31 : Added note 3 to $t_{LBKLOV1}$. Table 31 : Modified values for t_{LBKHK1} , $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$. Figure 21 : Changed Input Signals: LAD[0:31]/LDP[0:3]. Table 43 : Modified note for signal CLK_OUT. Table 43 : PCI1_CLK and PCI2_CLK changed from I/O to I. Table 52 : Added column for Encryption Acceleration.
3	8/29/2005	Table 4 : Modified max. power values. Table 43 : Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL.
2	8/2005	Previous revision's history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 31 is now listed as Table 31 . Table 7 : Added note 2. Table 14 : Modified min and max values for t_{DDKHMP}
1	6/2005	Table 27 : Changed LV_{dd} to OV_{dd} for the supply voltage Ethernet management interface. Table 4 : Modified footnote 4 and changed typical power for the 1000MHz core frequency. Table 31 : Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state.
0	6/2005	Initial Release.

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in [Section 19.1, “Nomenclature of Parts Fully Addressed by this Document.”](#)

19.1 Nomenclature of Parts Fully Addressed by this Document

[Table 52](#) provides the Freescale part numbering nomenclature for the MPC8541E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 52. Part Numbering Nomenclature

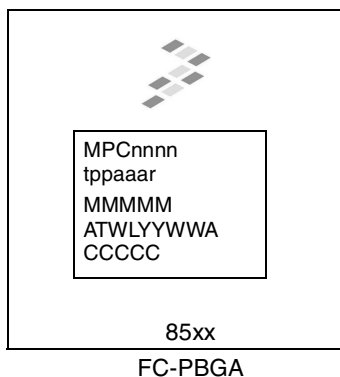
MPC	nnnn		<i>t</i>	<i>pp</i>	<i>aa</i>	<i>a</i>	<i>r</i>
Product Code	Part Identifier	Encryption Acceleration	Temperature Range ¹	Package ²	Processor Frequency ³	Platform Frequency	Revision Level ⁴
MPC	8541	Blank = not included E = included	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (lead free)	AJ = 533 MHz AK = 600 MHz AL = 667 MHz AP = 833 MHz AQ = 1000 MHz	D = 266 MHz E = 300 MHz F = 333 MHz	

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.
2. See [Section 14, “Package and Pin Listings,”](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. Contact you local Freescale field applications engineer (FAE).

19.2 Part Marking

Parts are marked as the example shown in [Figure 53](#).



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 53. Part Marking for FC-PBGA Device

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