Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8541pxapf

Table 5. Typical I/O Power Dissipation

Interface	Parameters	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	—
	CCB = 266 MHz	0.59	—	—	—	W	—
	CCB = 300 MHz	0.66	—	—	—	W	—
	CCB = 333 MHz	0.73	—	—	—	W	—
PCI I/O	64b, 66 MHz	—	0.14	—	—	W	—
	64b, 33 MHz	—	0.08	—	—	W	—
	32b, 66 MHz	—	0.07	—	—	W	Multiply by 2 if using two 32b ports
	32b, 33 MHz	—	0.04	—	—	W	
Local Bus I/O	32b, 167 MHz	—	0.30	—	—	W	—
	32b, 133 MHz	—	0.24	—	—	W	—
	32b, 83 MHz	—	0.16	—	—	W	—
	32b, 66 MHz	—	0.13	—	—	W	—
	32b, 33 MHz	—	0.07	—	—	W	—
TSEC I/O	MII	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	0.07	—	W	
	RGMII or RTBI	—	—	—	0.04	W	
CPM - FCC	MII	—	0.015	—	—	W	—
	RMII	—	0.013	—	—	W	—
	HDLC 16 Mbps	—	0.009	—	—	W	—

4.3 Real Time Clock Timing

Table 8 provides the real time clock (RTC) AC timing specifications.

Table 8. RTC AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	t_{RTCH}	2 x t_{CCB_CLK}	—	—	ns	—
RTC clock low time	t_{RTCL}	2 x t_{CCB_CLK}	—	—	ns	—

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8541E. Table 9 provides the RESET initialization AC timing specifications.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	512	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before HRESET negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8541E. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for more details.

Table 10 provides the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:
1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the SYSCLK × platform PLL ratio.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8541E.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8541E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	–10	10	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	5	µA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

Table 22. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF} [2,3]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

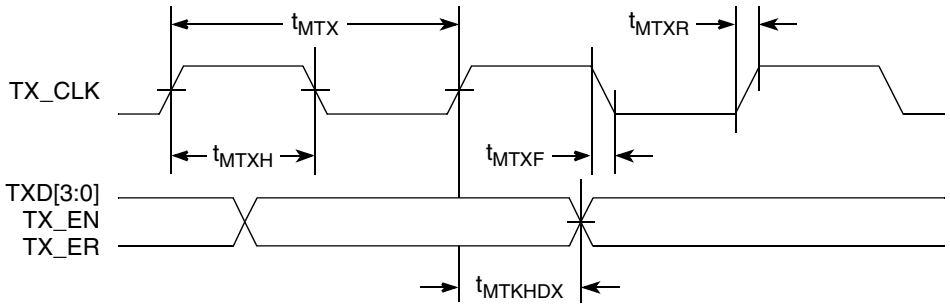


Figure 10. MII Transmit AC Timing Diagram

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8541E with the DLL enabled.

Table 30. Local Bus General Timing Parameters—DLL Enabled

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	—	ns	3, 4, 8
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5	—	ns	3, 4, 8
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV1}$	—	2.3	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			3.8		
Local bus clock to data valid for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV2}$	—	2.5	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			4.0		
Local bus clock to address valid for LAD	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV3}$	—	2.6	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			4.1		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOX1}$	0.7	—	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)		1.6			
Output hold from local bus clock for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOX2}$	0.7	—	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)		1.6			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOZ1}$	—	2.8	ns	5, 9
	$\overline{LWE[0:1]}$ = 11 (default)			4.2		

Table 31. Local Bus General Timing Parameters—DLL Bypassed (continued)

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to address valid for LAD	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOV3}$	—	0.8	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.3		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOX1}$	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)		–1.8			
Output hold from local bus clock for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOX2}$	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)		–1.8			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOZ1}$	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.4		
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOZ2}$	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.4		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 16 provides the AC test load for the local bus.

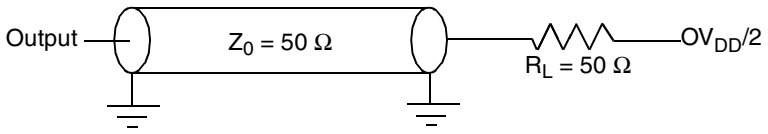


Figure 16. Local Bus C Test Load

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8541E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:
1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.
9. Guaranteed by characterization.
10. Guaranteed by design.

Figure 16 provides the AC test load for PCI.

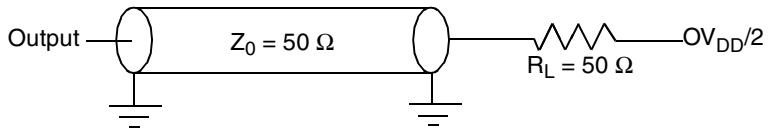


Figure 38. PCI AC Test Load

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_GNT[1:4]	AD18, AE18, AE19, AD19	O	OV_{DD}	5, 9
PCI2_IDSEL	AC22	I	OV_{DD}	—
PCI2_IRDY	AD20	I/O	OV_{DD}	2
PCI2_PERR	AC20	I/O	OV_{DD}	2
PCI2_REQ[0]	AD21	I/O	OV_{DD}	—
PCI2_REQ[1:4]	AE21, AD22, AE22, AC23	I	OV_{DD}	—
PCI2_SERR	AE20	I/O	OV_{DD}	2,4
PCI2_STOP	AC21	I/O	OV_{DD}	2
PCI2_TRDY	AC19	I/O	OV_{DD}	2
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	—
MBA[0:1]	B18, B19	O	GV_{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	—
MWE	D17	O	GV_{DD}	—
MRAS	F17	O	GV_{DD}	—
MCAS	J16	O	GV_{DD}	—
MCS[0:3]	H16, G16, J15, H15	O	GV_{DD}	—
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	—
MCK[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	—
MSYNC_IN	M28	I	GV_{DD}	22
MSYNC_OUT	N28	O	GV_{DD}	22
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	5, 9

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	5, 7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	5, 8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	—
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	P27	O	OV_{DD}	1
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	P28	O	OV_{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	—
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/$\overline{\text{LSDWE}}$	U22	O	OV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	V28	O	OV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LSDCAS}}$	V27	O	OV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	21
LGPL5	V22	O	OV_{DD}	5, 9
LSYNC_IN	T27	I	OV_{DD}	—
LSYNC_OUT	T28	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:1]/LSDDQM[0:1]/ $\overline{\text{LBS}}$[0:1]	AB28, AB27	O	OV_{DD}	1, 5, 9
$\overline{\text{LWE}}$[2:3]/LSDDQM[2:3]/ $\overline{\text{LBS}}$[2:3]	T23, P24	O	OV_{DD}	1, 5, 9
DMA				
$\overline{\text{DMA\_DREQ}}$[0:1]	H5, G4	I	OV_{DD}	—
$\overline{\text{DMA\_DACK}}$[0:1]	H6, G5	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0:1]	H7, G6	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP}}$	AG17	I	OV_{DD}	—
$\overline{\text{UDE}}$	AG16	I	OV_{DD}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV_{DD}	—
IRQ8	AB20	I	OV_{DD}	9
IRQ9/$\overline{\text{DMA\_DREQ3}}$	Y20	I	OV_{DD}	1
IRQ10/$\overline{\text{DMA\_DACK3}}$	AF26	I/O	OV_{DD}	1
IRQ11/$\overline{\text{DMA\_DDONE3}}$	AH24	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV_{DD}	5, 9
EC_MDIO	E1	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV_{DD}	—
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV_{DD}	9, 18
TSEC1_TX_EN	C8	O	LV_{DD}	11
TSEC1_TX_ER	B8	O	LV_{DD}	—
TSEC1_TX_CLK	C6	I	LV_{DD}	—
TSEC1_GTX_CLK	B6	O	LV_{DD}	—
TSEC1_CRS	C3	I	LV_{DD}	—
TSEC1_COL	G7	I	LV_{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV_{DD}	—
TSEC1_RX_DV	D2	I	LV_{DD}	—
TSEC1_RX_ER	E5	I	LV_{DD}	—
TSEC1_RX_CLK	D6	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV_{DD}	—
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV_{DD}	5, 9, 18
TSEC2_TX_EN	B11	O	LV_{DD}	11
TSEC2_TX_ER	D11	O	LV_{DD}	—
TSEC2_TX_CLK	D10	I	LV_{DD}	—
TSEC2_GTX_CLK	C10	O	LV_{DD}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	—
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7 AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—

15 Clocking

This section describes the PLL configuration of the MPC8541E. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 44 provides the clocking specifications for the processor core and Table 44 provides the clocking specifications for the memory bus.

Table 44. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency										Unit	Notes
	533 MHz		600 MHz		667 MHz		833 MHz		1000 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	533	400	600	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. 1000 MHz frequency supports only a 1.3 V core.

Table 45. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	533, 600, 667, 883, 1000 MHz			
	Min	Max		
Memory bus frequency	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. 1000 MHz frequency supports only a 1.3 V core.

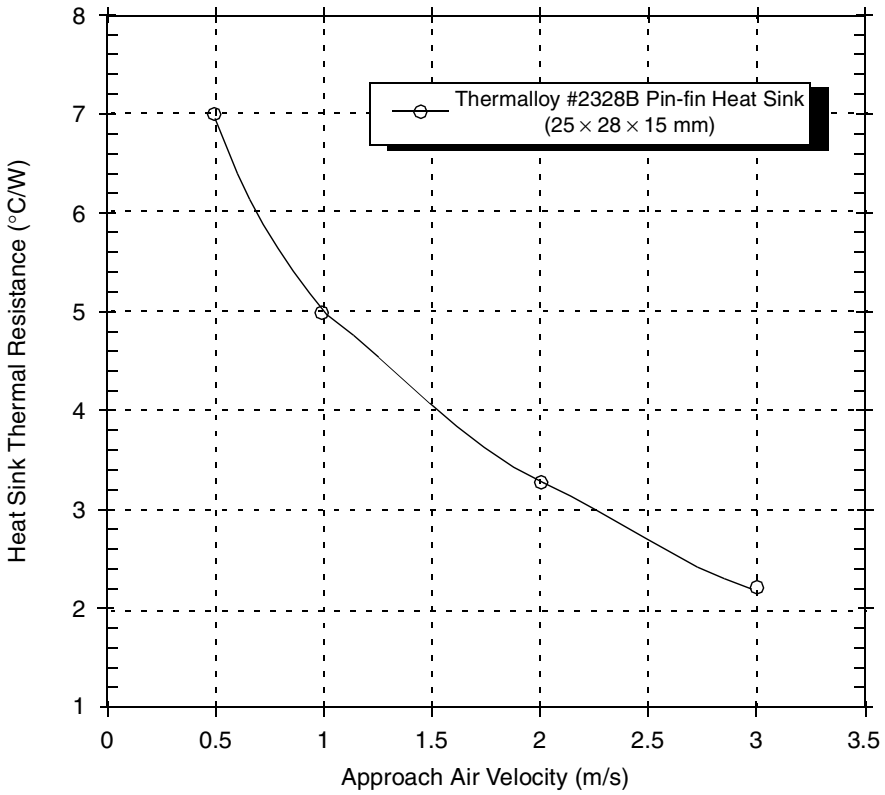


Figure 46. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

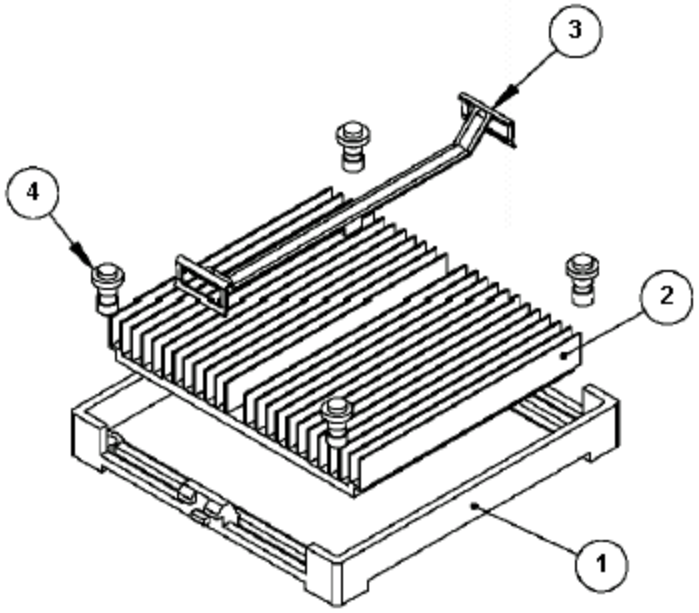
16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in Table 49 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 47 and Figure 48. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

Item No	QTY	MEI PN	Description
1	1	MFRAME-2000	HEATSINK FRAME
2	1	MSNK-1120	EXTRUDED HEATSINK
3	1	MCLIP-1013	CLIP
4	4	MPPINS-1000	FRAME ATTACHMENT PINS



Illustrative source provided by
Millennium Electronics (MEI)

Figure 48. Exploded Views (2) of a Heat Sink Attachment using a Plastic Force

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

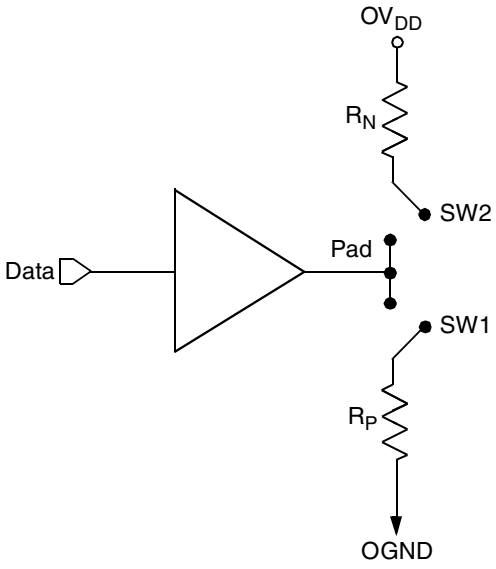


Figure 50. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 50 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 50. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	Ω
R_P	43 Target	25 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

17.6 Configuration Pin Multiplexing

The MPC8541E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The MPC8541E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 52. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 52. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	07/2007	Inserted Figure 3, ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Table 4: Added footnote 2 about junction temperature. Table 4: Added max. power values for 1000 MHz core frequency. Removed Figure 3, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Table 30: Modified note to $t_{LBKSKEW}$ from 8 to 9 Table 30: Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values. Table 30: Added note 3 to $t_{LBKHOV1}$. Table 30 and Table 31: Modified note 3. Table 31: Added note 3 to $t_{LBKLOV1}$. Table 31: Modified values for t_{LBKHKT}, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$. Figure 21: Changed Input Signals: LAD[0:31]/LDP[0:3]. Table 43: Modified note for signal CLK_OUT. Table 43: PCI1_CLK and PCI2_CLK changed from I/O to I. Table 52: Added column for Encryption Acceleration.
3	8/29/2005	Table 4: Modified max. power values. Table 43: Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL.
2	8/2005	Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 31 is now listed as Table 31. Table 7: Added note 2. Table 14: Modified min and max values for t_{DDKHMP}
1	6/2005	Table 27: Changed LV_{dd} to OV_{dd} for the supply voltage Ethernet management interface. Table 4: Modified footnote 4 and changed typical power for the 1000MHz core frequency. Table 31: Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state.
0	6/2005	Initial Release.

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, “Nomenclature of Parts Fully Addressed by this Document.”

19.1 Nomenclature of Parts Fully Addressed by this Document

Table 52 provides the Freescale part numbering nomenclature for the MPC8541E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 52. Part Numbering Nomenclature

MPC	*nnnn*		*t*	*pp*	*aa*	*a*	*r*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range[1]**	**Package [2]**	**Processor Frequency [3]**	**Platform Frequency**	**Revision Level[4]**
MPC	8541	Blank = not included E = included	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (lead free)	AJ = 533 MHz AK = 600 MHz AL = 667 MHz AP = 833 MHz AQ = 1000 MHZ	D = 266 MHz E = 300 MHz F = 333 MHz	

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.
2. See Section 14, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. Contact you local Freescale field applications engineer (FAE).

THIS PAGE INTENTIONALLY LEFT BLANK