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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	•
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8541pxaqf

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1 Overview

The following section provides a high-level overview of the MPC8541E features. Figure 1 shows the major functional units within the MPC8541E.



Figure 1. MPC8541E Block Diagram

1.1 Key Features

The following lists an overview of the MPC8541E feature set.

- Embedded e500 Book E-compatible core
 - High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
 - Dual-issue superscalar, 7-stage pipeline design
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
 - Lockable L1 caches—entire cache or on a per-line basis
 - Separate locking for instructions and data
 - Single-precision floating-point operations
 - Memory management unit especially designed for embedded applications
 - Enhanced hardware and software debug support
 - Dynamic power management
 - Performance monitor facility



- Selectable hardware-enforced coherency
- Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
 - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
 - Supports power save modes: doze, nap, and sleep
 - Employs dynamic power management
 - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1TM-compatible, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8541E. The MPC8541E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.



6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8541E.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8541E.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	—
Output leakage current	I _{oz}	-10	10	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	—	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	—
MV _{REF} input leakage current	I _{VREF}	_	5	μA	_

Table 11. DDR SDRAM DC Electrical Characteristics

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

- 2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
- 4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.



Figure 4 shows the DDR SDRAM output timing for address skew with respect to any MCK.



Figure 4. Timing Diagram for $t_{\mbox{AOSKEW}}$ Measurement

Figure 5 shows the DDR SDRAM output timing diagram for the source synchronous mode.



Figure 5. DDR SDRAM Output Timing Diagram for Source Synchronous Mode



8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

Table 22. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX} 2	—	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	—	40	—	ns
TX_CLK duty cycle	t _{MTXH/} t _{MTX}	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t _{MTXR} , t _{MTXF} ^{2,3}	1.0	_	4.0	ns

Notes:

 The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

- 2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- 3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.



Figure 10. MII Transmit AC Timing Diagram



Ethernet: Three-Speed, MII Management

8.2.3.2 MII Receive AC Timing Specifications

Table 23 provides the MII receive AC timing specifications.

Table 23. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period 10 Mbps	t _{MRX} 2	_	400	_	ns
RX_CLK clock period 100 Mbps	t _{MRX}		40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t _{MRXR} , t _{MRXF} ^{2,3}	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.

3.Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.



Figure 11. MII Receive AC Timing Diagram



Local Bus

Figure 15 shows the MII management AC timing diagram.



Figure 15. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8541E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	V _{OUT} ≤ V _{OL} (max)	-0.3	0.8	V
Input current	I _{IN}	V_{IN} ¹ = 0 V or V_{IN} = V_{DD}	—	±5	μA
High-level output voltage	V _{OH}	$OV_{DD} = min,$ $I_{OH} = -2mA$	OV _{DD} -0.2	_	V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 2mA	—	0.2	V

Table 29. Local Bus DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.



Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to address valid for LAD	LWE[0:1] = 00	t _{LBKLOV3}	_	0.8	ns	3
	LWE[0:1] = 11 (default)			2.3		
Output hold from local bus clock (except	LWE[0:1] = 00	t _{LBKLOX1}	-2.7	_	ns	3
LAD/LDP and LALE)	LWE[0:1] = 11 (default)		-1.8			
Output hold from local bus clock for LAD/LDP	LWE[0:1] = 00	t _{LBKLOX2}	-2.7	_	ns	3
	LWE[0:1] = 11 (default)		-1.8			
Local bus clock to output high Impedance	<u>LWE[0:1]</u> = 00	t _{LBKLOZ1}	_	1.0	ns	5
(except LAD/LDP and LALE)	LWE[0:1] = 11 (default)			2.4		
Local bus clock to output high impedance for	<u>LWE[0:1]</u> = 00	t _{LBKLOZ2}		1.0	ns	5
	LWE[0:1] = 11 (default)			2.4		

Table 31. Local Bus General Timing Parameters—DLL Bypassed (continued)

Notes:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to LSYNC_IN for DLL enabled mode.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins LWE[0:1].
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at OV_{DD}/2.
- 8. Guaranteed by characterization.
- 9. Guaranteed by design.

Figure 16 provides the AC test load for the local bus.



Figure 16. Local Bus C Test Load



Table 33. CPM Input AC Timing Specifications ¹ (continued)

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{FIIVKH} symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock t_{FCC} (K) going to the high (H) state or setup time.
- 3. PIO and TIMER inputs and outputs are asynchronous to SYSCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

Characteristic	Symbol ²	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	t _{FIKHOX}	1	5.5	ns
FCC outputs—external clock (NMSI) delay	t _{FEKHOX}	2	8	ns
SPI outputs—internal clock (NMSI) delay	t _{NIKHOX}	0.5	10	ns
SPI outputs—external clock (NMSI) delay	t _{NEKHOX}	2	8	ns
PIO outputs delay	t _{PIKHOX}	1	11	ns

Table 34. CPM Output AC Timing Specifications ¹

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{FIKHOX} symbolizes the FCC inputs internal timing (FI) for the time t_{FCC} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>

Figure 23 provides the AC test load for the CPM.



Figure 23. CPM AC Test Load

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СРМ



Figure 35 provides the test access port timing diagram.



Figure 35. Test Access Port Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8541E.

12.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I^2C interface of the MPC8541E.

Table 39. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	$0.7 imes OV_{DD}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3 imes OV_{DD}$	V	
Low level output voltage	V _{OL}	0	$0.2 \times \text{OV}_{\text{DD}}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t _{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 \times OV_{DD} and 0.9 \times OV_{DD}(max)	I	-10	10	μΑ	4
Capacitance for each I/O pin	CI	—	10	pF	—

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the MPC8555E PowerQUICC[™] III Integrated Communications Processor Reference Manual for information on the digital filter used.

4. I/O pins obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.



Table 40 provides the AC timing parameters for the I²C interface of the MPC8541E.

Table 40. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol ¹	Min	Мах	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL} 6	1.3	_	μs
High period of the SCL clock	t _{I2CH} 6	0.6	_	μs
Setup time for a repeated START condition	t _{I2SVKH} ⁶	0.6	_	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL} 6	0.6	_	μs
Data setup time	t _{I2DVKH} 6	100	_	ns
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	0 ²	0.9 ³	μs
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns
Set-up time for STOP condition	t _{I2PVKH}	0.6	_	μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	_	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V

Notes:

- 1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the low (L) state or hold time. Also, t_{12PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- MPC8541E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.
- 5. Guaranteed by design.



14.2 Mechanical Dimensions of the FC-PBGA

Figure 41 the mechanical dimensions and bottom surface nomenclature of the MPC8541E 783 FC-PBGA package.



Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
- 7. The socket lid must always be oriented to A1.

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_GNT[1:4]	AD18, AE18, AE19, AD19	0	OV _{DD}	5, 9
PCI2_IDSEL	AC22	I	OV _{DD}	—
PCI2_IRDY	AD20	I/O	OV _{DD}	2
PCI2_PERR	AC20	I/O	OV _{DD}	2
PCI2_REQ[0]	AD21	I/O	OV _{DD}	—
PCI2_REQ[1:4]	AE21, AD22, AE22, AC23	I	OV _{DD}	—
PCI2_SERR	AE20	I/O	OV _{DD}	2,4
PCI2_STOP	AC21	I/O	OV _{DD}	2
PCI2_TRDY	AC19	I/O	OV _{DD}	2
	DDR SDRAM Memory Interface			1
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV _{DD}	
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV _{DD}	
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	0	GV _{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV _{DD}	—
MBA[0:1]	B18, B19	0	GV _{DD}	
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	0	GV _{DD}	_
MWE	D17	0	GV _{DD}	—
MRAS	F17	0	GV _{DD}	—
MCAS	J16	0	GV _{DD}	—
MCS[0:3]	H16, G16, J15, H15	0	GV _{DD}	—
MCKE[0:1]	E26, E28	0	GV _{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	0	GV _{DD}	—
MCK[0:5]	F20, G27, B15, E20, F27, L14	0	GV _{DD}	—
MSYNC_IN	M28	I	GV _{DD}	22
MSYNC_OUT	N28	0	GV _{DD}	22
	Local Bus Controller Interface			
LA[27]	U18	0	OV _{DD}	5, 9



Clocking

15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

Table 47. e500 Core to CCB Ratio

15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 48. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	17	25	33	42	67	83	100	111	133
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333		•	<u>.</u>
5				208	333		2		
6			200	250		<u>-</u>			
8		200	267	333					
9		225	300		4				
10		250	333	1					
12	200	300		-					
16	267		-						





16 Thermal

This section describes the thermal specifications of the MPC8541E.

16.1 Thermal Characteristics

Table 49 provides the package thermal characteristics for the MPC8541E.

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{ extsf{ heta}JMA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1.0 m/s) on four layer board (2s2p)	$R_{ extsf{ heta}JMA}$	14	°C/W	1, 2
Junction-to-ambient (@400 ft/min or 2.0 m/s) on four layer board (2s2p)	$R_{ extsf{ heta}JMA}$	13	°C/W	1, 2
Junction-to-board thermal	$R_{ extsf{ heta}JB}$	10	°C/W	3
Junction-to-case thermal	R _{θJC}	0.96	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance

- 2. Per JEDEC JESD51-6 with the board horizontal.
- 3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 42. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.



FC-PBGA Package Heat Sink Clip Thermal Interface Material

Printed-Circuit Board

Figure 42. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8541E. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers [™] P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102



Chanhassen, MN 55317 Internet: www.bergquistcompany.com Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com

888-246-9050

16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

 T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

 T_R is the air temperature rise within the computer cabinet

 θ_{IC} is the junction-to-case thermal resistance

 θ_{INT} is the adhesive or interface material thermal resistance

 θ_{SA} is the heat sink base-to-ambient thermal resistance

 P_D is the power dissipated by the device. See Table 4 and Table 5.

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. For the purposes of this example, the θ_{JC} value given in Table 49 that includes the thermal grease interface and is documented in note 4 is used. If a thermal pad is used, θ_{INT} must be added.

Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package $\theta_{JC} = 0.96$, and a power consumption (P_D) of 8.0 W, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30^{\circ}C + 5^{\circ}C + (0.96^{\circ}C/W + \theta_{SA}) \times 8.0 W$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 46.

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3°C/W, thus

 $T_{\rm J} = 30^{\circ}\text{C} + 5^{\circ}\text{C} + (0.96^{\circ}\text{C/W} + 3.3^{\circ}\text{C/W}) \times 8.0 \text{ W},$

resulting in a die-junction temperature of approximately 69°C which is well within the maximum operating temperature of the component.







Figure 46. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in Table 49 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 47 and Figure 48. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.



Device Nomenclature

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, "Nomenclature of Parts Fully Addressed by this Document."

19.1 Nomenclature of Parts Fully Addressed by this Document

Table 52 provides the Freescale part numbering nomenclature for the MPC8541E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

MPC	nnnn		t	рр	aa	а	r
Product Code	Part Identifier	Encryption Acceleration	Temperature Range ¹	Package ²	Processor Frequency ³	Platform Frequency	Revision Level ⁴
MPC	8541	Blank = not included E = included	Blank = 0 to 105°C C = -40 to 105°C	PX = FC-PBGA VT = FC-PBGA (lead free)	AJ = 533 MHz AK = 600 MHz AL = 667 MHz AP = 833 MHz AQ = 1000 MHZ	D = 266 MHz E = 300 MHz F = 333 MHz	

Table 52. Part Numbering Nomenclature

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.

2. See Section 14, "Package and Pin Listings," for more information on available package types.

 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

4. Contact you local Freescale field applications engineer (FAE).



Device Nomenclature

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