Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8541vtajd

  - SRAM operation supports relocation and is byte-accessible
  - Cache mode supports instruction caching, data caching, or both
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
  - Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
  - Supports locking the entire cache or selected lines
    - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately
  - Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI
    - Four inbound windows
    - Four outbound windows plus default translation for PCI
- DDR memory controller
  - Programmable timing supporting first generation DDR SDRAM
  - 64-bit data interface, up to MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Sleep mode support for self refresh DDR SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller

  - Selectable hardware-enforced coherency
  - Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power save modes: doze, nap, and sleep
  - Employs dynamic power management
  - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8541E. The MPC8541E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

4 Clock Timing

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8541E.

Table 6. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are ±1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8541E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise time	t_{G125R}	—	—	1.0	ns	1
EC_GTX_CLK125 fall time	t_{G125F}	—	—	1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

Figure 6 provides the AC test load for the DDR bus.

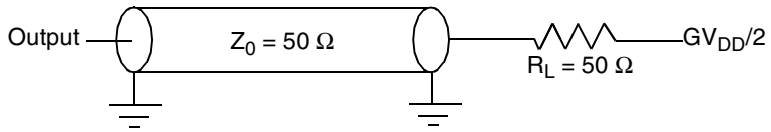


Figure 6. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:
1. Data input threshold measurement point.
2. Data output measurement point.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8541E.

7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8541E.

Table 16. DUART DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR}, t_{TTXF} [2,3]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

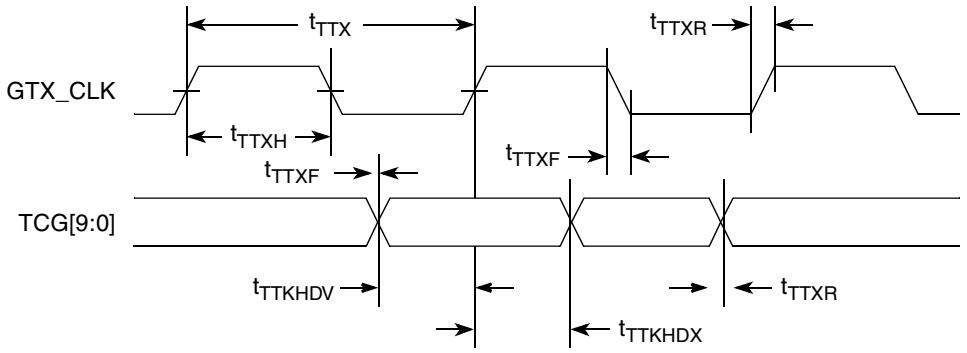


Figure 12. TBI Transmit AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

Table 26. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration [3]	t_{RGT}[6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT}[6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT}[6]	40	50	60	%
Rise and fall times	t_{RGTR}[6,7], t_{RGTF}[6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device functions with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 and 2.0 V voltage levels.

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8541E with the DLL enabled.

Table 30. Local Bus General Timing Parameters—DLL Enabled

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	—	ns	3, 4, 8
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5	—	ns	3, 4, 8
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV1}$	—	2.3	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			3.8		
Local bus clock to data valid for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV2}$	—	2.5	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			4.0		
Local bus clock to address valid for LAD	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOV3}$	—	2.6	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)			4.1		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOX1}$	0.7	—	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)		1.6			
Output hold from local bus clock for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOX2}$	0.7	—	ns	3, 8
	$\overline{LWE[0:1]}$ = 11 (default)		1.6			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOZ1}$	—	2.8	ns	5, 9
	$\overline{LWE[0:1]}$ = 11 (default)			4.2		

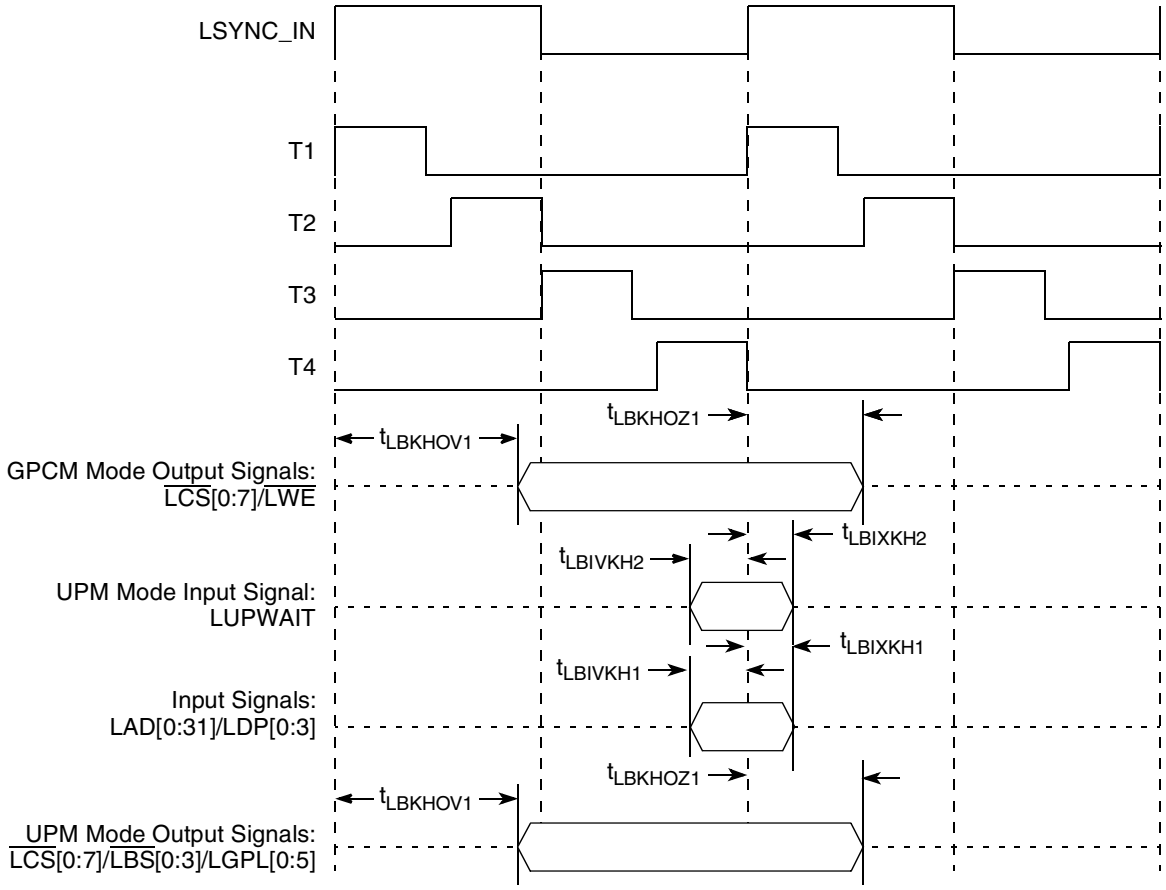


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

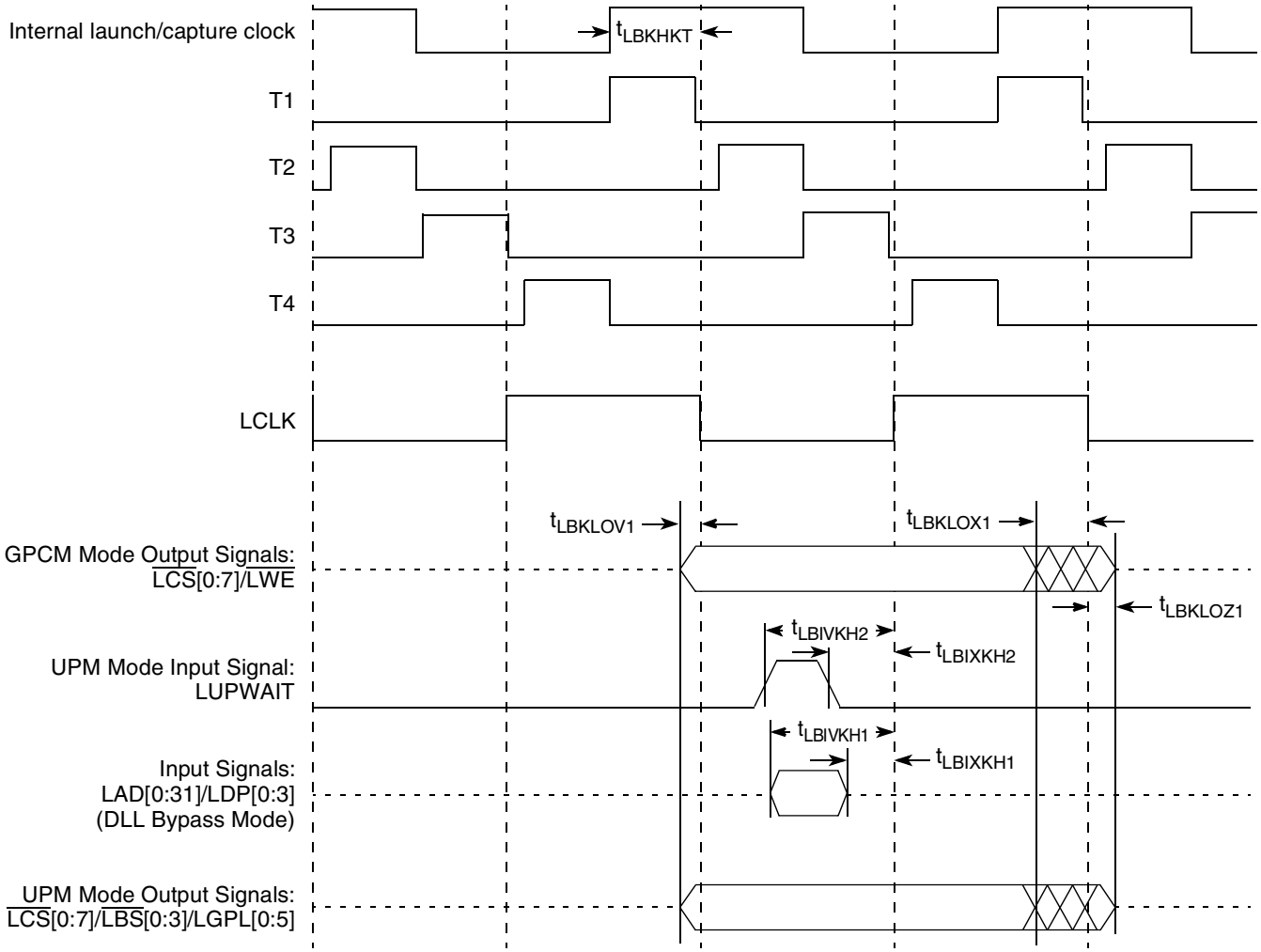
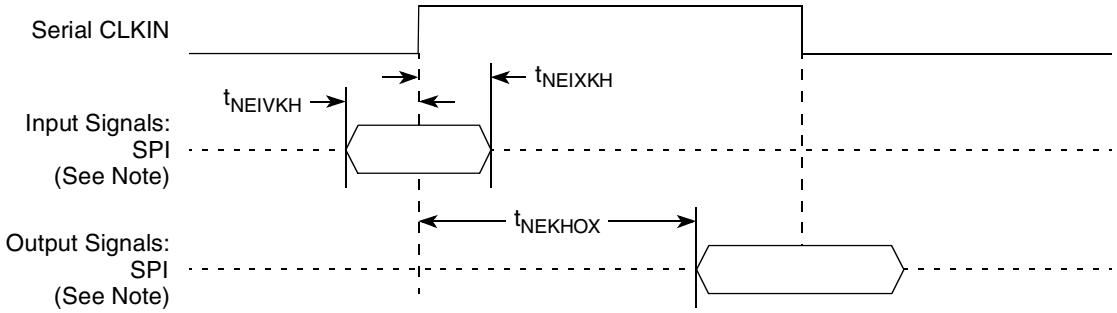


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

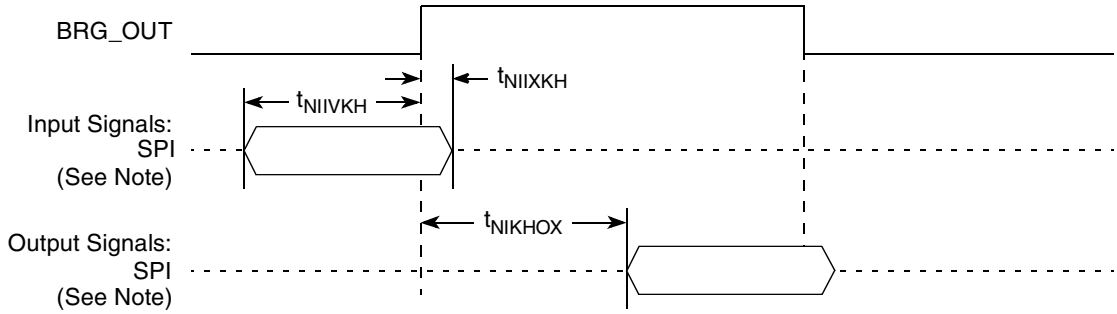
Figure 27 shows the SPI external clock.



Note: The clock edge is selectable on SPI.

Figure 27. SPI AC Timing External Clock Diagram

Figure 28 shows the SPI internal clock.



Note: The clock edge is selectable on SPI.

Figure 28. SPI AC Timing Internal Clock Diagram

NOTE

[1] SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

[2] SPI AC timings refer always to SPICLK.

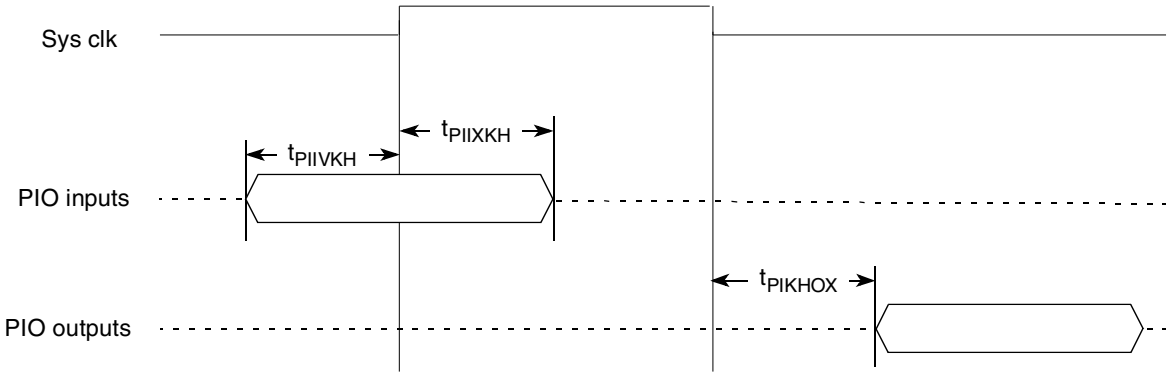


Figure 29. PIO Signal Diagram

The following two tables are examples of I2C AC parameters at I2C clock value of 100k and 400k respectively.

Table 36. CPM I2C Timing (f_{SCL}=100 kHz)

Characteristic	Expression	Frequency = 100 kHz		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	—	100	kHz
SCL clock frequency (master)	f_{SCL}	—	100	kHz
Bus free time between transmissions	t_{SDHDL}	4.7	—	µs
Low period of SCL	t_{SCLCH}	4.7	—	µs
High period of SCL	t_{SCHCL}	4	—	µs
Start condition setup time	t_{SCHDL}	2	—	µs
Start condition hold time	t_{SDLCL}	3	—	µs
Data hold time	t_{SCLDX}	2	—	µs
Data setup time	t_{SDVCH}	3	—	µs
SDA/SCL rise time	t_{SRISE}	—	1	µs
SDA/SCL fall time (master)	t_{SFALL}	—	303	ns
Stop condition setup time	t_{SCHDH}	2	—	µs

Table 37. CPM I2C Timing (f_{SCL}=400 kHz)

Characteristic	Expression	Frequency = 400 kHz		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	—	400	kHz
SCL clock frequency (master)	f_{SCL}	—	400	kHz
Bus free time between transmissions	t_{SDHDL}	1.2	—	µs
Low period of SCL	t_{SCLCH}	1.2	—	µs
High period of SCL	t_{SCHCL}	1	—	µs
Start condition setup time	t_{SCHDL}	420	—	ns
Start condition hold time	t_{SDLCL}	630	—	ns
Data hold time	t_{SCLDX}	420	—	ns
Data setup time	t_{SDVCH}	630	—	ns
SDA/SCL rise time	t_{SRISE}	—	250	ns
SDA/SCL fall time	t_{SFALL}	—	75	ns
Stop condition setup time	t_{SCHDH}	420	—	ns

Figure 31 provides the AC test load for TDO and the boundary-scan outputs of the MPC8541E.

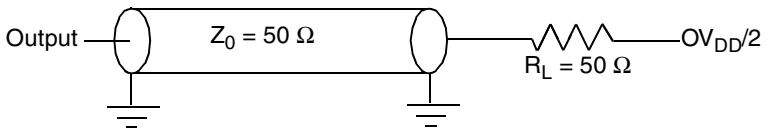


Figure 31. AC Test Load for the JTAG Interface

Figure 32 provides the JTAG clock input timing diagram.

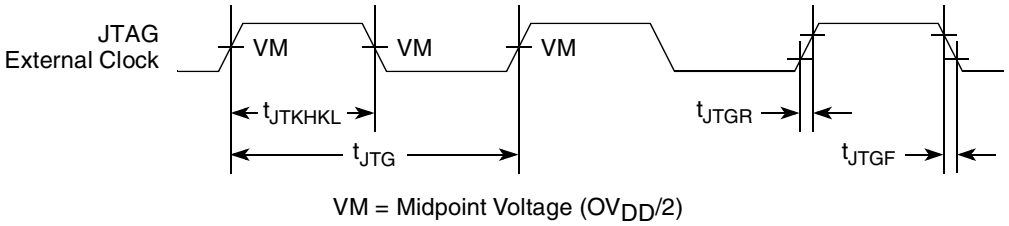


Figure 32. JTAG Clock Input Timing Diagram

Figure 33 provides the $\overline{\text{TRST}}$ timing diagram.

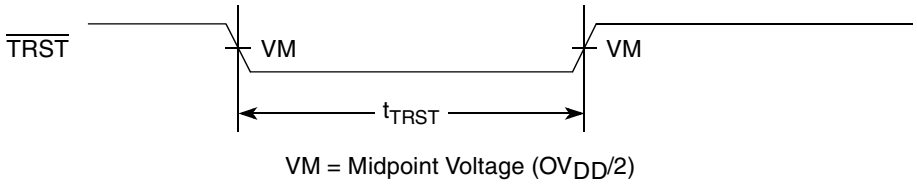


Figure 33. $\overline{\text{TRST}}$ Timing Diagram

Figure 34 provides the boundary-scan timing diagram.

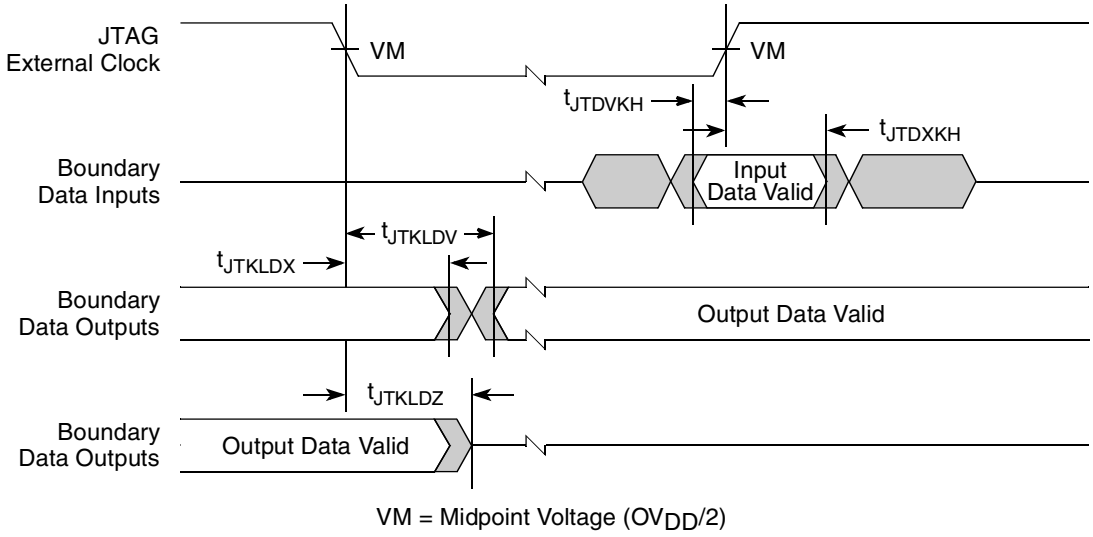


Figure 34. Boundary-Scan Timing Diagram

Figure 16 provides the AC test load for the I^2C.

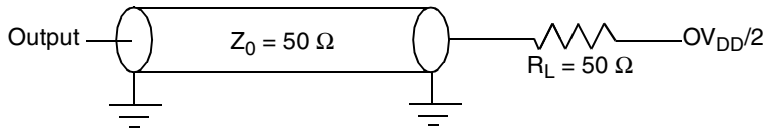


Figure 36. I^2C AC Test Load

Figure 37 shows the AC timing diagram for the I^2C bus.

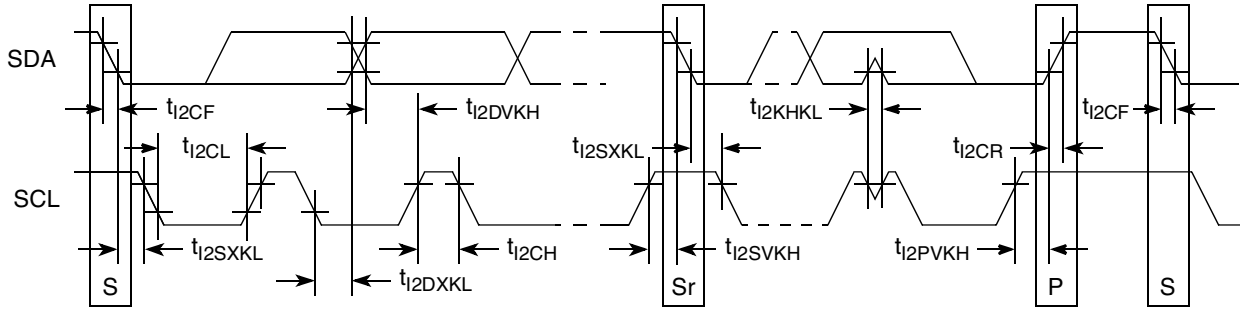


Figure 37. I^2C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8541E.

13.1 PCI DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI interface of the MPC8541E.

Table 41. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [2] = 0 V or $V_{IN} = V_{DD}$	—	±5	µA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

14.2 Mechanical Dimensions of the FC-PBGA

Figure 41 the mechanical dimensions and bottom surface nomenclature of the MPC8541E 783 FC-PBGA package.

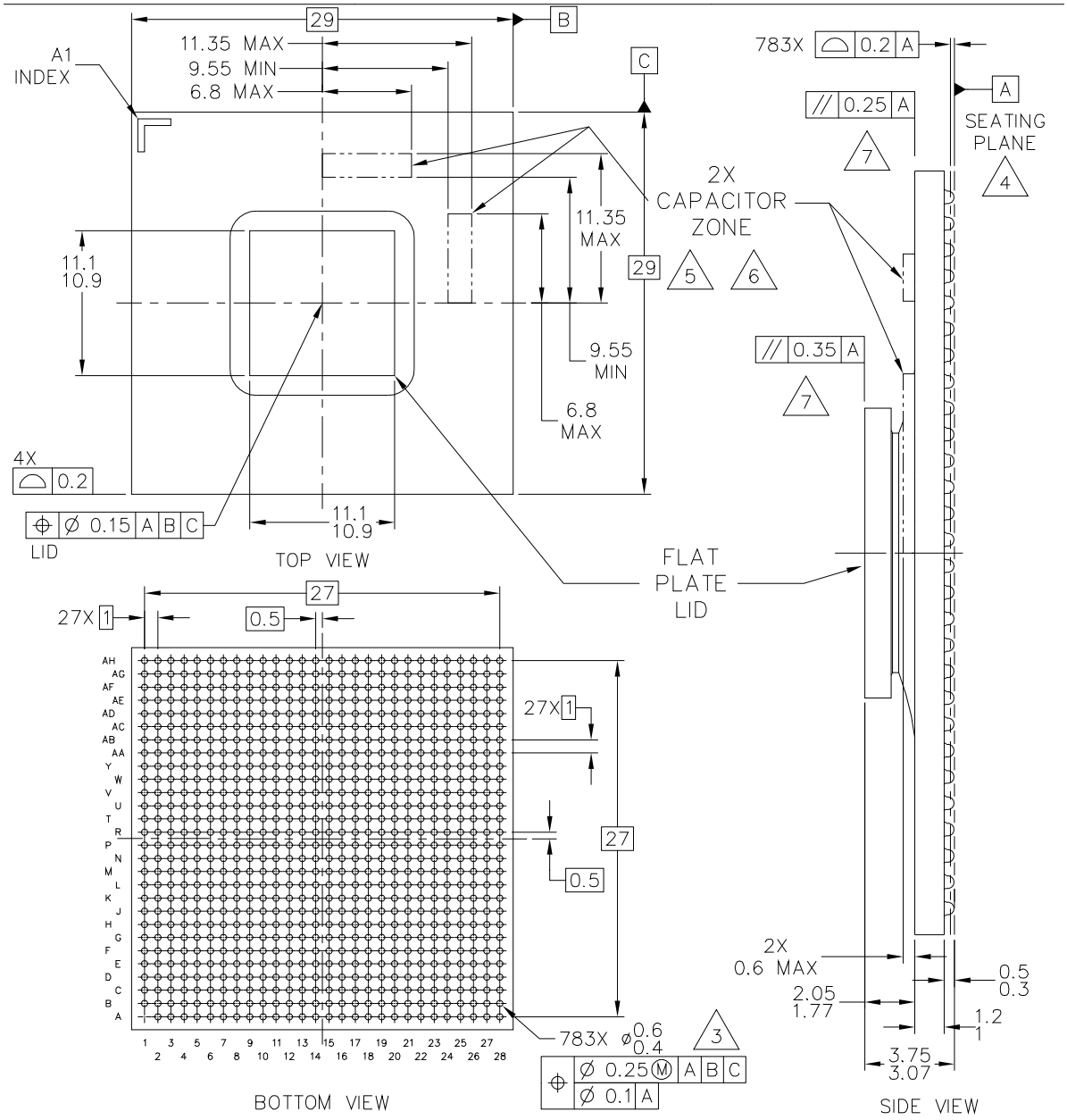


Figure 41. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA

Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

16 Thermal

This section describes the thermal specifications of the MPC8541E.

16.1 Thermal Characteristics

Table 49 provides the package thermal characteristics for the MPC8541E.

Table 49. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@400 ft/min or 2.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	$R_{\theta JC}$	0.96	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51–6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 42. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

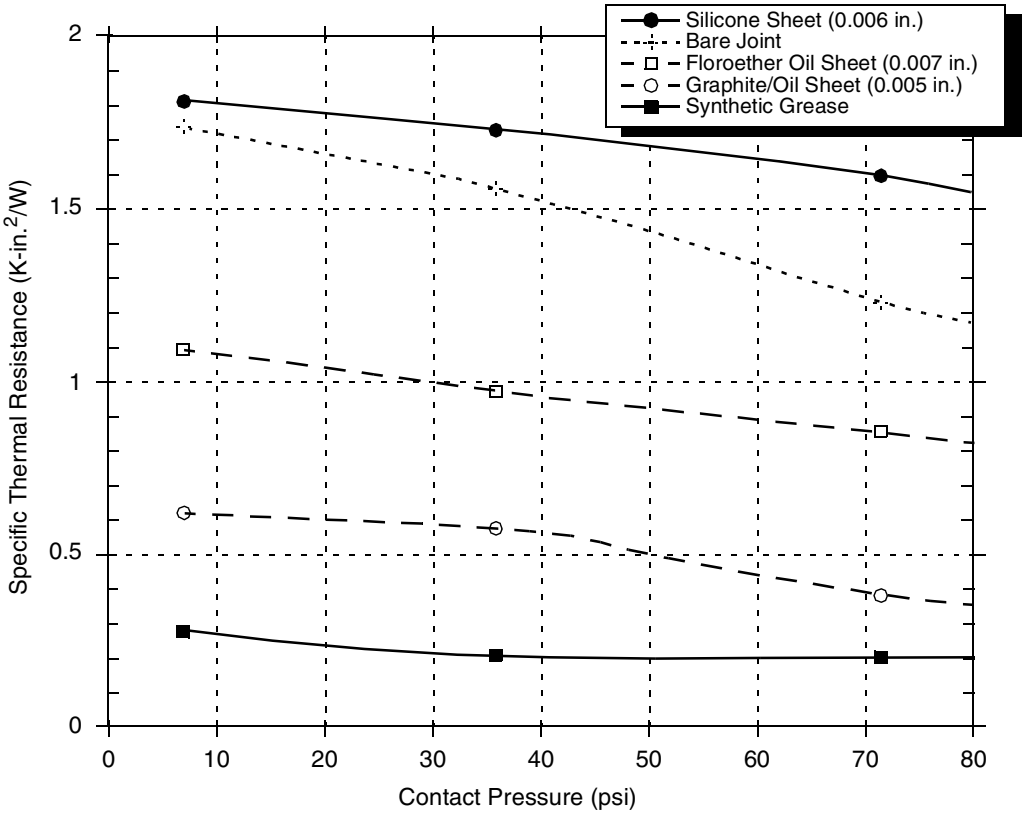


Figure 45. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St.	800-347-4572

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

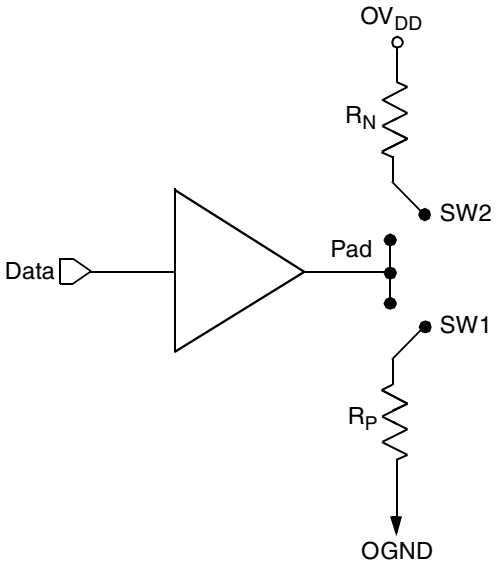


Figure 50. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 50 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 50. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	Ω
R_P	43 Target	25 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	07/2007	Inserted Figure 3, ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Table 4: Added footnote 2 about junction temperature. Table 4: Added max. power values for 1000 MHz core frequency. Removed Figure 3, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Table 30: Modified note to $t_{LBKSKEW}$ from 8 to 9 Table 30: Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values. Table 30: Added note 3 to $t_{LBKHOV1}$. Table 30 and Table 31: Modified note 3. Table 31: Added note 3 to $t_{LBKLOV1}$. Table 31: Modified values for t_{LBKHKT}, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$. Figure 21: Changed Input Signals: LAD[0:31]/LDP[0:3]. Table 43: Modified note for signal CLK_OUT. Table 43: PCI1_CLK and PCI2_CLK changed from I/O to I. Table 52: Added column for Encryption Acceleration.
3	8/29/2005	Table 4: Modified max. power values. Table 43: Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL.
2	8/2005	Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 31 is now listed as Table 31. Table 7: Added note 2. Table 14: Modified min and max values for t_{DDKHMP}
1	6/2005	Table 27: Changed LV_{dd} to OV_{dd} for the supply voltage Ethernet management interface. Table 4: Modified footnote 4 and changed typical power for the 1000MHz core frequency. Table 31: Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state.
0	6/2005	Initial Release.

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, “Nomenclature of Parts Fully Addressed by this Document.”

19.1 Nomenclature of Parts Fully Addressed by this Document

Table 52 provides the Freescale part numbering nomenclature for the MPC8541E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 52. Part Numbering Nomenclature

MPC	*nnnn*		*t*	*pp*	*aa*	*a*	*r*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range[1]**	**Package [2]**	**Processor Frequency [3]**	**Platform Frequency**	**Revision Level[4]**
MPC	8541	Blank = not included E = included	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (lead free)	AJ = 533 MHz AK = 600 MHz AL = 667 MHz AP = 833 MHz AQ = 1000 MHZ	D = 266 MHz E = 300 MHz F = 333 MHz	

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.
2. See Section 14, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. Contact you local Freescale field applications engineer (FAE).

THIS PAGE INTENTIONALLY LEFT BLANK