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Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8541vtapf

1 Overview

The following section provides a high-level overview of the MPC8541E features. Figure 1 shows the major functional units within the MPC8541E.

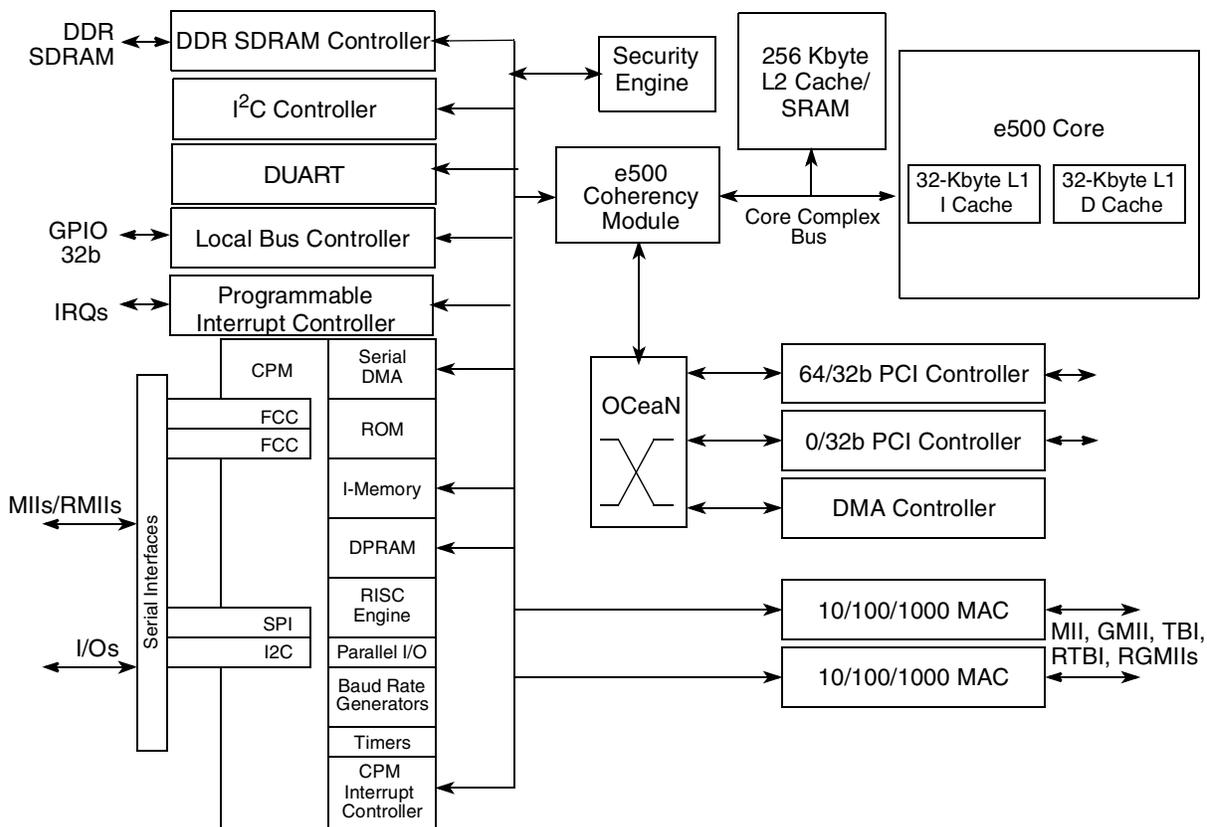


Figure 1. MPC8541E Block Diagram

1.1 Key Features

The following lists an overview of the MPC8541E feature set.

- Embedded e500 Book E-compatible core
 - High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
 - Dual-issue superscalar, 7-stage pipeline design
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
 - Lockable L1 caches—entire cache or on a per-line basis
 - Separate locking for instructions and data
 - Single-precision floating-point operations
 - Memory management unit especially designed for embedded applications
 - Enhanced hardware and software debug support
 - Dynamic power management
 - Performance monitor facility

- 1000 Mbps IEEE 802.3z TBI
- 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking
- OCeaN switch fabric
 - Three-port crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no-snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI Controllers
 - PCI 2.2 compatible
 - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
 - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes
 - PCI 3.3-V compatible

8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

Table 21. GMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} ^{2,3}	—	—	1.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

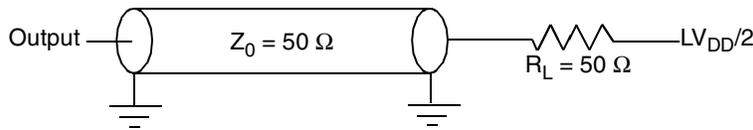


Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

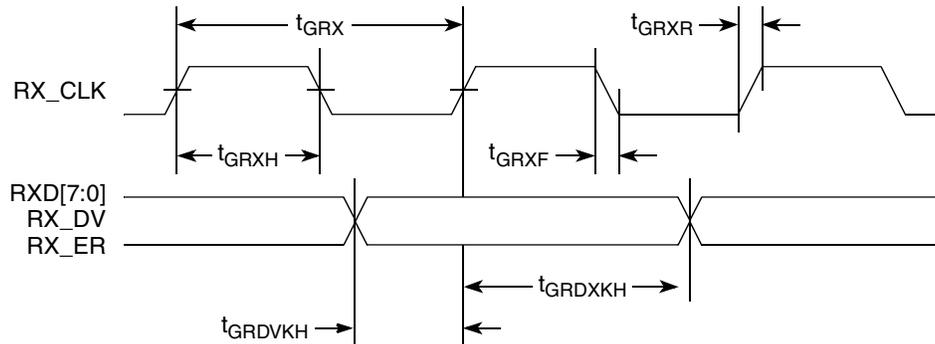


Figure 9. GMII Receive AC Timing Diagram

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.

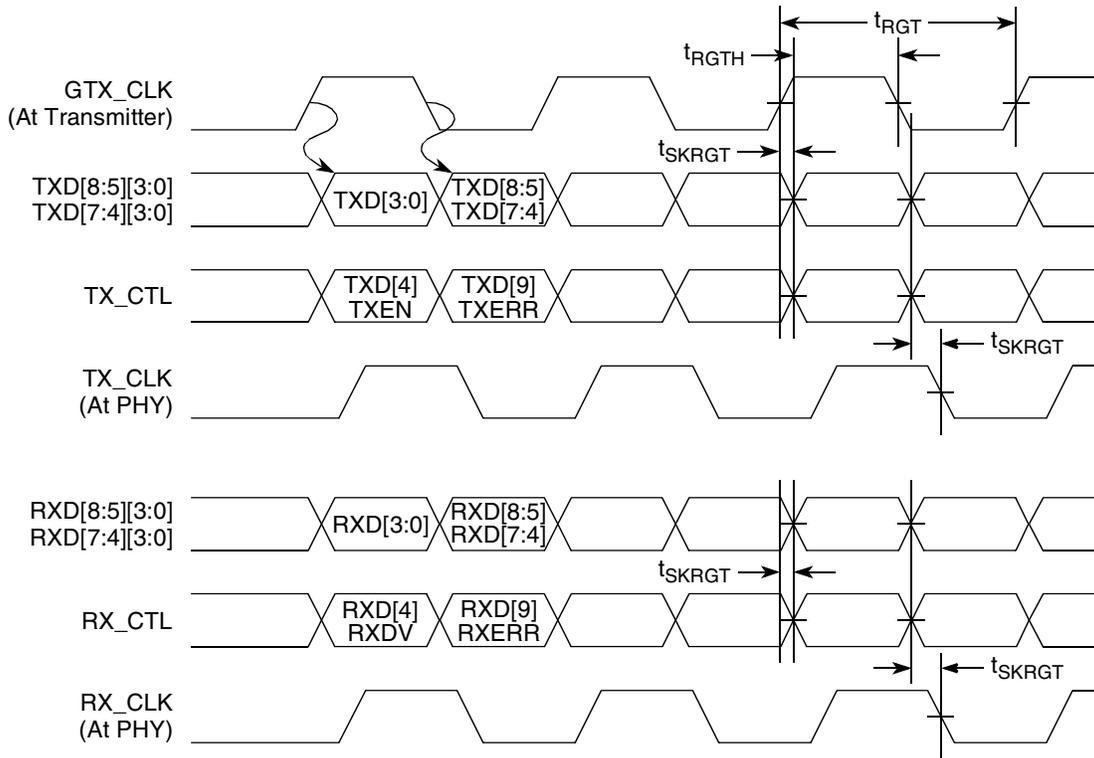


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, “Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	V_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	$V_{DD} = \text{Min}$	2.10	$V_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	$V_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—		1.70	—	V
Input low voltage	V_{IL}	—		—	0.90	V

Figure 15 shows the MII management AC timing diagram.

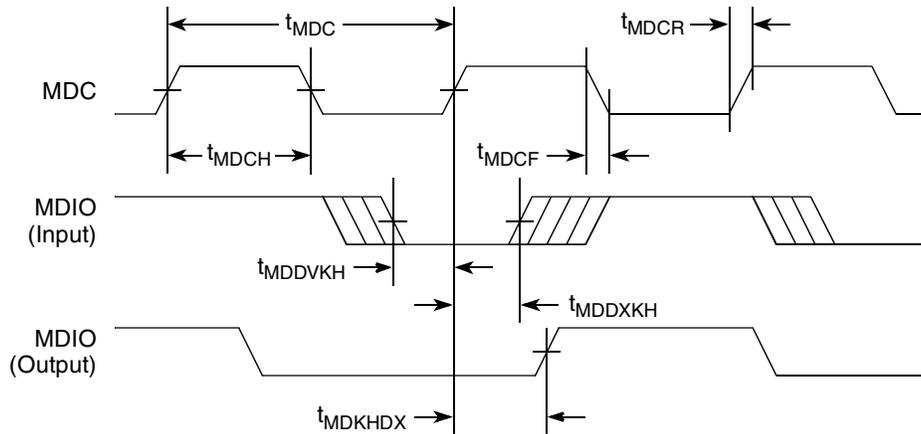


Figure 15. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8541E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} (\text{min})$ or $V_{OUT} \leq V_{OL} (\text{max})$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V}$ or $V_{IN} = V_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min}$, $I_{OH} = -2\text{mA}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min}$, $I_{OL} = 2\text{mA}$	—	0.2	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 17 to Figure 22 show the local bus signals.

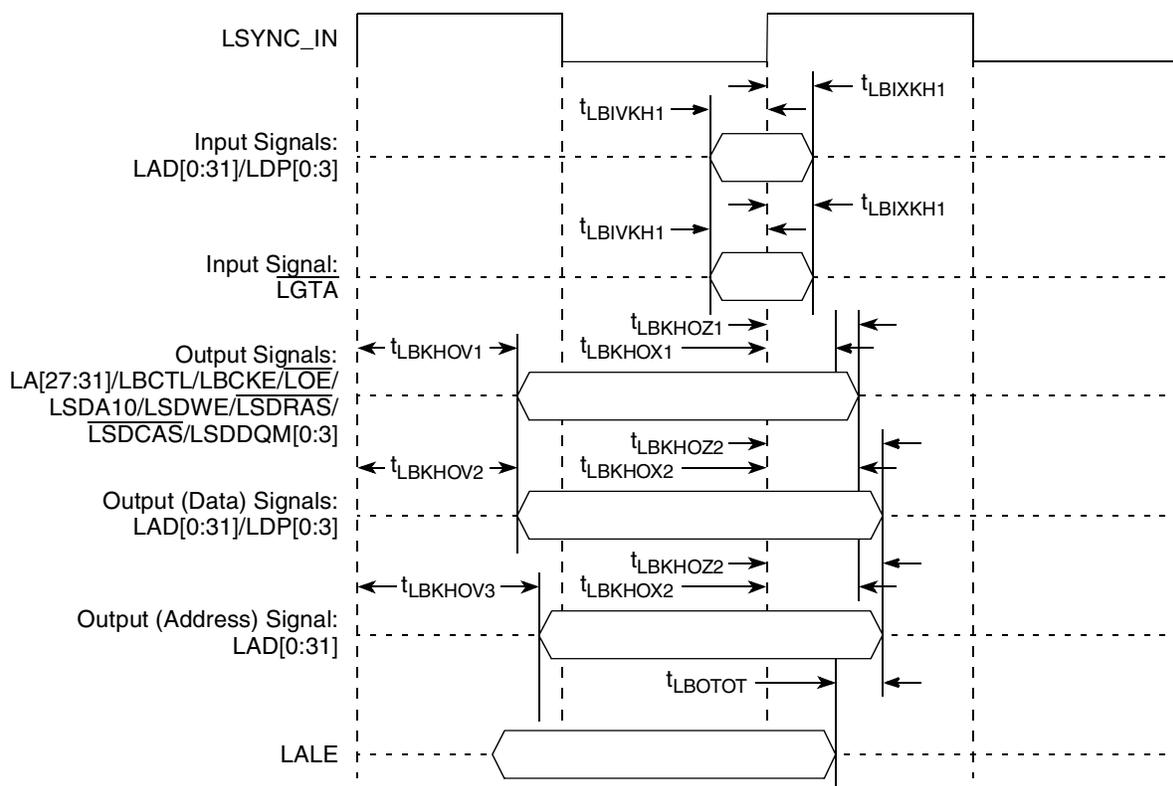


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

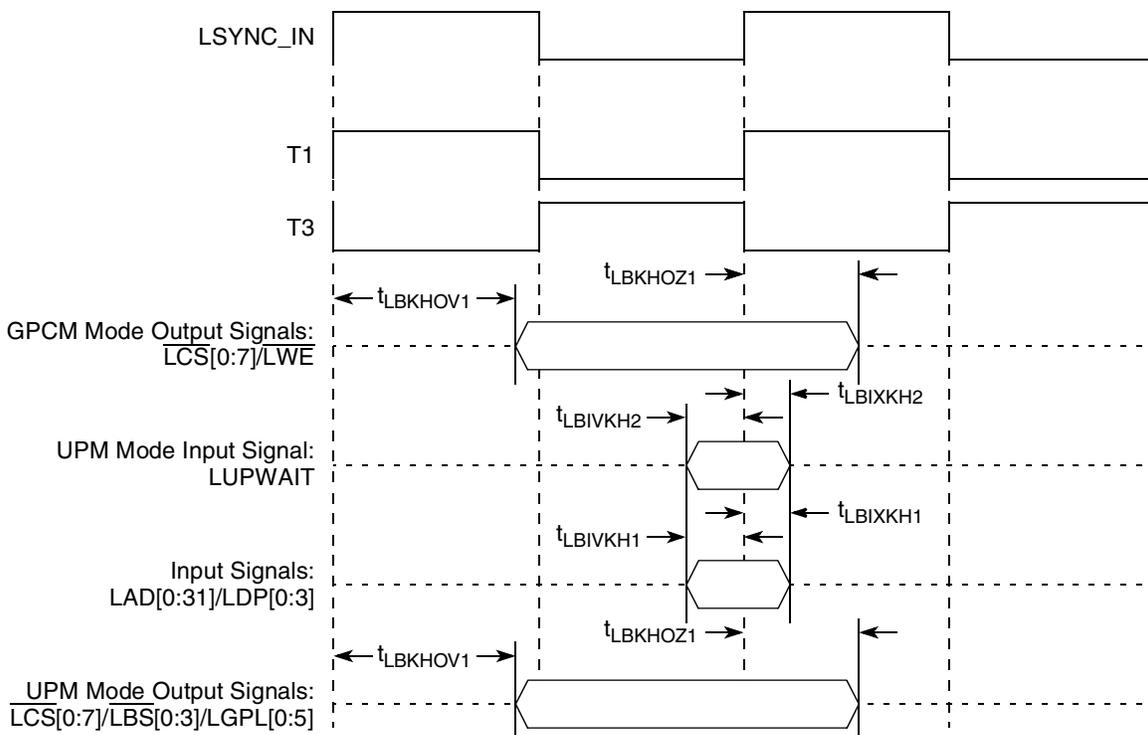


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

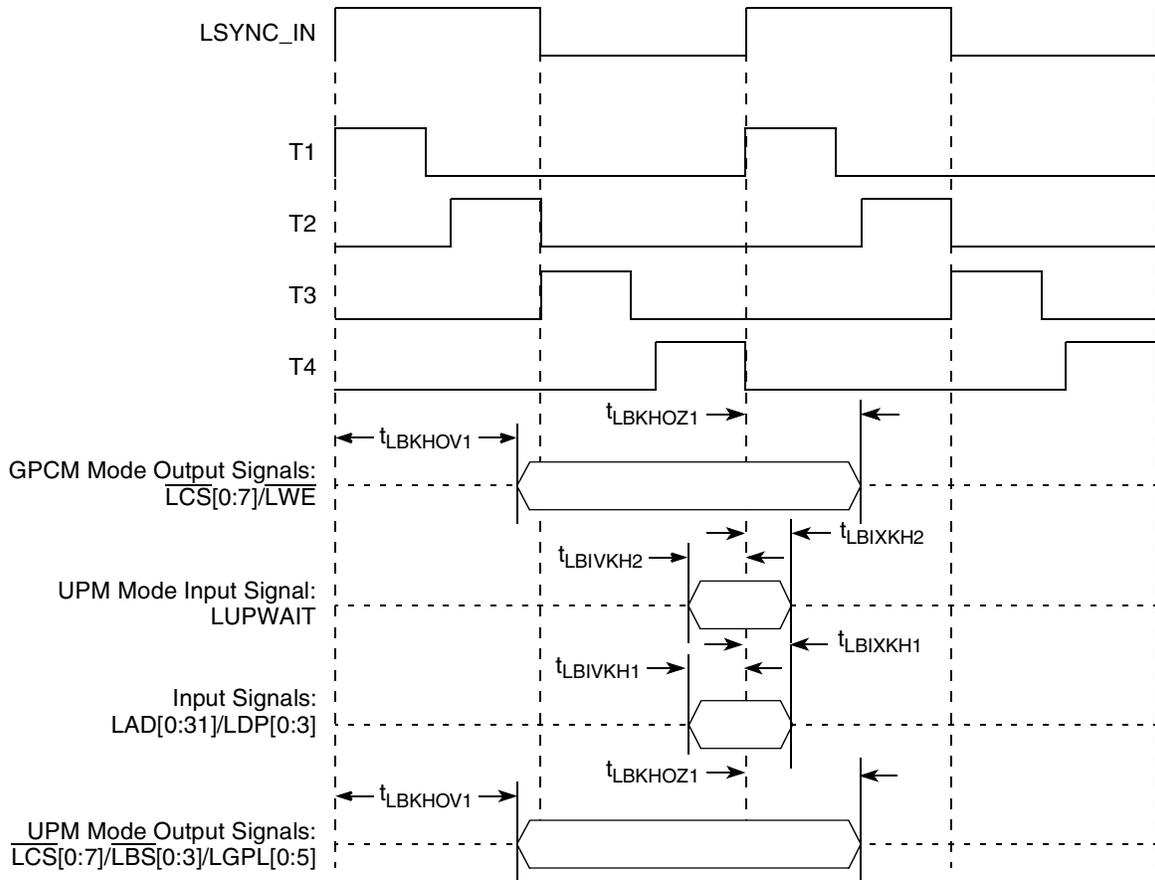


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 31 provides the AC test load for TDO and the boundary-scan outputs of the MPC8541E.

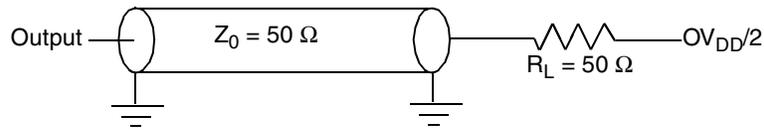


Figure 31. AC Test Load for the JTAG Interface

Figure 32 provides the JTAG clock input timing diagram.

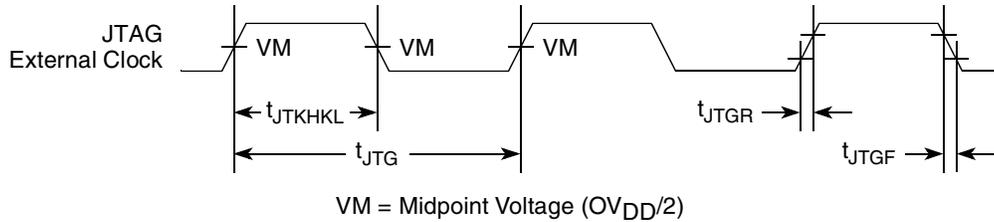


Figure 32. JTAG Clock Input Timing Diagram

Figure 33 provides the \overline{TRST} timing diagram.

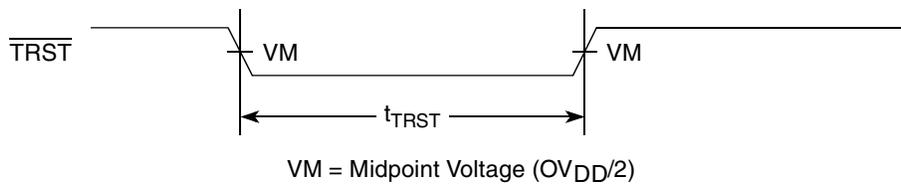


Figure 33. \overline{TRST} Timing Diagram

Figure 34 provides the boundary-scan timing diagram.

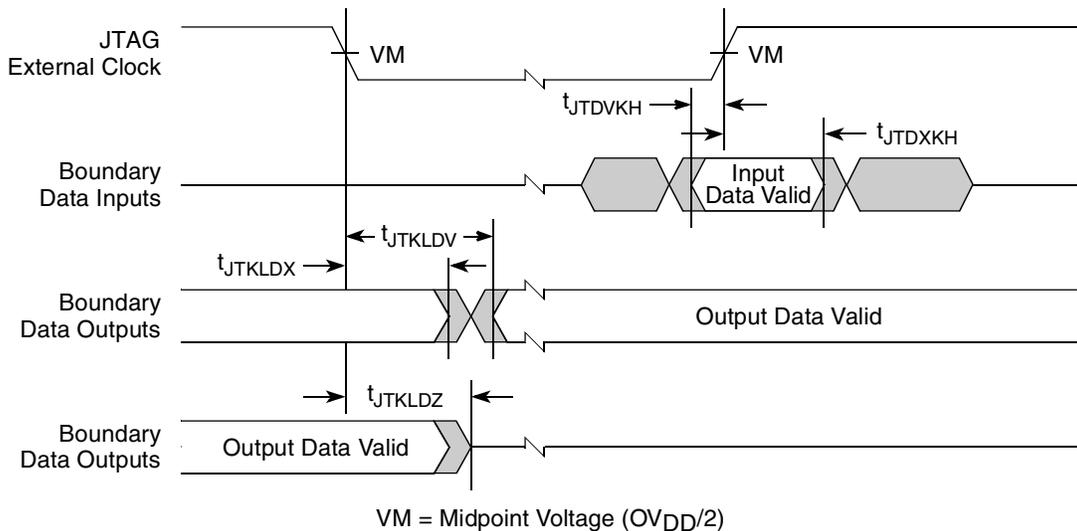


Figure 34. Boundary-Scan Timing Diagram

Figure 35 provides the test access port timing diagram.

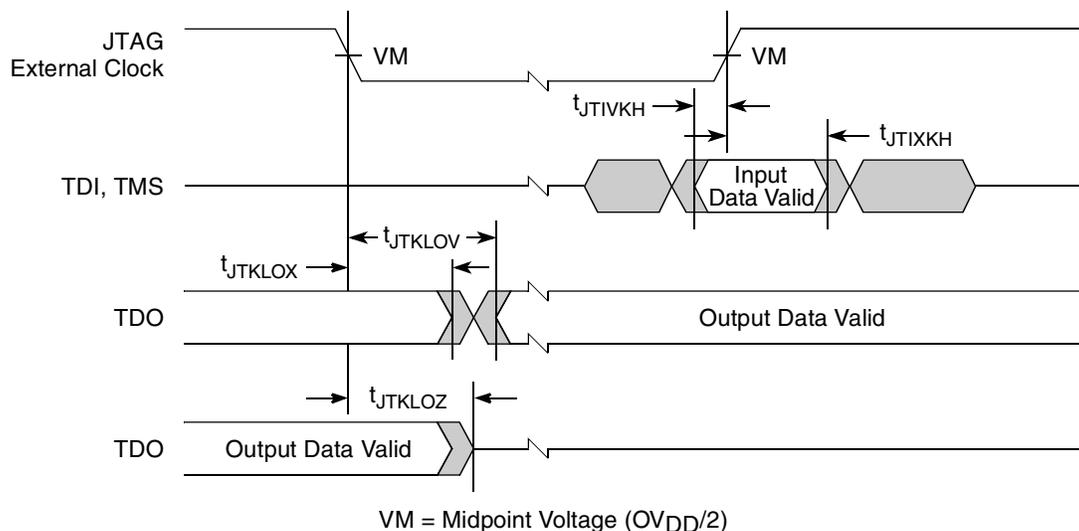


Figure 35. Test Access Port Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8541E.

12.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8541E.

Table 39. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{i2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{i2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}(\text{max})$)	I_I	-10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I²C interface of the MPC8541E.

Table 40. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL} ⁶	1.3	—	μs
High period of the SCL clock	t _{I2CH} ⁶	0.6	—	μs
Setup time for a repeated START condition	t _{I2SVKH} ⁶	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL} ⁶	0.6	—	μs
Data setup time	t _{I2DVKH} ⁶	100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	— 0 ²	— 0.9 ³	μs
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	0.1 × OV _{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	0.2 × OV _{DD}	—	V

Notes:

- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8541E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.
- Guaranteed by design.

14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8541E, 783 FC-PBGA package.

Table 43. MPC8541E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (one 64-bit or two 32-bit)				
PCI1_AD[63:32], PCI2_AD[31:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV _{DD}	17
PCI_C_BE64[7:4] PCI2_C_BE[3:0]	AG13, AH13, V14, W14	I/O	OV _{DD}	17
PCI_C_BE64[3:0] PCI1_C_BE[3:0]	AH8, AB10, AD11, AC12	I/O	OV _{DD}	17
PCI1_PAR	AA11	I/O	OV _{DD}	—
PCI1_PAR64/PCI2_PAR	Y14	I/O	OV _{DD}	—
PCI1_FRAME	AC10	I/O	OV _{DD}	2
PCI1_TRDY	AG10	I/O	OV _{DD}	2
PCI1_IRDY	AD10	I/O	OV _{DD}	2
PCI1_STOP	V11	I/O	OV _{DD}	2
PCI1_DEVSEL	AH10	I/O	OV _{DD}	2
PCI1_IDSEL	AA9	I	OV _{DD}	—
PCI1_REQ64/PCI2_FRAME	AE13	I/O	OV _{DD}	5, 10
PCI1_ACK64/PCI2_DEVSEL	AD13	I/O	OV _{DD}	2
PCI1_PERR	W11	I/O	OV _{DD}	2
PCI1_SERR	Y11	I/O	OV _{DD}	2, 4
PCI1_REQ[0]	AF5	I/O	OV _{DD}	—
PCI1_REQ[1:4]	AF3, AE4, AG4, AE5	I	OV _{DD}	—
PCI1_GNT[0]	AE6	I/O	OV _{DD}	—
PCI1_GNT[1:4]	AG5, AH5, AF6, AG6	O	OV _{DD}	5, 9
PCI1_CLK	AH25	I	OV _{DD}	—
PCI2_CLK	AH27	I	OV _{DD}	—
PCI2_GNT[0]	AC18	I/O	OV _{DD}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV _{DD}	—
IRQ8	AB20	I	OV _{DD}	9
IRQ9/DMA_DREQ ₃	Y20	I	OV _{DD}	1
IRQ10/DMA_DACK ₃	AF26	I/O	OV _{DD}	1
IRQ11/DMA_DDONE ₃	AH24	I/O	OV _{DD}	1
IRQ_OUT	AB21	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV _{DD}	5, 9
EC_MDIO	E1	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV _{DD}	—
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV _{DD}	9, 18
TSEC1_TX_EN	C8	O	LV _{DD}	11
TSEC1_TX_ER	B8	O	LV _{DD}	—
TSEC1_TX_CLK	C6	I	LV _{DD}	—
TSEC1_GTX_CLK	B6	O	LV _{DD}	—
TSEC1_CRS	C3	I	LV _{DD}	—
TSEC1_COL	G7	I	LV _{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV _{DD}	—
TSEC1_RX_DV	D2	I	LV _{DD}	—
TSEC1_RX_ER	E5	I	LV _{DD}	—
TSEC1_RX_CLK	D6	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV _{DD}	—
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV _{DD}	5, 9, 18
TSEC2_TX_EN	B11	O	LV _{DD}	11
TSEC2_TX_ER	D11	O	LV _{DD}	—
TSEC2_TX_CLK	D10	I	LV _{DD}	—
TSEC2_GTX_CLK	C10	O	LV _{DD}	—

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PB[18:31]	P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/O	OV _{DD}	—
PC[0, 1, 4–29]	R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8	I/O	OV _{DD}	—
PD[7, 14–25, 29–31]	Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2	I/O	OV _{DD}	—

Notes:

- All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5/DMA_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
- Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD}.
- This pin must always be pulled down to GND.
- This pin is an open drain signal.
- This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8541E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
- Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSClk PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See [Section 15.2, “Platform/System PLL Ratio.”](#)
- The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See the [Section 15.3, “e500 Core PLL Ratio.”](#)
- Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
- This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
- This output is actively driven during reset rather than being three-stated during reset.
- These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- Internal thermally sensitive resistor.
- No connections should be made to these pins.
- These pins are not connected for any functional use.
- PCI specifications recommend that a weak pull-up resistor (2–10 k Ω) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI2_C_BE}}$ [7:4]).
- If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
- Recommend a pull-up resistor (~1 k Ω) be placed on this pin to OV_{DD}.
- These are test signals for factory use only and must be pulled up (100 Ω to 1k Ω) to OV_{DD} for normal machine operation.
- If this signal is used as both an input and an output, a weak pull-up (~10k Ω) is required on this pin.
- MSYNC_IN and MSYNC_OUT should be connected together for proper operation.

15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

Table 47. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 48. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	17	25	33	42	67	83	100	111	133
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in [Table 49](#), the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

[Figure 44](#) depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

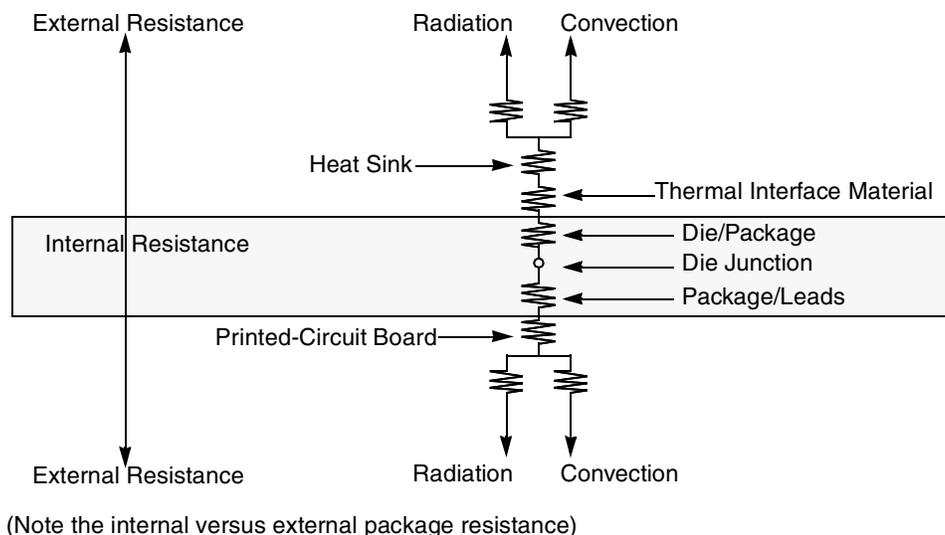


Figure 44. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, [Figure 45](#) shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see [Figure 41](#)). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8541E.

17.1 System Clocking

The MPC8541E includes five PLLs.

1. The platform PLL (AV_{DD1}) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 15.2, “Platform/System PLL Ratio.”](#)
2. The e500 Core PLL (AV_{DD2}) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 15.3, “e500 Core PLL Ratio.”](#)
3. The CPM PLL (AV_{DD3}) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL (AV_{DD4}) generates the clocking for the first PCI bus.
5. The PCI2 PLL (AV_{DD5}) generates the clock for the second PCI bus.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , AV_{DD3} , AV_{DD4} , and AV_{DD5} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 49](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

17.6 Configuration Pin Multiplexing

The MPC8541E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The MPC8541E requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 52](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 51 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 51, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 51 is common to all known emulators.

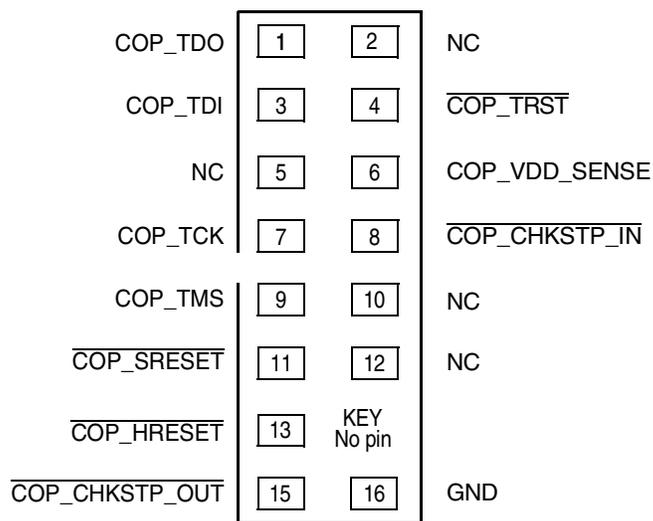


Figure 51. COP Connector Physical Pinout

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