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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8541vtaqf">https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8541vtaqf</a>

- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
  - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI
    - Four inbound windows
    - Four outbound windows plus default translation for PCI
- DDR memory controller
  - Programmable timing supporting first generation DDR SDRAM
  - 64-bit data interface, up to MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Sleep mode support for self refresh DDR SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller

- Four global high resolution timers/counters that can generate interrupts
- Supports additional internal interrupt sources
- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- Two I<sup>2</sup>C controllers (one is contained within the CPM, the other is a stand-alone controller which is not part of the CPM)
  - Two-wire interface
  - Multiple master support
  - Master or slave I<sup>2</sup>C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the stand-alone I<sup>2</sup>C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I<sup>2</sup>C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (RXD, TXD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Two Three-speed (10/100/1000)Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z AC compliant controllers
  - Support for Ethernet physical interfaces:
    - 10/100/1000 Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII

## 4.3 Real Time Clock Timing

Table 8 provides the real time clock (RTC) AC timing specifications.

**Table 8. RTC AC Timing Specifications**

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	$t_{RTCH}$	2 x $t_{CCB\_CLK}$	—	—	ns	—
RTC clock low time	$t_{RTCL}$	2 x $t_{CCB\_CLK}$	—	—	ns	—

## 5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8541E. Table 9 provides the RESET initialization AC timing specifications.

**Table 9. RESET Initialization Timing Specifications**

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$	100	—	$\mu s$	—
Minimum assertion time for $\overline{SRESET}$	512	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{HRESET}$ negation	100	—	$\mu s$	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{HRESET}$	4	—	SYSCLKs	1
Input hold time for POR configs (including PLL config) with respect to negation of $\overline{HRESET}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{HRESET}$	—	5	SYSCLKs	1

**Notes:**

1. SYSCLK is identical to the PCI\_CLK signal and is the primary clock input for the MPC8541E. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for more details.

Table 10 provides the PLL and DLL lock times.

**Table 10. PLL and DLL Lock Times**

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	$\mu s$	—
DLL lock times	7680	122,880	CCB Clocks	1, 2

**Notes:**

1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the  $SYSCLK \times \text{platform PLL ratio}$ .

## 7.2 DUART AC Electrical Specifications

Table 17 provides the AC timing parameters for the DUART interface of the MPC8541E.

**Table 17. DUART AC Timing Specifications**

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB\_CLK} / 1048576$	baud	3
Maximum baud rate	$f_{CCB\_CLK} / 16$	baud	1, 3
Oversample rate	16	—	2, 3

**Notes:**

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8<sup>th</sup> sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16<sup>th</sup> sample.
3. Guaranteed by design.

## 8 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

### 8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), the MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 V or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, “Ethernet Management Interface Electrical Characteristics.”

#### 8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 18 and Table 19. The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver’s power supply (for example, a GMII driver powered from a 3.6-V supply driving  $V_{OH}$  into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

### 8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

**Table 21. GMII Receive AC Timing Specifications**

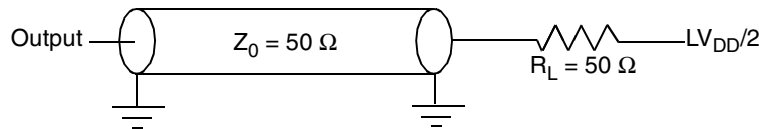
At recommended operating conditions with  $LV_{DD}$  of  $3.3\text{ V} \pm 5\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
RX_CLK clock period	$t_{GRX}$	—	8.0	—	ns
RX_CLK duty cycle	$t_{GRXH}/t_{GRX}$	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	$t_{GRDVKH}$	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	$t_{GRDXKH}$	0.5	—	—	ns
RX_CLK clock rise and fall time	$t_{GRXR}, t_{GRXF}$ <sup>2,3</sup>	—	—	1.0	ns

**Note:**

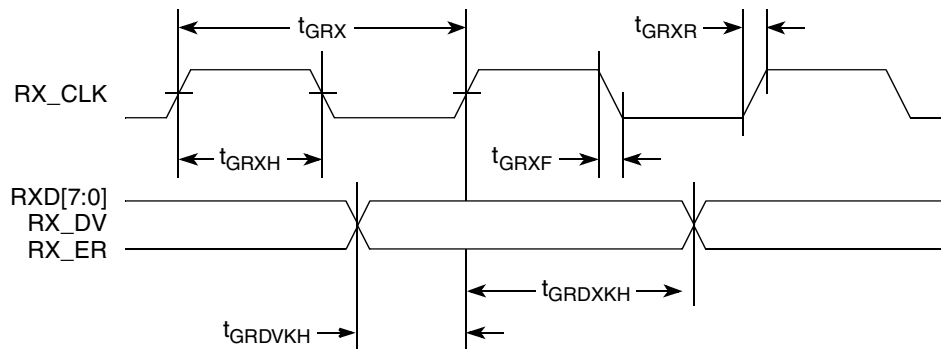
- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{GRDVKH}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{RX}$  clock reference (K) going to the high state (H) or setup time. Also,  $t_{GRDXKL}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{GRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GRX}$  represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 8 provides the AC test load for TSEC.



**Figure 8. TSEC AC Test Load**

Figure 9 shows the GMII receive AC timing diagram.



**Figure 9. GMII Receive AC Timing Diagram**

## 8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

**Table 24. TBI Transmit AC Timing Specifications**

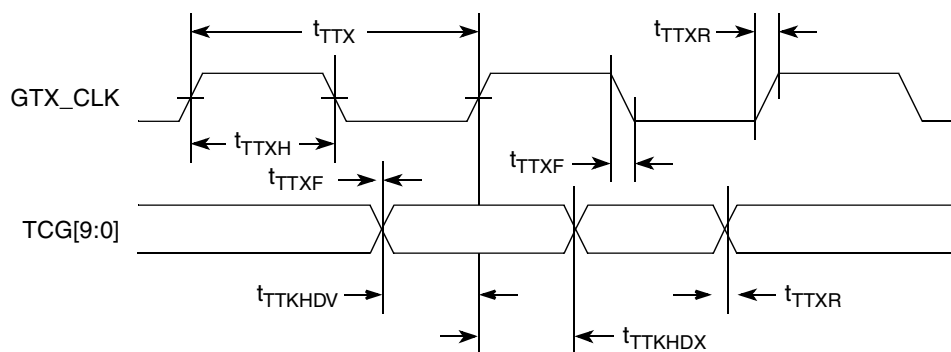
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
GTX_CLK clock period	$t_{TTX}$	—	8.0	—	ns
GTX_CLK duty cycle	$t_{TTXH}/t_{TTX}$	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	$t_{TTKHdV}$	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	$t_{TTKHdX}$	1.0	—	—	ns
GTX_CLK clock rise and fall time	$t_{TTXR}$ , $t_{TTXF}$ <sup>2,3</sup>	—	—	1.0	ns

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{TTKHdV}$  symbolizes the TBI transmit timing (TT) with respect to the time from  $t_{TTX}$  (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also,  $t_{TTKHdX}$  symbolizes the TBI transmit timing (TT) with respect to the time from  $t_{TTX}$  (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{TTX}$  represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.



**Figure 12. TBI Transmit AC Timing Diagram**

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.

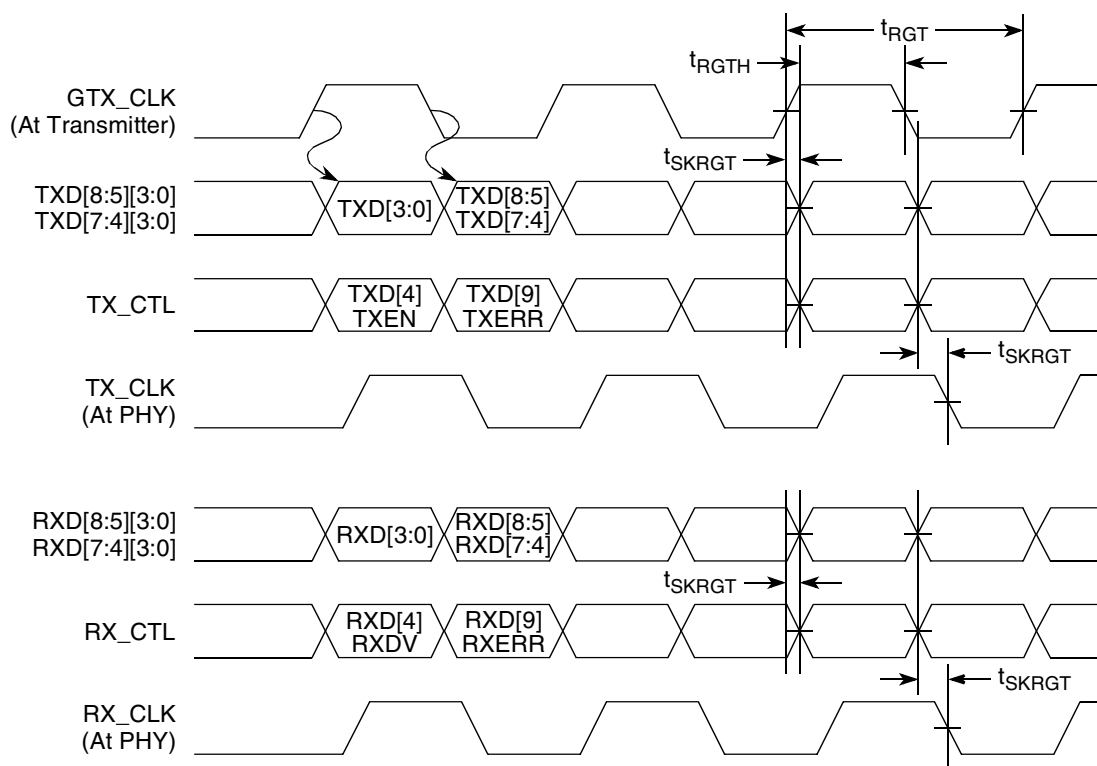


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

## 8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in [Section 8.1, “Three-Speed Ethernet Controller \(TSEC\) \(10/100/1000 Mbps\)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”](#)

### 8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 27](#).

Table 27. MII Management DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	$OV_{DD}$	—		3.13	3.47	V
Output high voltage	$V_{OH}$	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.10	$LV_{DD} + 0.3$	V
Output low voltage	$V_{OL}$	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	$V_{IH}$	—		1.70	—	V
Input low voltage	$V_{IL}$	—		—	0.90	V



**Table 27. MII Management DC Electrical Characteristics (continued)**

Parameter	Symbol	Conditions		Min	Max	Unit
Input high current	$I_{IH}$	$LV_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	$\mu\text{A}$
Input low current	$I_{IL}$	$LV_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	−600	—	$\mu\text{A}$

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

### 8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

**Table 28. MII Management AC Timing Specifications**

At recommended operating conditions with  $LV_{DD}$  is  $3.3 \text{ V} \pm 5\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit	Notes
MDC frequency	$f_{MDC}$	0.893	—	10.4	MHz	2
MDC period	$t_{MDC}$	96	—	1120	ns	
MDC clock pulse width high	$t_{MDCH}$	32	—	—	ns	
MDC to MDIO valid	$t_{MDKHDV}$			$2 \cdot [1/(f_{ccb\_clk}/8)]$	ns	3
MDC to MDIO delay	$t_{MDKHDX}$	10	—	$2 \cdot [1/(f_{ccb\_clk}/8)]$	ns	3
MDIO to MDC setup time	$t_{MDDVKH}$	5	—	—	ns	
MDIO to MDC hold time	$t_{MDDXKH}$	0	—	—	ns	
MDC rise time	$t_{MDCR}$	—	—	10	ns	
MDC fall time	$t_{MDHF}$	—	—	10	ns	

**Notes:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{MDKHDX}$  symbolizes management data timing (MD) for the time  $t_{MDC}$  from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also,  $t_{MDDVKH}$  symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MDC}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
- This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
- Guaranteed by design.

Figure 15 shows the MII management AC timing diagram.

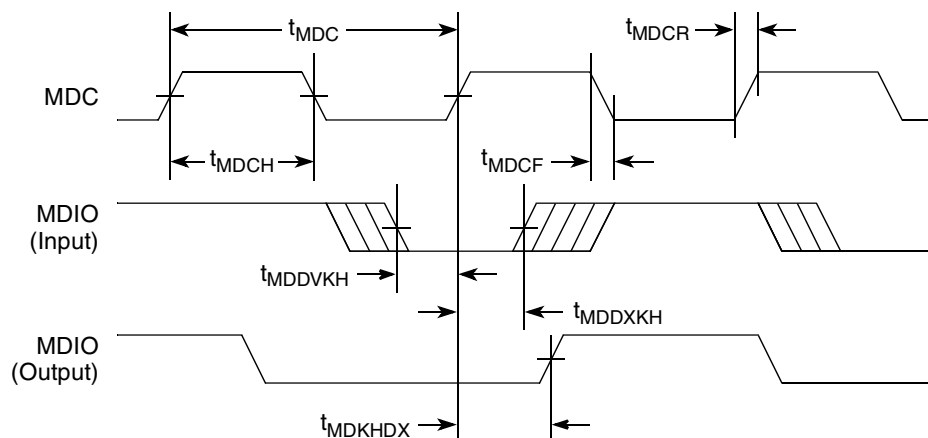


Figure 15. MII Management Interface Timing Diagram

## 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8541E.

### 9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	$V_{IH}$	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$		-0.3	0.8	V
Input current	$I_{IN}$	$V_{IN}^1 = 0 \text{ V or } V_{IN} = V_{DD}$	—	$\pm 5$	$\mu\text{A}$
High-level output voltage	$V_{OH}$	$OV_{DD} = \text{min, } I_{OH} = -2\text{mA}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	$V_{OL}$	$OV_{DD} = \text{min, } I_{OL} = 2\text{mA}$	—	0.2	V

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

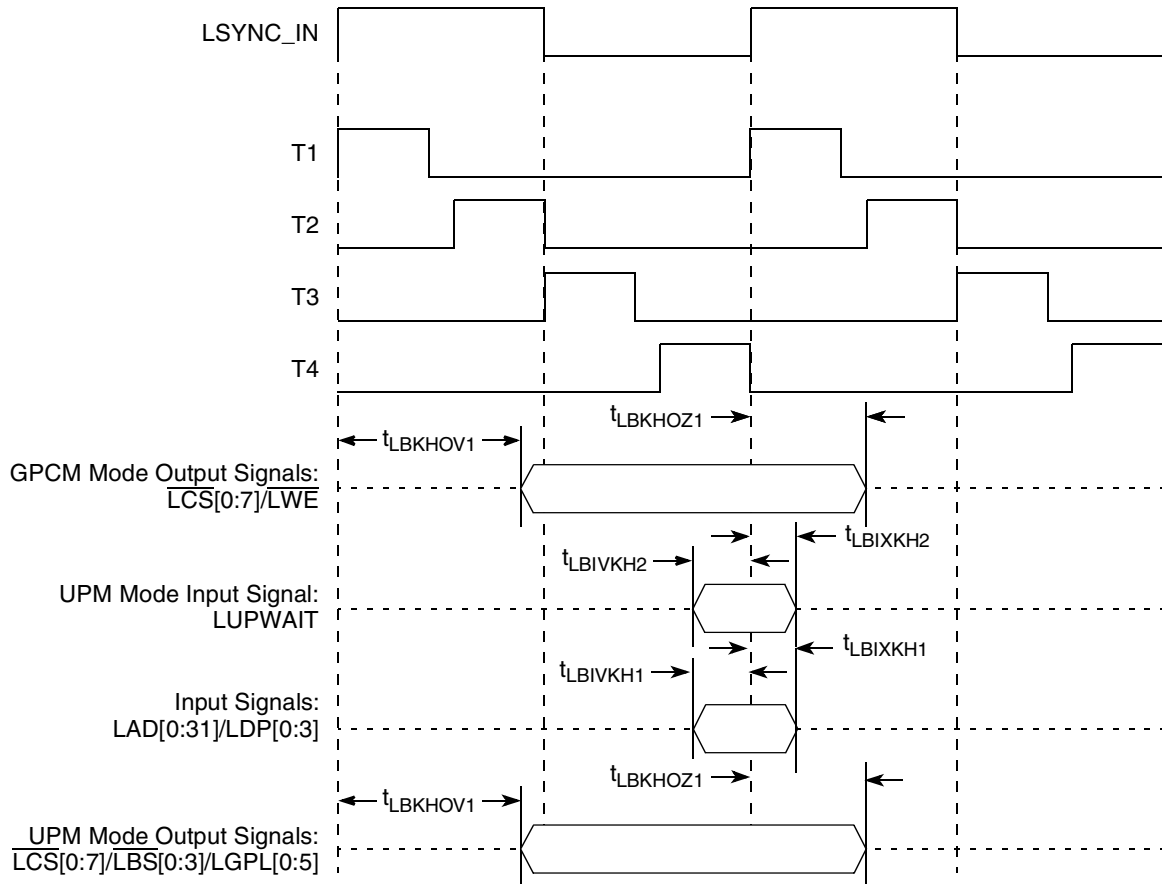


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

**Table 33. CPM Input AC Timing Specifications <sup>1</sup> (continued)**

Characteristic	Symbol <sup>2</sup>	Min <sup>3</sup>	Unit
PIO inputs—input hold time	$t_{PIIXKH}$	1	ns
COL width high (FCC)	$t_{FCCH}$	1.5	CLK

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{FIIVKH}$  symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock  $t_{FCC}$  (K) going to the high (H) state or setup time.
3. PIO and TIMER inputs and outputs are asynchronous to SYCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

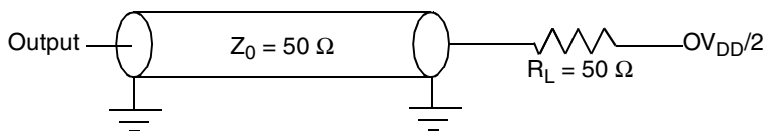
**Table 34. CPM Output AC Timing Specifications <sup>1</sup>**

Characteristic	Symbol <sup>2</sup>	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	$t_{FIKHOX}$	1	5.5	ns
FCC outputs—external clock (NMSI) delay	$t_{FEKHOX}$	2	8	ns
SPI outputs—internal clock (NMSI) delay	$t_{NIKHOX}$	0.5	10	ns
SPI outputs—external clock (NMSI) delay	$t_{NEKHOX}$	2	8	ns
PIO outputs delay	$t_{PIKHOX}$	1	11	ns

**Notes:**

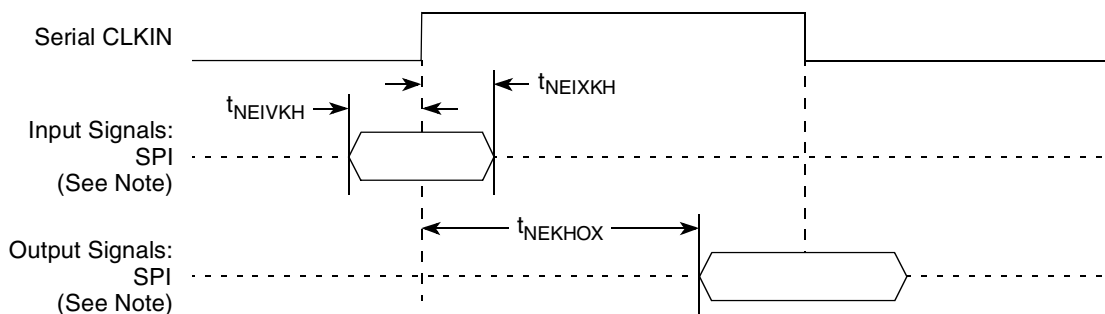
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{FIKHOX}$  symbolizes the FCC inputs internal timing (FI) for the time  $t_{FCC}$  memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 23 provides the AC test load for the CPM.



**Figure 23. CPM AC Test Load**

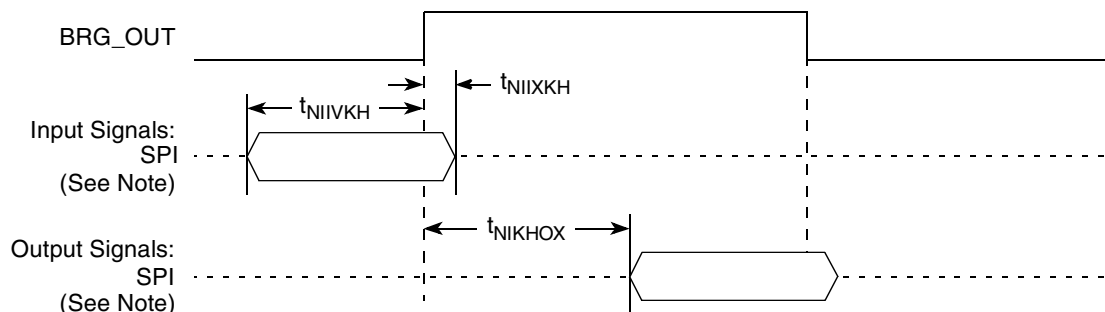
Figure 27 shows the SPI external clock.



**Note:** The clock edge is selectable on SPI.

**Figure 27. SPI AC Timing External Clock Diagram**

Figure 28 shows the SPI internal clock.



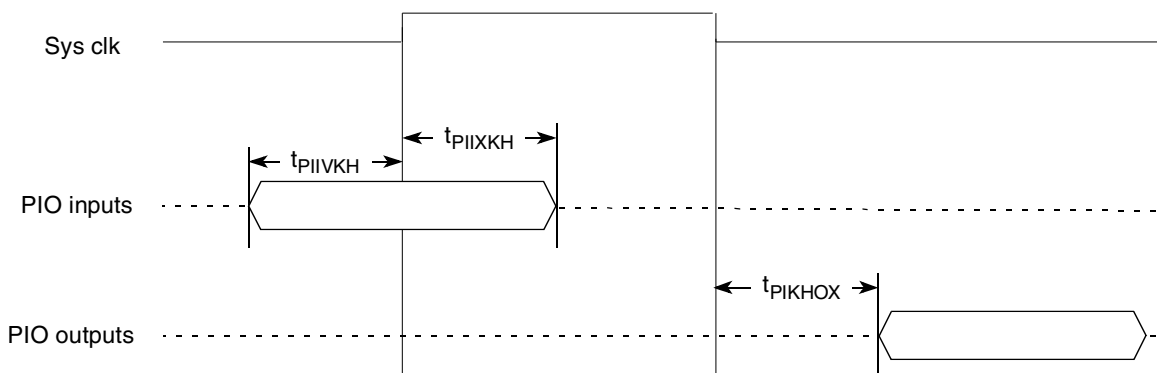
**Note:** The clock edge is selectable on SPI.

**Figure 28. SPI AC Timing Internal Clock Diagram**

### NOTE

<sup>1</sup> SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

<sup>2</sup> SPI AC timings refer always to SPICLK.



**Figure 29. PIO Signal Diagram**

## 12.2 I<sup>2</sup>C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I<sup>2</sup>C interface of the MPC8541E.

**Table 40. I<sup>2</sup>C AC Electrical Specifications**

All values refer to  $V_{IH}$  (min) and  $V_{IL}$  (max) levels (see Table 39).

Parameter	Symbol <sup>1</sup>	Min	Max	Unit
SCL clock frequency	$f_{I2C}$	0	400	kHz
Low period of the SCL clock	$t_{I2CL}$ <sup>6</sup>	1.3	—	μs
High period of the SCL clock	$t_{I2CH}$ <sup>6</sup>	0.6	—	μs
Setup time for a repeated START condition	$t_{I2SVKH}$ <sup>6</sup>	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	$t_{I2SXKL}$ <sup>6</sup>	0.6	—	μs
Data setup time	$t_{I2DVKH}$ <sup>6</sup>	100	—	ns
Data hold time: CBUS compatible masters I <sup>2</sup> C bus devices	$t_{I2DXKL}$	— 0 <sup>2</sup>	— 0.9 <sup>3</sup>	μs
Rise time of both SDA and SCL signals	$t_{I2CR}$	$20 + 0.1 C_b$ <sup>4</sup>	300	ns
Fall time of both SDA and SCL signals	$t_{I2CF}$	$20 + 0.1 C_b$ <sup>4</sup>	300	ns
Set-up time for STOP condition	$t_{I2PVKH}$	0.6	—	μs
Bus free time between a STOP and START condition	$t_{I2KHDX}$	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	$V_{NL}$	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	$V_{NH}$	$0.2 \times OV_{DD}$	—	V

### Notes:

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{I2DVKH}$  symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{I2C}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{I2SXKL}$  symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the  $t_{I2C}$  clock reference (K) going to the low (L) state or hold time. Also,  $t_{I2PVKH}$  symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the  $t_{I2C}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8541E provides a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum  $t_{I2DVKH}$  has only to be met if the device does not stretch the LOW period ( $t_{I2CL}$ ) of the SCL signal.
- $C_b$  = capacitance of one bus line in pF.
- Guaranteed by design.

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_GNT[1:4]	AD18, AE18, AE19, AD19	O	OV <sub>DD</sub>	5, 9
PCI2_IDSEL	AC22	I	OV <sub>DD</sub>	—
PCI2_IRDY	AD20	I/O	OV <sub>DD</sub>	2
PCI2_PERR	AC20	I/O	OV <sub>DD</sub>	2
PCI2_REQ[0]	AD21	I/O	OV <sub>DD</sub>	—
PCI2_REQ[1:4]	AE21, AD22, AE22, AC23	I	OV <sub>DD</sub>	—
PCI2_SERR	AE20	I/O	OV <sub>DD</sub>	2,4
PCI2_STOP	AC21	I/O	OV <sub>DD</sub>	2
PCI2_TRDY	AC19	I/O	OV <sub>DD</sub>	2
<b>DDR SDRAM Memory Interface</b>				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV <sub>DD</sub>	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV <sub>DD</sub>	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV <sub>DD</sub>	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV <sub>DD</sub>	—
MBA[0:1]	B18, B19	O	GV <sub>DD</sub>	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV <sub>DD</sub>	—
MWE	D17	O	GV <sub>DD</sub>	—
MRAS	F17	O	GV <sub>DD</sub>	—
MCAS	J16	O	GV <sub>DD</sub>	—
MCS[0:3]	H16, G16, J15, H15	O	GV <sub>DD</sub>	—
MCKE[0:1]	E26, E28	O	GV <sub>DD</sub>	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV <sub>DD</sub>	—
MCK[0:5]	F20, G27, B15, E20, F27, L14	O	GV <sub>DD</sub>	—
MSYNC_IN	M28	I	GV <sub>DD</sub>	22
MSYNC_OUT	N28	O	GV <sub>DD</sub>	22
<b>Local Bus Controller Interface</b>				
LA[27]	U18	O	OV <sub>DD</sub>	5, 9

Table 43. MPC8541E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_CRS	D9	I	LV <sub>DD</sub>	—
TSEC2_COL	F8	I	LV <sub>DD</sub>	—
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV <sub>DD</sub>	—
TSEC2_RX_DV	H8	I	LV <sub>DD</sub>	—
TSEC2_RX_ER	A8	I	LV <sub>DD</sub>	—
TSEC2_RX_CLK	E10	I	LV <sub>DD</sub>	—
<b>DUART</b>				
UART_CTS[0,1]	Y2, Y3	I	OV <sub>DD</sub>	—
UART_RTS[0,1]	Y1, AD1	O	OV <sub>DD</sub>	—
UART_SIN[0,1]	P11, AD5	I	OV <sub>DD</sub>	—
UART_SOUT[0,1]	N6, AD2	O	OV <sub>DD</sub>	—
<b>I<sup>2</sup>C interface</b>				
IIC_SDA	AH22	I/O	OV <sub>DD</sub>	4, 19
IIC_SCL	AH23	I/O	OV <sub>DD</sub>	4, 19
<b>System Control</b>				
HRESET	AH16	I	OV <sub>DD</sub>	—
HRESET_REQ	AG20	O	OV <sub>DD</sub>	18
SRESET	AF20	I	OV <sub>DD</sub>	—
CKSTP_IN	M11	I	OV <sub>DD</sub>	—
CKSTP_OUT	G1	O	OV <sub>DD</sub>	2, 4
<b>Debug</b>				
TRIG_IN	N12	I	OV <sub>DD</sub>	—
TRIG_OUT/READY	G2	O	OV <sub>DD</sub>	6, 9, 18
MSRCID[0:1]	J9, G3	O	OV <sub>DD</sub>	5, 6, 9
MSRCID[2:3]	F3, F5	O	OV <sub>DD</sub>	6
MSRCID4	F2	O	OV <sub>DD</sub>	6
MDVAL	F4	O	OV <sub>DD</sub>	6
<b>Clock</b>				
SYSCLK	AH21	I	OV <sub>DD</sub>	—
RTC	AB23	I	OV <sub>DD</sub>	—
CLK_OUT	AF22	O	OV <sub>DD</sub>	—



# 16 Thermal

This section describes the thermal specifications of the MPC8541E.

## 16.1 Thermal Characteristics

Table 49 provides the package thermal characteristics for the MPC8541E.

**Table 49. Package Thermal Characteristics**

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@400 ft/min or 2.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	$R_{\theta JC}$	0.96	°C/W	4

### Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51–6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

## 16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 42. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that allows the MPC8541E to function in various environments.

## 16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8541E thermal model is shown in Figure 44. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

Conductivity	Value	Unit
Lid (11 × 11 × 1 mm)		W/(m × K)
k <sub>x</sub>	360	
k <sub>y</sub>	360	
k <sub>z</sub>	360	
Lid Adhesive—Collapsed resistance (8.7 × 9.3 × 0.05 mm)		
k <sub>z</sub>	1.07	
Die (8.7 × 9.3 × 0.75 mm)		
Bump/Underfill—Collapsed resistance (8.7 × 9.3 × 0.07 mm)		
k <sub>z</sub>	4.4	
Substrate and Solder Balls (25 × 25 × 1.6 mm)		
k <sub>x</sub>	14.2	
k <sub>y</sub>	14.2	
k <sub>z</sub>	1.2	

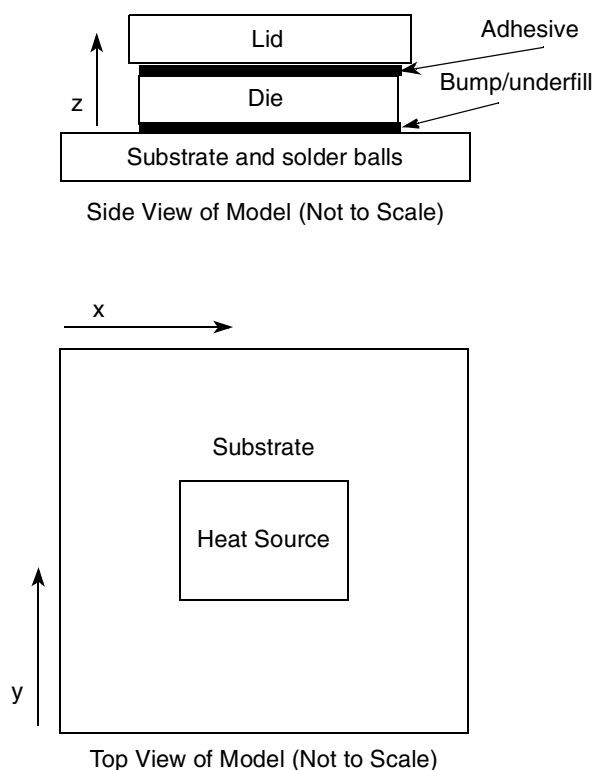


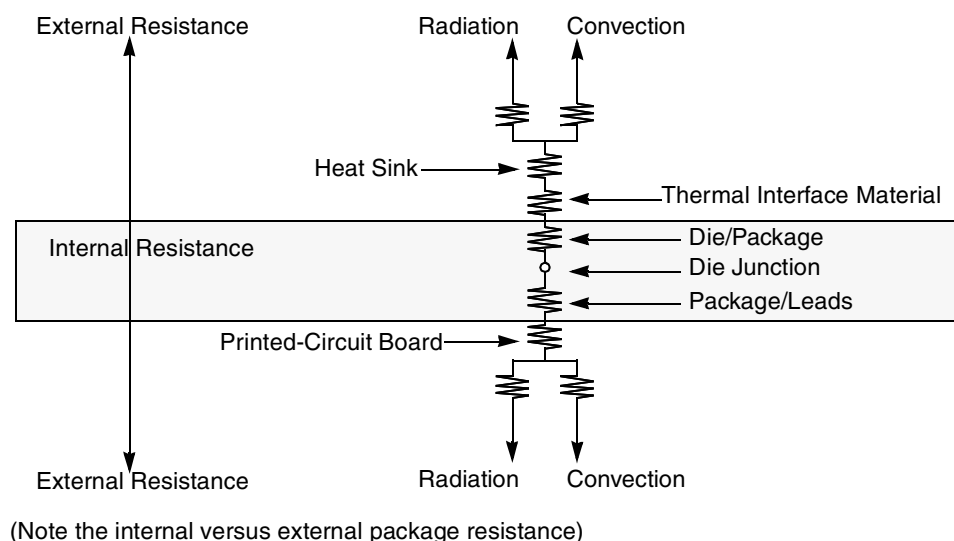
Figure 43. MPC8541E Thermal Model

## 16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 44 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



**Figure 44. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

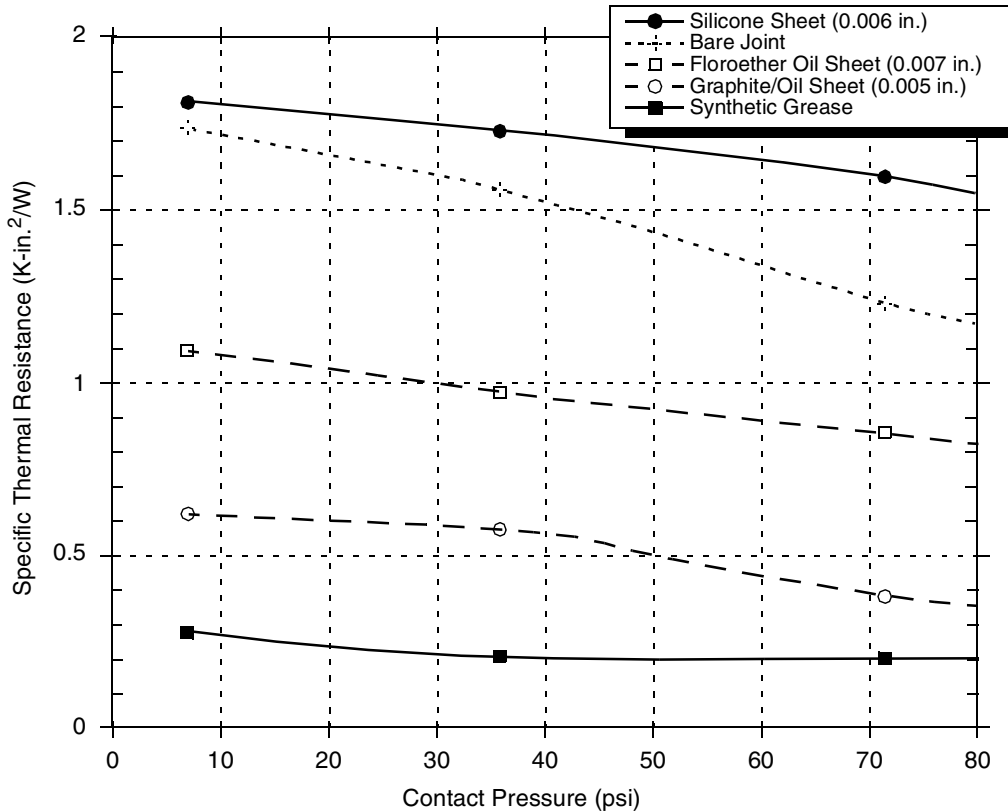
## 16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 45 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 41). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

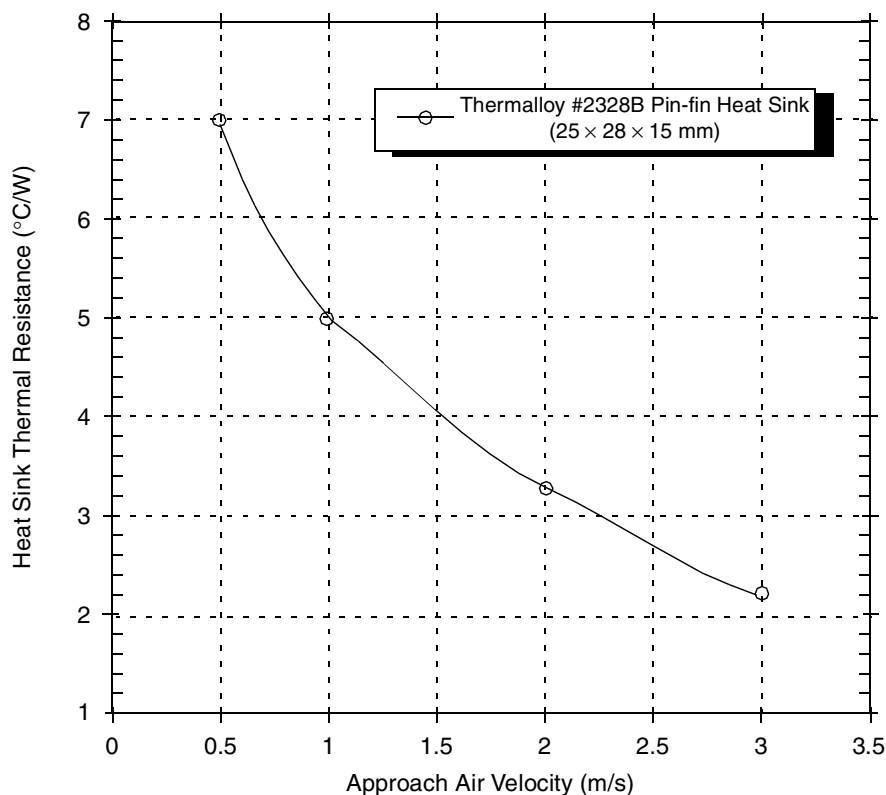
the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.



**Figure 45. Thermal Performance of Select Thermal Interface Materials**

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: <a href="http://www.chomerics.com">www.chomerics.com</a>	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: <a href="http://www.dowcorning.com">www.dowcorning.com</a>	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: <a href="http://www.microsi.com">www.microsi.com</a>	888-642-7674
The Bergquist Company 18930 West 78 <sup>th</sup> St.	800-347-4572



**Figure 46. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity**

#### 16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in [Table 49](#) includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in [Figure 47](#) and [Figure 48](#). This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.