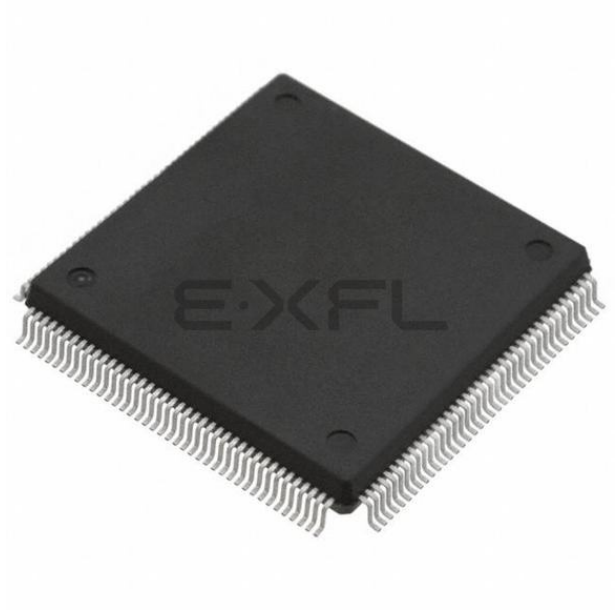

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, SPI, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 39 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.4V ~ 1.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 160-BQFP |
| Supplier Device Package | 160-QFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5270ab100 |

# 1 MCF5271 Family Configurations

**Table 1. MCF5271 Family Configurations**

| Module | MCF5270 | MCF5271 |
|---|---|---|
| ColdFire V2 Core with EMAC and Hardware Divide | x | x |
| System Clock | 150 MHz | |
| Performance (Dhrystone/2.1 MIPS) | 144 | |
| Instruction/Data Cache | 8 Kbytes | |
| Static RAM (SRAM) | 64 Kbytes | |
| Interrupt Controllers (INTC) | 2 | 2 |
| Edge Port Module (EPORT) | x | x |
| External Interface Module (EIM) | x | x |
| 4-channel Direct-Memory Access (DMA) | x | x |
| SDRAM Controller | x | x |
| Fast Ethernet Controller (FEC) | x | x |
| Hardware Encryption | — | x |
| Watchdog Timer (WDT) | x | x |
| Four Periodic Interrupt Timers (PIT) | x | x |
| 32-bit DMA Timers | 4 | 4 |
| QSPI | x | x |
| UART(s) | 3 | 3 |
| $I^2C$ | x | x |
| General Purpose I/O Module (GPIO) | x | x |
| JTAG - IEEE 1149.1 Test Access Port | x | x |
| Package | 160 QFP, 196 MAPBGA | 160 QFP, 196 MAPBGA |

# 2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array plastic ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

# 3 Features

For a detailed feature list see the MCF5271 Reference Manual (MCF5271RM).

# 4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5271 signals, consult the *MCF5271 Reference Manual* (MCF5271RM).

## 4.1 Signal Properties

Table 4 lists all of the signals grouped by function. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts and Part Numbers," for package diagrams.

**NOTE**

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

**NOTE**

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

**Table 2. MCF5270 and MCF5271 Signal Information and Muxing**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | MCF5270 MCF5271 160 QFP | MCF5270 MCF5271 196 MAPBGA |
|---|---|---|---|---|---|---|
| **Reset** | | | | | | |
| $\overline{\text{RESET}}$ | — | — | — | I | 83 | N13 |
| $\overline{\text{RSTOUT}}$ | — | — | — | O | 82 | P13 |
| **Clock** | | | | | | |
| EXTAL | — | — | — | I | 86 | M14 |
| XTAL | — | — | — | O | 85 | N14 |
| CLKOUT | — | — | — | O | 89 | K14 |
| **Mode Selection** | | | | | | |
| CLKMOD[1:0] | — | — | — | I | 20,21 | G5,H5 |
| $\overline{\text{RCON}}$ | — | — | — | I | 79 | K10 |
| **External Memory Interface and Ports** | | | | | | |
| A[23:21] | PADDR[7:5] | $\overline{\text{CS}}$[6:4] | — | O | 126, 125, 124 | B11, C11, D11 |

**Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | MCF5270 MCF5271 160 QFP | MCF5270 MCF5271 196 MAPBGA |
|---|---|---|---|---|---|---|
| A[20:0] | — | — | — | O | 123:115, 112:106, 102:98 | A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13 |
| D[31:16] | — | — | — | O | 22:30, 33:39 | G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2 |
| D[15:8] | PDATAH[7:0] | — | — | O | 42:49 | M1, N1, M2, N2, P2, L3, M3, N3 |
| D[7:0] | PDATAL[7:0] | — | — | O | 50:52, 56:60 | P3, M4, N4, P4, L5, M5, N5, P5 |
| $\overline{BS}$[3:0] | PBS[7:4] | $\overline{CAS}$[3:0] | — | O | 143:140 | B6, C6, D7, C7 |
| $\overline{OE}$ | PBUSCTL7 | — | — | O | 62 | N6 |
| $\overline{TA}$ | PBUSCTL6 | — | — | I | 96 | H11 |
| $\overline{TEA}$ | PBUSCTL5 | $\overline{DREQ1}$ | — | I | — | J14 |
| R/$\overline{W}$ | PBUSCTL4 | — | — | O | 95 | J13 |
| $\overline{TSIZ1}$ | PBUSCTL3 | DACK1 | — | O | — | P6 |
| $\overline{TSIZ0}$ | PBUSCTL2 | DACK0 | — | O | — | P7 |
| $\overline{TS}$ | PBUSCTL1 | DACK2 | — | O | 97 | H13 |
| $\overline{TIP}$ | PBUSCTL0 | DREQ0 | — | O | — | H12 |
| **Chip Selects** | | | | | | |
| $\overline{CS}$[7:4] | PCS[7:4] | — | — | O | — | B9, A10, C10, A11 |
| $\overline{CS}$[3:2] | PCS[3:2] | SD_CS[1:0] | — | O | 132,131 | A9, C9 |
| $\overline{CS1}$ | PCS1 | — | — | O | 130 | B10 |
| $\overline{CS0}$ | — | — | — | O | 129 | D10 |
| **SDRAM Controller** | | | | | | |
| $\overline{SD\_WE}$ | PSDRAM5 | — | — | O | 92 | K13 |
| $\overline{SD\_SCAS}$ | PSDRAM4 | — | — | O | 91 | K12 |
| $\overline{SD\_SRAS}$ | PSDRAM3 | — | — | O | 90 | K11 |
| SD_CKE | PSDRAM2 | — | — | O | — | E8 |
| $\overline{SD\_CS}$[1:0] | PSDRAM[1:0] | — | — | O | — | L12, L13 |

will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $V_{DD}$ to 0 V.
2. Drop $OV_{DD}/V_{DDPLL}$ supplies.

## 5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

## 5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, “Electrical Characteristics.”

## 5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

## 5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

## 5.7 Interface Recommendations

### 5.7.1 SDRAM Controller

#### 5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

**Table 3. Synchronous DRAM Signal Connections**

| Signal | Description |
|---|---|
| $\overline{\text{SD\_SRAS}}$ | Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals. |
| $\overline{\text{SD\_SCAS}}$ | Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM. |
| $\overline{\text{DRAMW}}$ | DRAM read/write. Asserted for write operations and negated for read operations. |
| $\overline{\text{SD\_CS}}$[1:0] | Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals. |
| SD_CKE | Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality. |
| $\overline{\text{BS}}$[3:0] | Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs. |
| CLKOUT | Bus clock output. Connects to the CLK input of SDRAMs. |

#### 5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

### 5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

**Table 4. MII Mode**

| Signal Description | MCF5271 Pin |
|---|---|
| Transmit clock | ETXCLK |
| Transmit enable | ETXEN |
| Transmit data | ETXD[3:0] |
| Transmit error | ETXER |
| Collision | ECOL |
| Carrier sense | ECRS |
| Receive clock | ERXCLK |
| Receive enable | ERXDV |
| Receive data | ERXD[3:0] |

**Table 4. MII Mode (continued)**

| Signal Description | MCF5271 Pin |
|---|---|
| Receive error | ERXER |
| Management channel clock | EMDC |
| Management channel serial data | EMDIO |

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5271 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

**Table 5. Seven-Wire Mode Configuration**

| Signal Description | MCF5271 Pin |
|---|---|
| Transmit clock | ETXCLK |
| Transmit enable | ETXEN |
| Transmit data | ETXD[0] |
| Collision | ECOL |
| Receive clock | ERXCLK |
| Receive enable | ERXDV |
| Receive data | ERXD[0] |
| Unused, configure as PB14 | ERXER |
| Unused input, tie to ground | ECRS |
| Unused, configure as PB[13:11] | ERXD[3:1] |
| Unused output, ignore | ETXER |
| Unused, configure as PB[10:8] | ETXD[3:1] |
| Unused, configure as PB15 | EMDC |
| Input after reset, connect to ground | EMDIO |

Refer to the M5271EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5271 site by navigating to: http://www.freescale.com/coldfire.

### 5.7.3 BDM

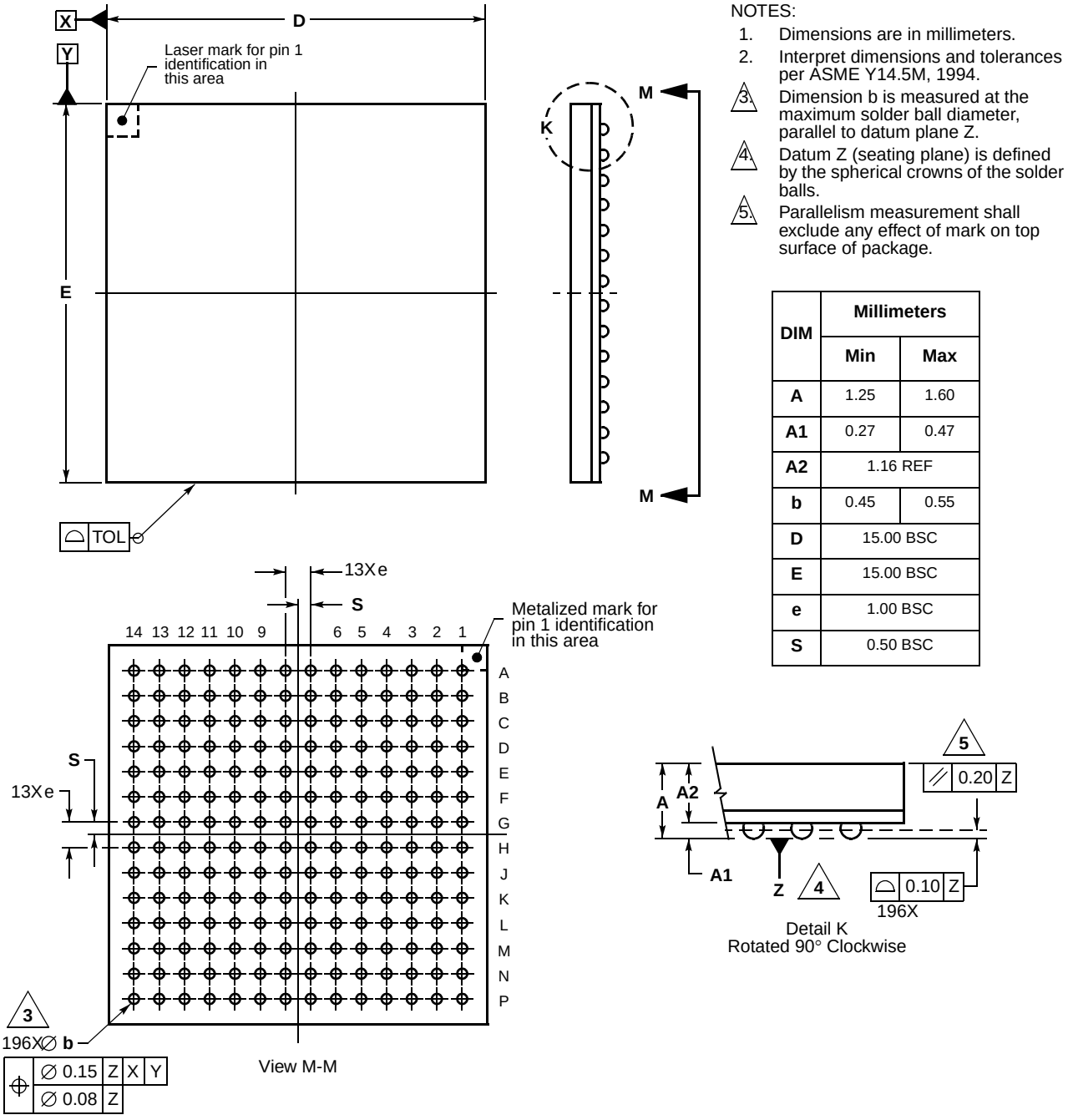
Use the BDM interface as shown in the M5271EVB evaluation board user's manual. The schematics for this board are accessible at the Freescale website at: http://www.freescale.com/coldfire.

# 6 Mechanicals/Pinouts and Part Numbers

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF5271 devices. See Table 4 for a list the signal names and pin locations for each device.

## 6.2 Package Dimensions—196 MAPBGA

Figure 4 shows MCF5270/71CVMxxx package dimensions.



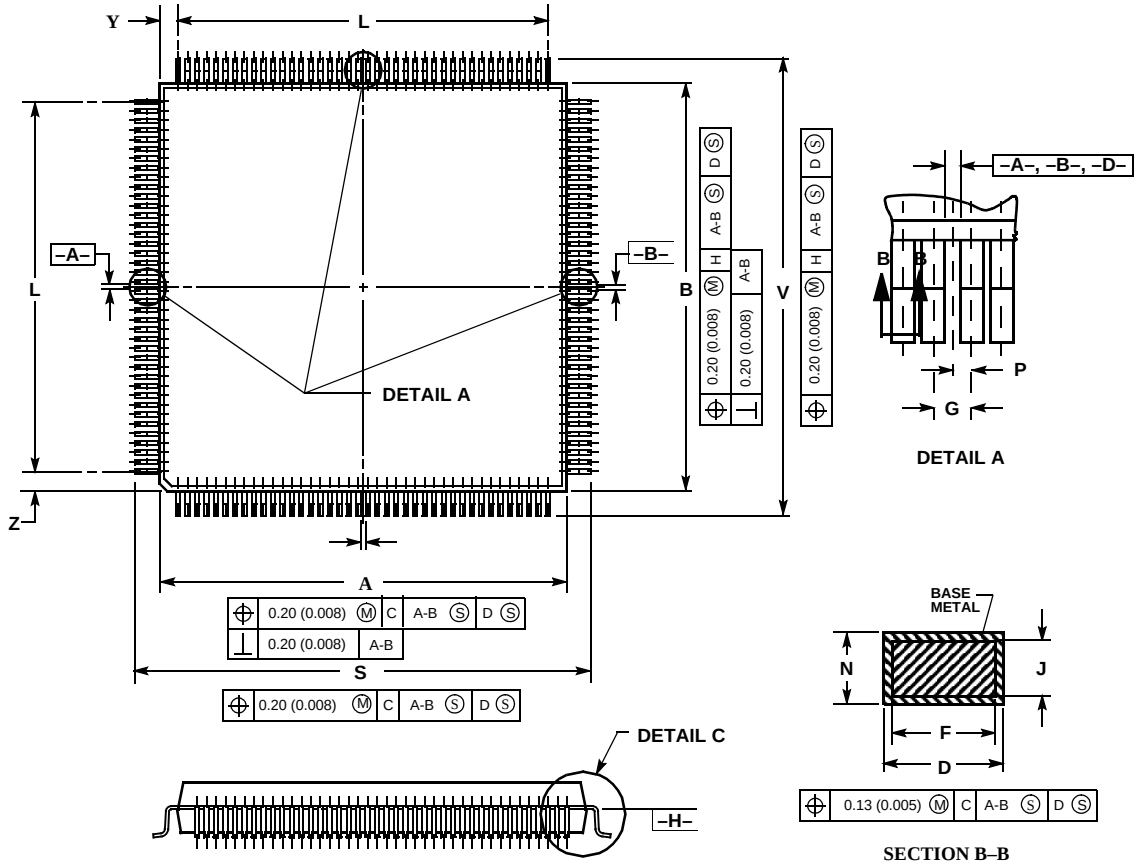

NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

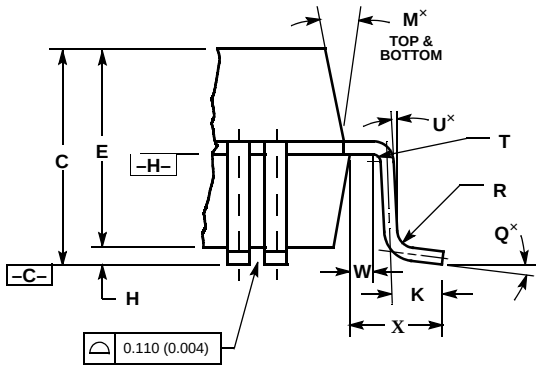
| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.25 | 1.60 |
| A1 | 0.27 | 0.47 |
| A2 | 1.16 REF | |
| b | 0.45 | 0.55 |
| D | 15.00 BSC | |
| E | 15.00 BSC | |
| e | 1.00 BSC | |
| S | 0.50 BSC | |

**Figure 4. 196 MAPBGA Package Dimensions (Case No. 1128A-01)**

## 6.4 Package Dimensions—160 QFP

Figure 6 shows MCF5270/71CAB80 package dimensions.




DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 27.90 | 28.10 | 1.098 | 1.106 |
| B | 27.90 | 28.10 | 1.098 | 1.106 |
| C | 3.35 | 3.85 | 0.132 | 1.106 |
| D | 0.22 | 0.38 | 0.009 | 0.015 |
| E | 3.20 | 3.50 | 0.126 | 0.138 |
| F | 0.22 | 0.33 | 0.009 | 0.013 |
| G | 0.65 BSC | | 0.026 REF | |
| H | 0.25 | 0.35 | 0.010 | 0.014 |
| J | 0.11 | 0.23 | 0.004 | 0.009 |
| K | 0.70 | 0.90 | 0.028 | 0.035 |
| L | 25.35 BSC | | 0.998 REF | |
| M | 5° | 16° | 5° | 16° |
| N | 0.11 | 0.19 | 0.004 | 0.007 |
| P | 0.325 BSC | | 0.013 REF | |
| Q | 0° | 7° | 0° | 7° |
| R | 0.13 | 0.30 | 0.005 | 0.012 |
| S | 31.00 | 31.40 | 1.220 | 1.236 |
| T | 0.13 | — | 0.005 | — |
| U | 0° | — | 0° | — |
| V | 31.00 | 31.40 | 1.220 | 1.236 |
| W | 0.4 | — | 0.016 | — |
| X | 1.60 REF | | 0.063 REF | |
| Y | 1.33 REF | | 0.052 REF | |
| Z | 1.33 REF | | 0.052 REF | |

**Case 864A-03**

**Figure 6. 160 QFP Package Dimensions**

## 6.5 Ordering Information

**Table 6. Orderable Part Numbers**

| Freescale Part Number | Description | Package | Speed | Lead-Free? | Temperature |
|---|---|---|---|---|---|
| MCF5270AB100 | MCF5270 RISC Microprocessor | 160 QFP | 100MHz | Yes | 0° to +70° C |
| MCF5270CAB100 | MCF5270 RISC Microprocessor | 160 QFP | 100MHz | Yes | -40° to +85° C |
| MCF5270VM100 | MCF5270 RISC Microprocessor | 196 MAPBGA | 100MHz | Yes | 0° to +70° C |
| MCF5270CVM150 | MCF5270 RISC Microprocessor | 196 MAPBGA | 150MHz | Yes | -40° to +85° C |
| MCF5271CAB100 | MCF5271 RISC Microprocessor | 160 QFP | 100MHz | Yes | -40° to +85° C |
| MCF5271CVM100 | MCF5271 RISC Microprocessor | 196 MAPBGA | 100MHz | Yes | -40° to +85° C |
| MCF5271CVM150 | MCF5271 RISC Microprocessor | 196 MAPBGA | 150MHz | Yes | -40° to +85° C |

# 7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5271 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5271.

**NOTE**

The parameters specified in this processor document supersede any values found in the module specifications.

## 7.1 Maximum Ratings

**Table 7. Absolute Maximum Ratings[1, 2]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | – 0.5 to +2.0 | V |
| Pad Supply Voltage | $OV_{DD}$ | – 0.3 to +4.0 | V |
| PLL Supply Voltage | $V_{DDPLL}$ | – 0.3 to +4.0 | V |
| Digital Input Voltage [3] | $V_{IN}$ | – 0.3 to + 4.0 | V |
| Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5] | $I_D$ | 25 | mA |
| Operating Temperature Range (Packaged) | $T_A$ ($T_L$ - $T_H$) | – 40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | – 65 to 150 | °C |

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $OV_{DD}$).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to $V_{SS}$ and $OV_{DD}$.

5 Power supply must maintain regulation within operating $OV_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $OV_{DD}$ and could result in external power supply going out of regulation. Insure external $OV_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating $OV_{DD}$ range during instantaneous and operating maximum current conditions.

## 7.2 Thermal Characteristics

The below table lists thermal resistance values.

**Table 8. Thermal Characteristics**

| Characteristic | | Symbol | 196 MAPBGA | 160QFP | Unit |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JMA}$ | 32[1,2] | 40[1,2] | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 29[1,2] | 36[1,2] | °C/W |
| Junction to board | | $\theta_{JB}$ | 20[3] | 25[3] | °C/W |
| Junction to case | | $\theta_{JC}$ | 10[4] | 10[4] | °C/W |
| Junction to top of package | | $\Psi_{jt}$ | 2[1,5] | 2[1,5] | °C/W |
| Maximum operating junction temperature | | $T_j$ | 104 | 105 | °C |

1 $\theta_{JMA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of $\theta_{JmA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

**Table 9. DC Electrical Specifications[1] (continued)**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Load Capacitance[4]<br>Low drive strength<br>High drive strength | $C_L$ | | —<br>— | 25<br>50 | pF<br>pF |
| Core Operating Supply Current [5]<br>Master Mode | $I_{DD}$ | — | 135 | 150 | mA |
| Pad Operating Supply Current<br>Master Mode<br>Low Power Modes | $OI_{DD}$ | —<br>— | 100<br>TBD | —<br>— | mA<br>µA |
| DC Injection Current [3, 6, 7, 8]<br>$V_{NEGCLAMP}$ =$V_{SS}$– 0.3 V, $V_{POSCLAMP}$ = $V_{DD}$ + 0.3<br>Single Pin Limit<br>Total processor Limit, Includes sum of all stressed pins | $I_{IC}$ | <br><br>–1.0<br>–10 | | <br><br>1.0<br>10 | <br><br>mA<br>mA |

1 Refer to Table 10 for additional PLL specifications.
2 Refer to the MCF5271 signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.
4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.
5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
6 All functional non-supply pins are internally clamped to $V_{SS}$ and their respective $V_{DD}$.
7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Insure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

## 7.4 Oscillator and PLLMRFM Electrical Characteristics

**Table 10. HiP7 PLLMRFM Electrical Specifications[1]**

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|---|---|---|---|---|---|
| 1 | PLL Reference Frequency Range<br>Crystal reference<br>External reference<br>1:1 mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$) | <br>$f_{ref\_crystal}$<br>$f_{ref\_ext}$<br>$f_{ref\_1:1}$ | <br>8<br>8<br>24 | <br>25<br>25<br>75 | MHz |
| 2 | Core frequency<br>CLKOUT Frequency [2]<br>External reference<br>On-Chip PLL Frequency | $f_{sys}$<br><br>$f_{sys/2}$ | <br>0<br>$f_{ref} \div 32$ | 150<br>75<br>75 | MHz<br>MHz<br>MHz |
| 3 | Loss of Reference Frequency [3, 5] | $f_{LOR}$ | 100 | 1000 | kHz |
| 4 | Self Clocked Mode Frequency [4, 5] | $f_{SCM}$ | 10.25 | 15.25 | MHz |
| 5 | Crystal Start-up Time [5, 6] | $t_{cst}$ | — | 10 | ms |

Read/write bus timings listed in Table 12 are shown in Figure 8, Figure 9, and Figure 10.

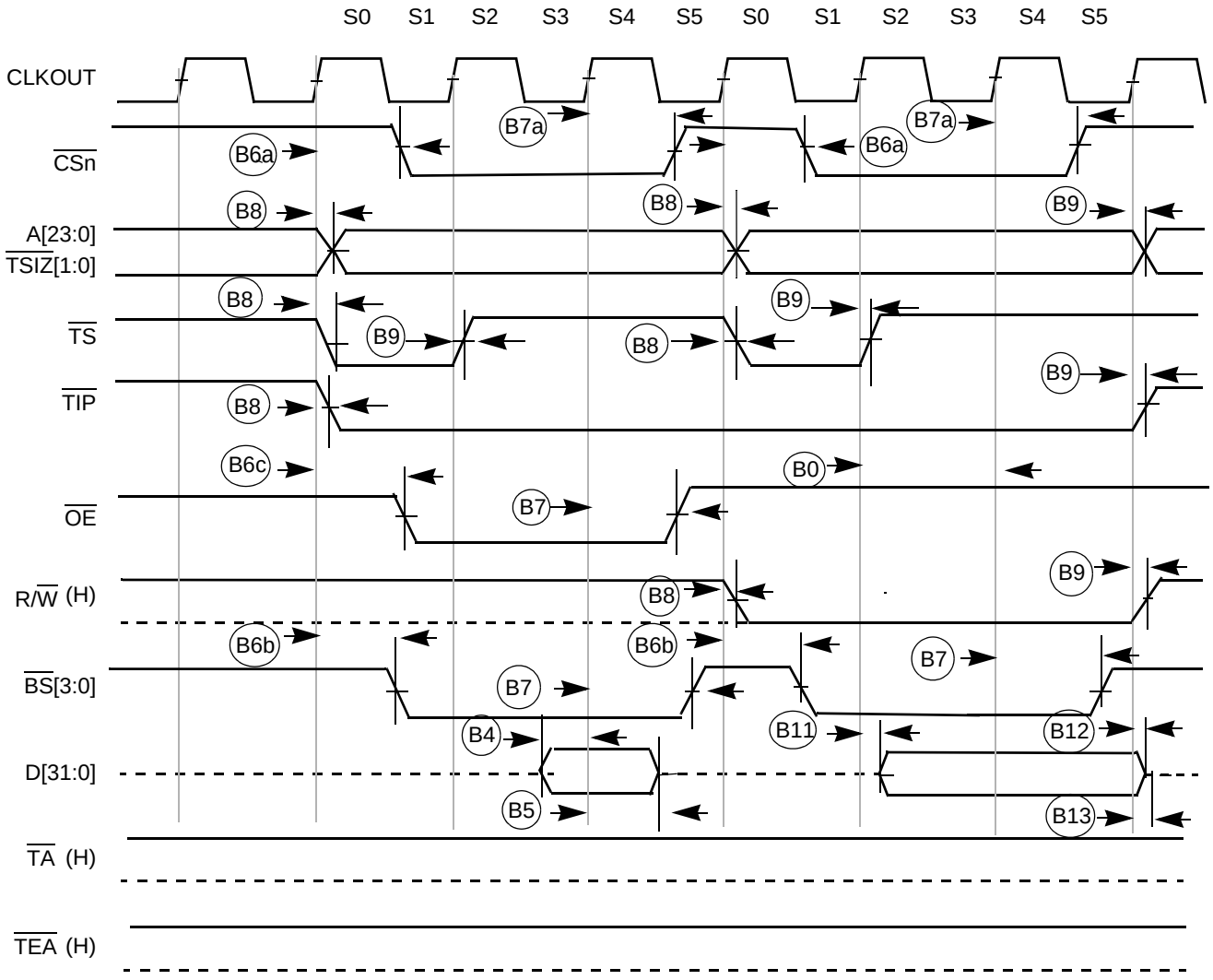



**Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing**

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

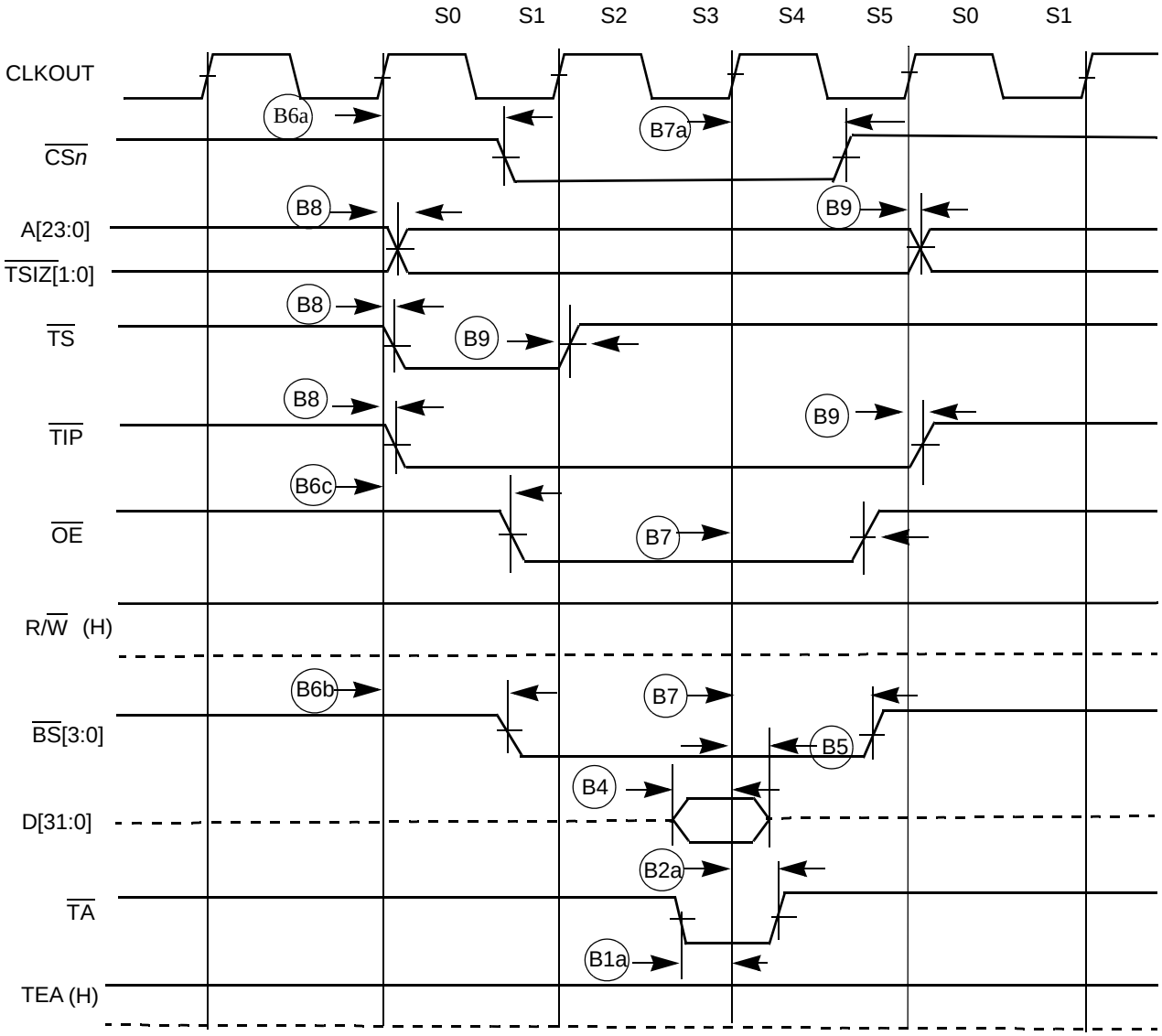



**Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$**

Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

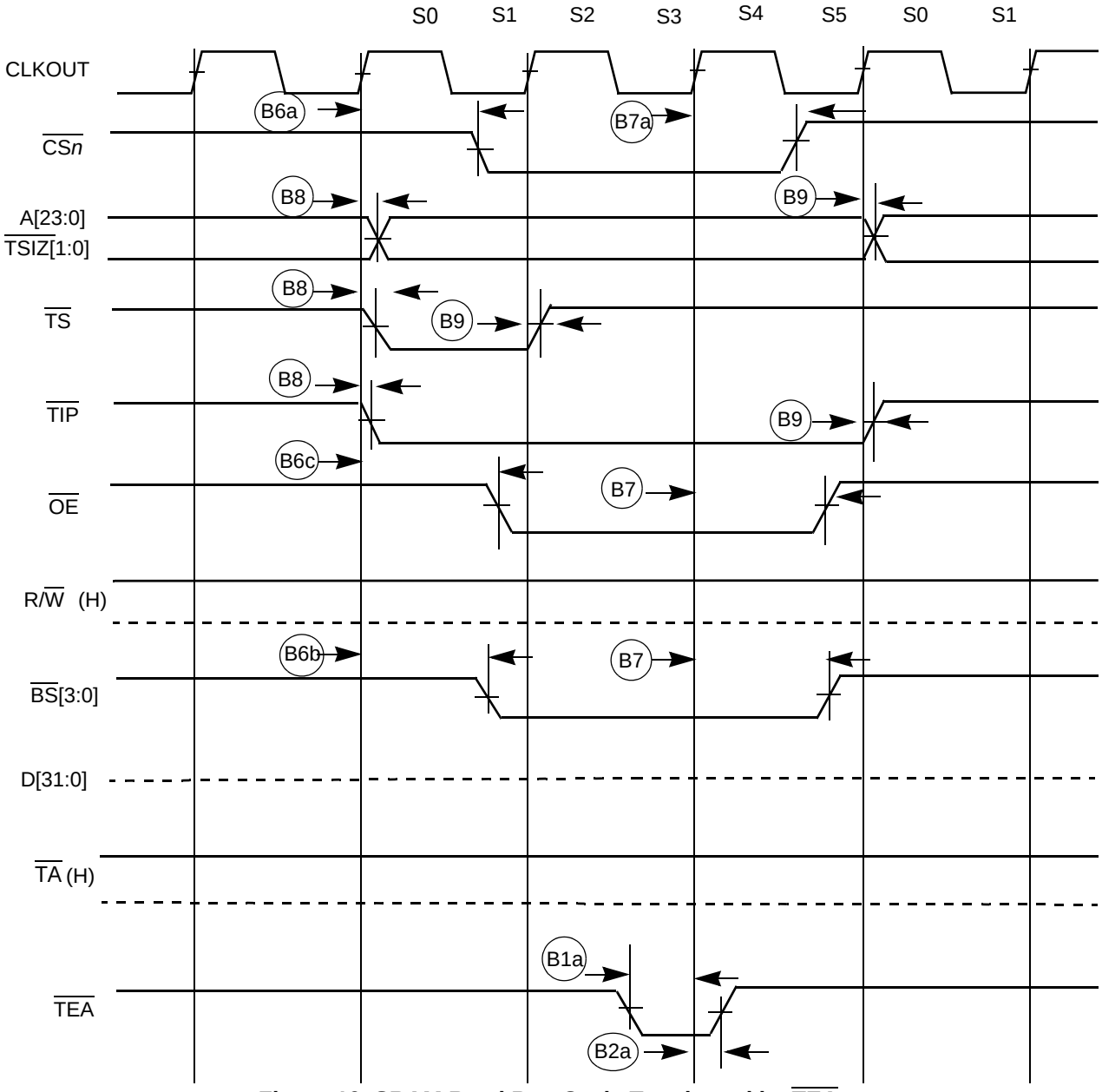



**Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$**

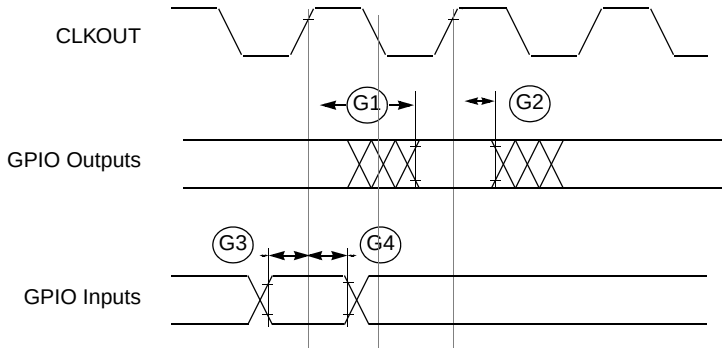



**Figure 13. GPIO Timing**

## 7.8 Reset and Configuration Override Timing

**Table 15. Reset and Configuration Override Timing**
**($V_{DD}$ = 2.7 to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = $T_L$ to $T_H$)[1]**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| R1 | $\overline{\text{RESET}}$ Input valid to CLKOUT High | $t_{RVCH}$ | 9 | — | ns |
| R2 | CLKOUT High to $\overline{\text{RESET}}$ Input invalid | $t_{CHRI}$ | 1.5 | — | ns |
| R3 | $\overline{\text{RESET}}$ Input valid Time [2] | $t_{RIVT}$ | 5 | — | $t_{CYC}$ |
| R4 | CLKOUT High to $\overline{\text{RSTOUT}}$ Valid | $t_{CHROV}$ | — | 10 | ns |
| R5 | $\overline{\text{RSTOUT}}$ valid to Config. Overrides valid | $t_{ROVCV}$ | 0 | — | ns |
| R6 | Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid | $t_{COS}$ | 20 | — | $t_{CYC}$ |
| R7 | Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid | $t_{COH}$ | 0 | — | ns |
| R8 | $\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance | $t_{ROICZ}$ | — | 1 | $t_{CYC}$ |

1 All AC timing is shown with respect to 50% $V_{DD}$ levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

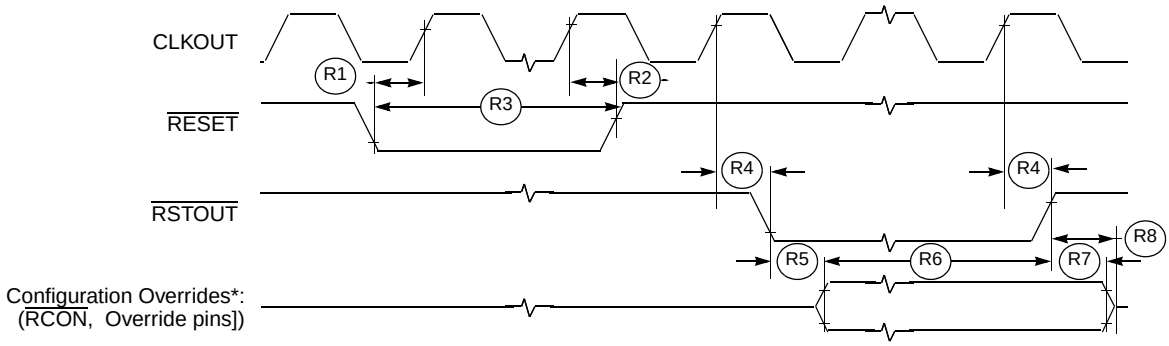



**Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing**

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

## 7.9 I²C Input/Output Timing Specifications

Table 16 lists specifications for the I²C input timing parameters shown in Figure 15.

**Table 16. I²C Input Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1 | Start condition hold time | 2 | — | $t_{cyc}$ |
| I2 | Clock low period | 8 | — | $t_{cyc}$ |
| I3 | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | 4 | — | $t_{cyc}$ |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | 2 | — | $t_{cyc}$ |
| I9 | Stop condition setup time | 2 | — | $t_{cyc}$ |

Table 17 lists specifications for the I²C output timing parameters shown in Figure 15.

**Table 17. I²C Output Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1[1] | Start condition hold time | 6 | — | $t_{cyc}$ |
| I2 [1] | Clock low period | 10 | — | $t_{cyc}$ |
| I3 [2] | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | — | µs |
| I4 [1] | Data hold time | 7 | — | $t_{cyc}$ |
| I5 [3] | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 3 | ns |
| I6 [1] | Clock high time | 10 | — | $t_{cyc}$ |
| I7 [1] | Data setup time | 2 | — | $t_{cyc}$ |
| I8 [1] | Start condition setup time (for repeated start condition only) | 20 | — | $t_{cyc}$ |
| I9 [1] | Stop condition setup time | 10 | — | $t_{cyc}$ |

1 Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 15 shows timing for the values in Table 16 and Table 17.

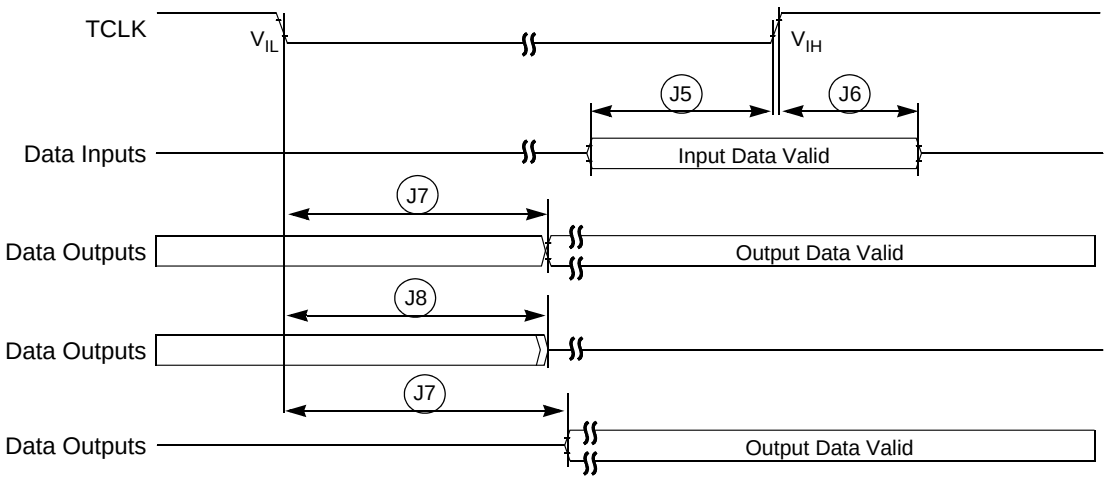



**Figure 22. Boundary Scan (JTAG) Timing**

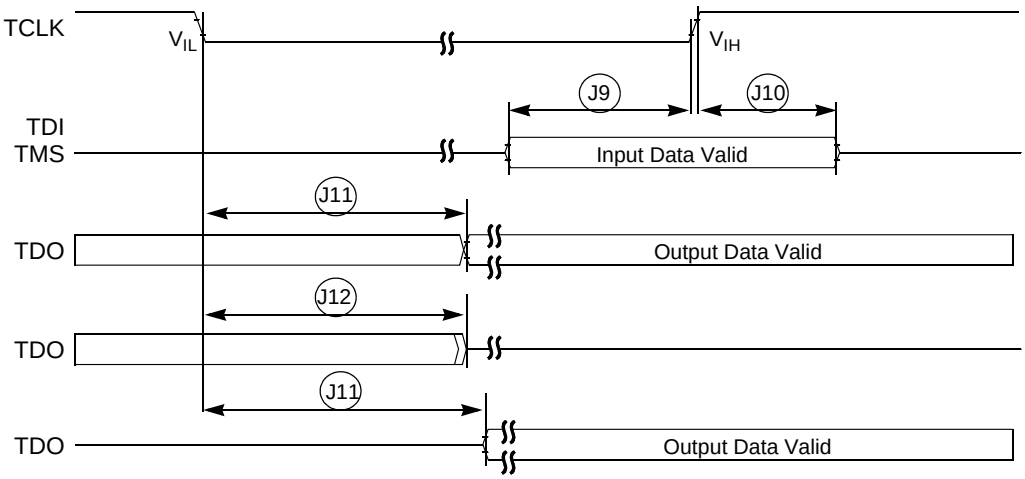



**Figure 23. Test Access Port Timing**

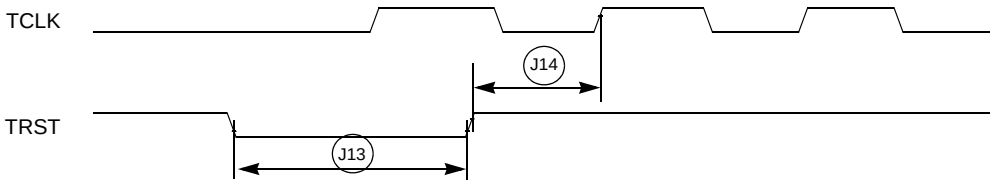



**Figure 24. $\overline{\text{TRST}}$ Timing**

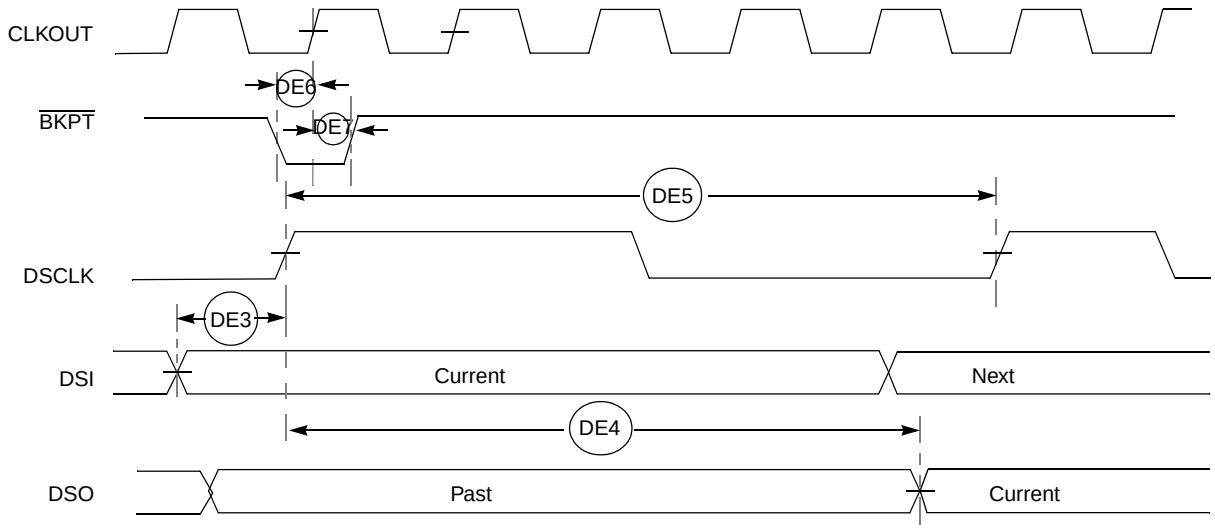



**Figure 26. BDM Serial Port AC Timing**

# 8 Documentation

Documentation regarding the MCF5271 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

# 9 Document Revision History

The below table provides a revision history for this document.

**Table 26. MCF5271EC Revision History**

| Rev. No. | Substantive Change(s) |
|---|---|
| 0 | Initial release |
| 1 | • Fixed several clock values.<br>• Updated Signal List table |
| 1.1 | • Removed duplicate information in the module description sections. The information is all in the Signals Description Table. |
| 1.2 | • Removed detailed signal description section. This information can be found in the MCF5271RM Chapter 2.<br>• Removed detailed feature list. This information can be found in the MCF5271RM Chapter 1.<br>• Changed instances of Motorola to Freescale<br>• Added values for ‘Maximum operating junction temperature’ in Table 8.<br>• Added typical values for ‘Core operating supply current (master mode)’ in Table 9.<br>• Added typical values for ‘Pad operating supply current (master mode)’ in Table 9.<br>• Removed unnecessary PLL specifications, #6-9, in Table 10. |

**Table 26. MCF5271EC Revision History (continued)**

| Rev. No. | Substantive Change(s) |
|---|---|
| 1.3 | • Device is now available in 150 MHz versions. Updated specs where necessary to reflect this improvement.<br>• Added 2 new part numbers to Table 6: MCF5270CVM150 and MCF5271CVM150.<br>• Removed features list. This information can be found in the MCF5271RM.<br>• Removed SDRAM address multiplexing section. This information can be found in the MCF5271RM. |
| 1.4 | • Added Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions.”<br>• Updated 196MAPBGA package dimensions, Figure 4. |
| 2 | • Table 2: Changed SD_CKE pin location from 139 to “—” for the 160QFP device.<br>• Table 2: Changed QSPI_CS1 pin location from “—” to 139 for the 160QFP device.<br>• Table 2: Changed DT3IN pin’s alternate 2 function from “—” to QSPI_CS2.<br>• Table 2: Changed DT3OUT pin’s alternate 2 function from “—” to QSPI_CS3.<br>• Figure 5: Changed pin 139 label from “SD_CKE/QSPI_CS1” to “QSPI_CS1/SD_CKE”.<br>• Removed second sentence from Section 7.10.1, “MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK),” and Section 7.10.2, “MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK),” regarding no minimum frequency requirement for TXCLK.<br>• Removed third and fourth paragraphs from Section 7.10.2, “MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK),” as this feature is not supported on this device. |
| 3 | • Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions” changed $PLLV_{DD}$ to $V_{DDPLL}$ to match rest of document.<br>• Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions” Changed $V_{DDPLL}$ voltage level from 1.5V to 3.3V throughout section.<br>• Section 5.2.1.1, “Power Up Sequence” first bullet, changed “Use 1 µs” to “Use 1 ms”.<br>• Corrected position of spec D5 in Figure 11.<br>• Figure 3: Corrected M4 ball location from DATA5 to DATA6, changed DATA*n* labels to D*n* for consistency<br>• Table 14: Added $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$ to footnote.<br>• Table 9, added PLL supply voltage row |
| 4 | • Added part number MCF5270CAB100 in Table 6 |