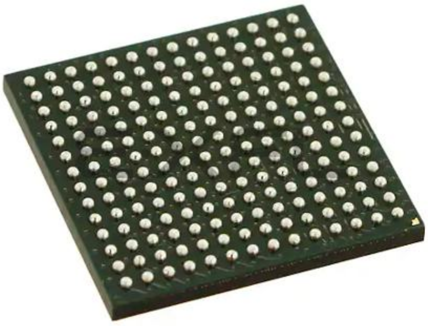

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5270cvm150

1 MCF5271 Family Configurations

Table 1. MCF5271 Family Configurations

Module	MCF5270	MCF5271
ColdFire V2 Core with EMAC and Hardware Divide	x	x
System Clock	150 MHz	
Performance (Dhrystone/2.1 MIPS)	144	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	64 Kbytes	
Interrupt Controllers (INTC)	2	2
Edge Port Module (EPORT)	x	x
External Interface Module (EIM)	x	x
4-channel Direct-Memory Access (DMA)	x	x
SDRAM Controller	x	x
Fast Ethernet Controller (FEC)	x	x
Hardware Encryption	—	x
Watchdog Timer (WDT)	x	x
Four Periodic Interrupt Timers (PIT)	x	x
32-bit DMA Timers	4	4
QSPI	x	x
UART(s)	3	3
I^2C	x	x
General Purpose I/O Module (GPIO)	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x
Package	160 QFP, 196 MAPBGA	160 QFP, 196 MAPBGA

2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array plastic ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

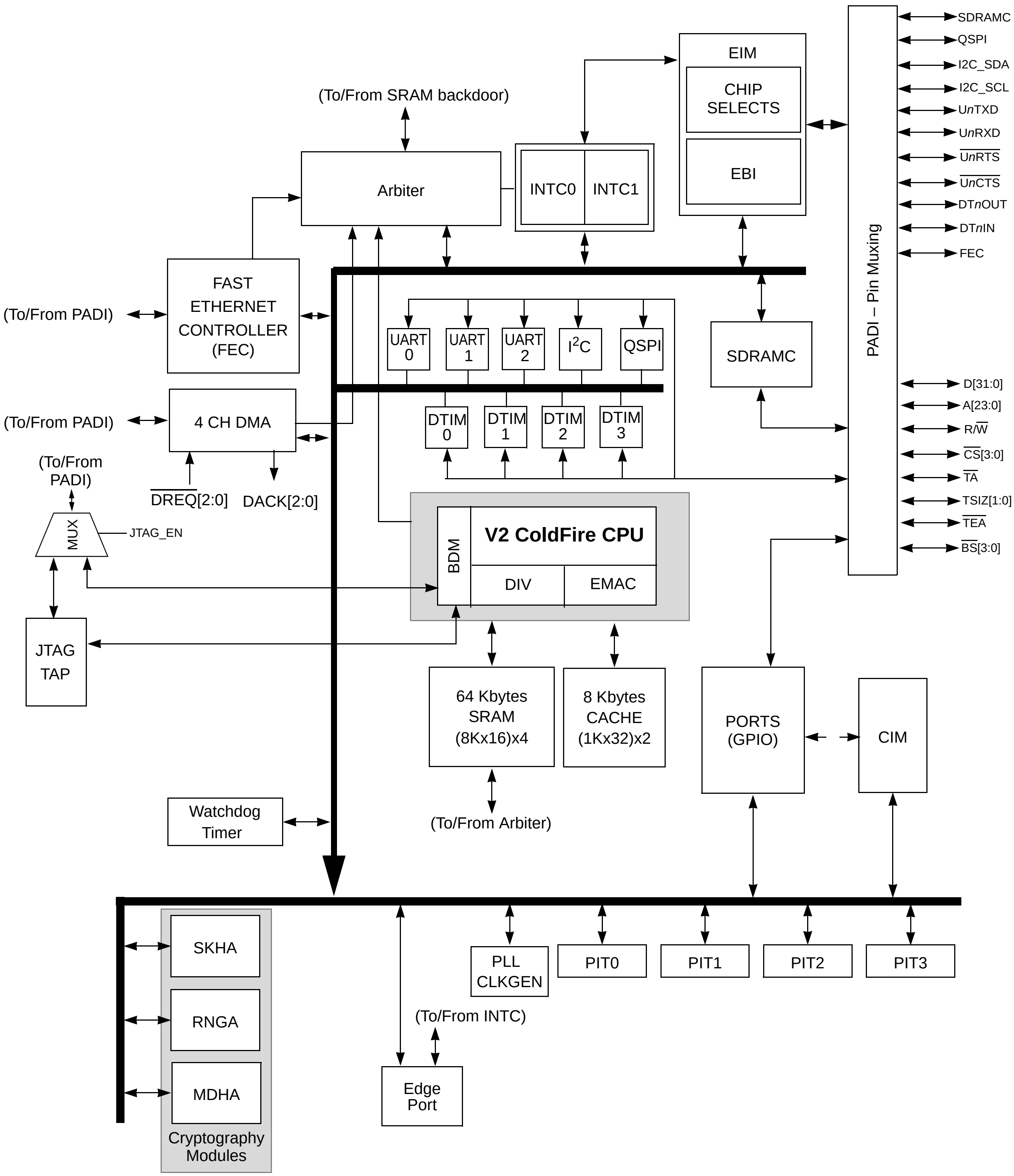


Figure 1. MCF5271 Block Diagram

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

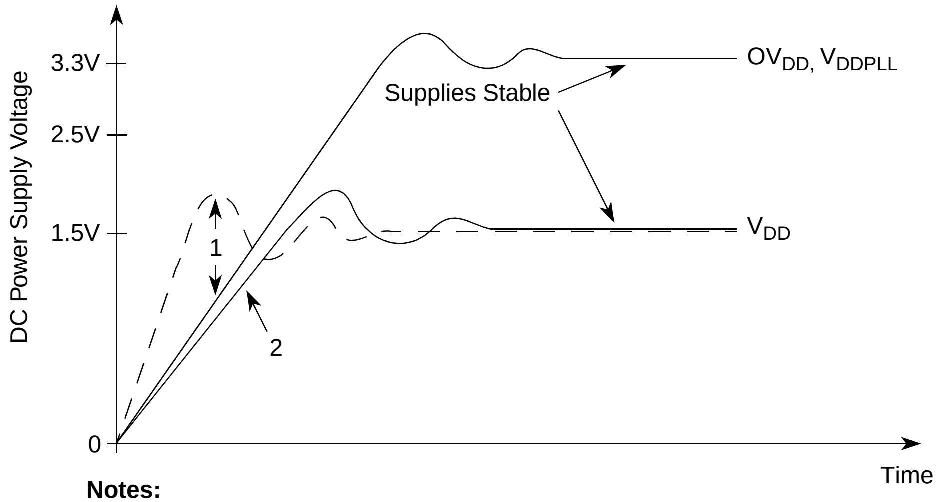
Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
A[20:0]	—	—	—	O	123:115, 112:106, 102:98	A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13
D[31:16]	—	—	—	O	22:30, 33:39	G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2
D[15:8]	PDATAH[7:0]	—	—	O	42:49	M1, N1, M2, N2, P2, L3, M3, N3
D[7:0]	PDATAL[7:0]	—	—	O	50:52, 56:60	P3, M4, N4, P4, L5, M5, N5, P5
$\overline{\mathrm{BS}}$[3:0]	PBS[7:4]	$\overline{\mathrm{CAS}}$[3:0]	—	O	143:140	B6, C6, D7, C7
$\overline{\mathrm{OE}}$	PBUSCTL7	—	—	O	62	N6
$\overline{\mathrm{TA}}$	PBUSCTL6	—	—	I	96	H11
$\overline{\mathrm{TEA}}$	PBUSCTL5	$\overline{\mathrm{DREQ1}}$	—	I	—	J14
R/$\overline{\mathrm{W}}$	PBUSCTL4	—	—	O	95	J13
$\overline{\mathrm{TSIZ1}}$	PBUSCTL3	DACK1	—	O	—	P6
$\overline{\mathrm{TSIZ0}}$	PBUSCTL2	DACK0	—	O	—	P7
$\overline{\mathrm{TS}}$	PBUSCTL1	DACK2	—	O	97	H13
$\overline{\mathrm{TIP}}$	PBUSCTL0	DREQ0	—	O	—	H12
Chip Selects						
$\overline{\mathrm{CS}}$[7:4]	PCS[7:4]	—	—	O	—	B9, A10, C10, A11
$\overline{\mathrm{CS}}$[3:2]	PCS[3:2]	SD_CS[1:0]	—	O	132,131	A9, C9
$\overline{\mathrm{CS1}}$	PCS1	—	—	O	130	B10
$\overline{\mathrm{CS0}}$	—	—	—	O	129	D10
SDRAM Controller						
$\overline{\mathrm{SD\_WE}}$	PSDRAM5	—	—	O	92	K13
$\overline{\mathrm{SD\_SCAS}}$	PSDRAM4	—	—	O	91	K12
$\overline{\mathrm{SD\_SRAS}}$	PSDRAM3	—	—	O	90	K11
SD_CKE	PSDRAM2	—	—	O	—	E8
$\overline{\mathrm{SD\_CS}}$[1:0]	PSDRAM[1:0]	—	—	O	—	L12, L13

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
External Interrupts Port						
$\overline{\text{IRQ}}$[7:3]	PIRQ[7:3]	—	—	I	IRQ7=63 IRQ4=64	N7, M7, L7, P8, N8
$\overline{\text{IRQ2}}$	PIRQ2	$\overline{\text{DREQ2}}$	—	I	—	M8
$\overline{\text{IRQ1}}$	PIRQ1	—	—	I	65	L8
FEC						
EMDC	PFECI2C3	I2C_SCL	U2TXD	O	151	D4
EMDIO	PFECI2C2	I2C_SDA	U2RXD	I/O	150	D5
ECOL	—	—	—	I	9	E2
ECRS	—	—	—	I	8	E1
ERXCLK	—	—	—	I	7	D1
ERXDV	—	—	—	I	6	D2
ERXD[3:0]	—	—	—	I	5:2	D3, C1, C2, B1
ERXER	—	—	—	O	159	B2
ETXCLK	—	—	—	I	158	A2
ETXEN	—	—	—	I	157	C3
ETXER	—	—	—	O	156	B3
ETXD[3:0]	—	—	—	O	155:152	A3, A4, C4, B4
I^2C						
I2C_SDA	PFECI2C1	—	—	I/O	—	J12
I2C_SCL	PFECI2C0	—	—	I/O	—	J11
DMA						
DACK[2:0] and $\overline{\text{DREQ}}$[2:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and DT2OUT for DACK2, $\overline{\text{TSIZ1}}$and DT1OUT for DACK1, TSIZ0 and DT0OUT for DACK0, $\overline{\text{IRQ2}}$ and DT2IN for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ and $\overline{\text{DT1IN}}$ for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ and DT0IN for $\overline{\text{DREQ0}}$.					—	—
QSPI						
QSPI_CS1	PQSPI4	SD_CKE	—	O	139	B7
QSPI_CS0	PQSPI3	—	—	O	146	A6
QSPI_CLK	PQSPI2	I2C_SCL	—	O	147	C5
QSPI_DIN	PQSPI1	I2C_SDA	—	I	148	B5
QSPI_DOUT	PQSPI0	—	—	O	149	A5

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}/V_{DDPLL} must power down. V_{DD} should not lag OV_{DD} or V_{DDPLL} going low by more than 0.4 V during power down or there

6.1 Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5270/71CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	ETXCLK	ETXD3	ETXD2	QSPI_DOUT	QSPI_CS0	U2RXD	U2TXD	CS3	CS6	CS4	A20	A17	VSS	A
B	ERXD0	ERXER	ETXER	ETXD0	QSPI_DIN	BS3	QSPI_CS1	U1CTS	CS7	CS1	A23	A19	A16	A15	B
C	ERXD2	ERXD1	ETXEN	ETXD1	QSCK	BS2	BS0	RTS1	CS2	CS5	A22	A18	A14	A13	C
D	ERXCLK	ERXDV	ERXD3	EMDC	EMDIO	Core VDD_4	BS1	U1RXD1	U1TXD	CS0	A21	A12	A11	A10	D
E	ECRS	ECOL	NC	TIN0	VDD	VSS	VDD	SD_CKE	VSS	VDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	U0CTS	DTOUT0	TEST	VSS	VDD	VSS	VDD	VSS	Core VDD_3	A5	A4	A3	F
G	D31	D30	U0RTS	Core VDD_1	CLK MOD1	VDD	VSS	VDD	VSS	NC	A2	A1	A0	DTOUT3	G
H	D29	D28	D27	D26	CLK MOD0	VSS	VDD	VDD	VDD	NC	TA	TIP	TS	DTIN3	H
J	D25	D24	D23	D22	VSS	VDD	VSS	VDD	VSS	VDD	I2C_SCL	I2C_SDA	R/W	TEA	J
K	D21	D20	D19	D18	VDD	VDD	VSS	VDD	JTAG_EN	RCON	SD_RAS	SD_CAS	SD_WE	CLKOUT	K
L	D17	D16	D10	Core VDD_2	D3	DTIN1	IRQ5	IRQ1	DTOUT2	PST0	DDATA0	SD_CS1	SD_CS0	VSSPLL	L
M	D15	D13	D9	D6	D2	DTOUT1	IRQ6	IRQ2	DTIN2	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	OE	IRQ7	IRQ3	TRST/ DSCLK	TDO/DSO	PST2	DDATA2	RESET	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	IRQ4	TCLK/ PSTCLK	TMS/ BKPT	PST1	DDATA1	RSTOUT	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3. MCF5270/71CVMxxx Pinout (196 MAPBGA)

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).
3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4 All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.
5 Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2 Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	104	105	^oC

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2 Per JEDEC JESD51-6 with the board horizontal.
3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A= Ambient Temperature, °C

Θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^{\ 2} \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.3 DC Electrical Specifications

Table 9. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Typical	Max	Unit
Core Supply Voltage	V_{DD}	1.4	—	1.6	V
Pad Supply Voltage	OV_{DD}	3.0	—	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	—	3.6	V
Input High Voltage	V_{IH}	$0.7 \times OV_{DD}$	—	3.65	V
Input Low Voltage	V_{IL}	$V_{SS} – 0.3$	—	$0.35 \times OV_{DD}$	V
Input Hysteresis	V_{HYS}	$0.06 \times OV_{DD}$	—	—	mV
Input Leakage Current $V_{in} = V_{DD}$ or V_{SS}, Input-only pins	I_{in}	–1.0	—	1.0	µA
High Impedance (Off-State) Leakage Current $V_{in} = V_{DD}$ or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	—	1.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	OV_{DD} - 0.5	—	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	–10	—	– 130	µA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	—	 7 7	pF

Timings listed in Table 11 are shown in Figure 7.

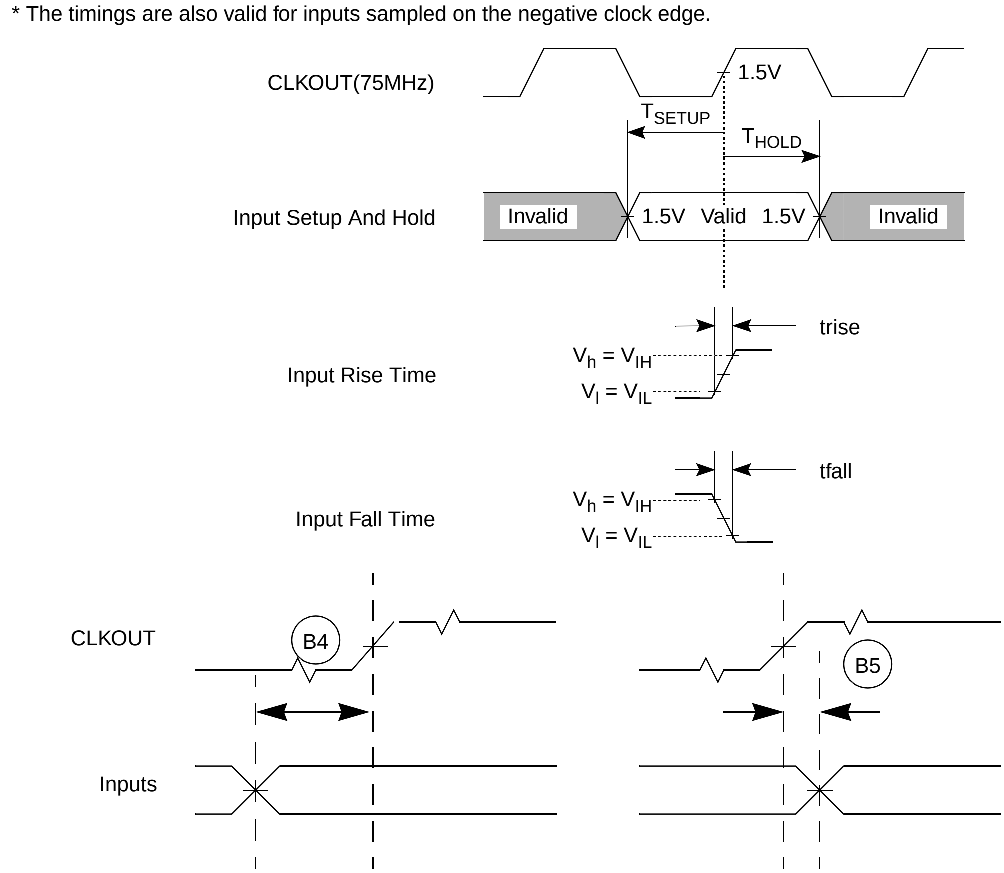


Figure 7. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{\text{TS}}$, $\overline{\text{TSIZ}}$[1:0], $\overline{\text{TIP}}$, R/$\overline{\text{W}}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{\text{TS}}$, $\overline{\text{TSIZ}}$[1:0], $\overline{\text{TIP}}$, R/$\overline{\text{W}}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

[1] $\overline{\text{CS}}$ transitions after the falling edge of CLKOUT.
[2] $\overline{\text{BS}}$ transitions after the falling edge of CLKOUT.
[3] $\overline{\text{OE}}$ transitions after the falling edge of CLKOUT.

Figure 9 shows a bus cycle terminated by $\overline{\text{TA}}$ showing timings listed in Table 12.

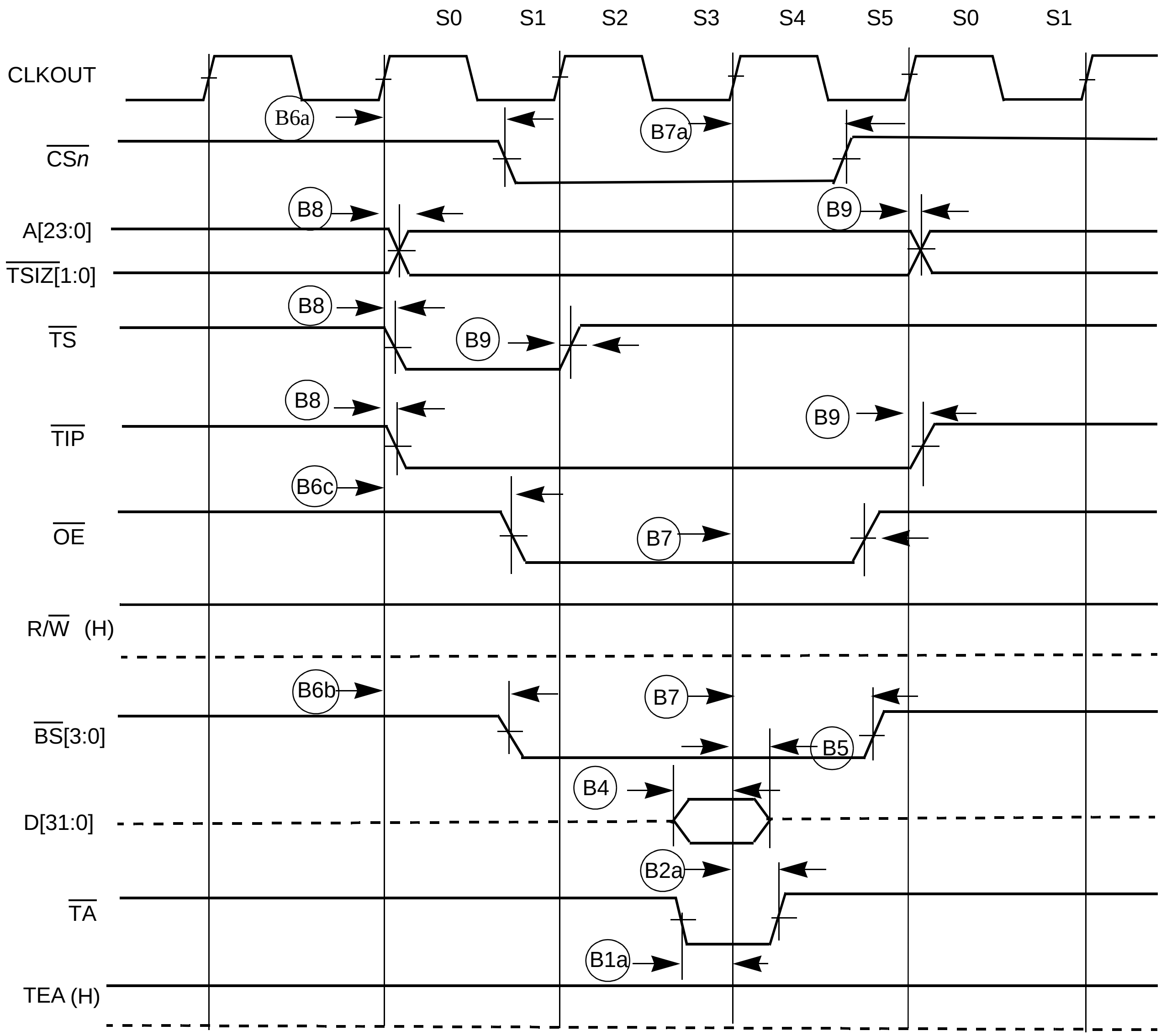


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{\text{TA}}$

Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

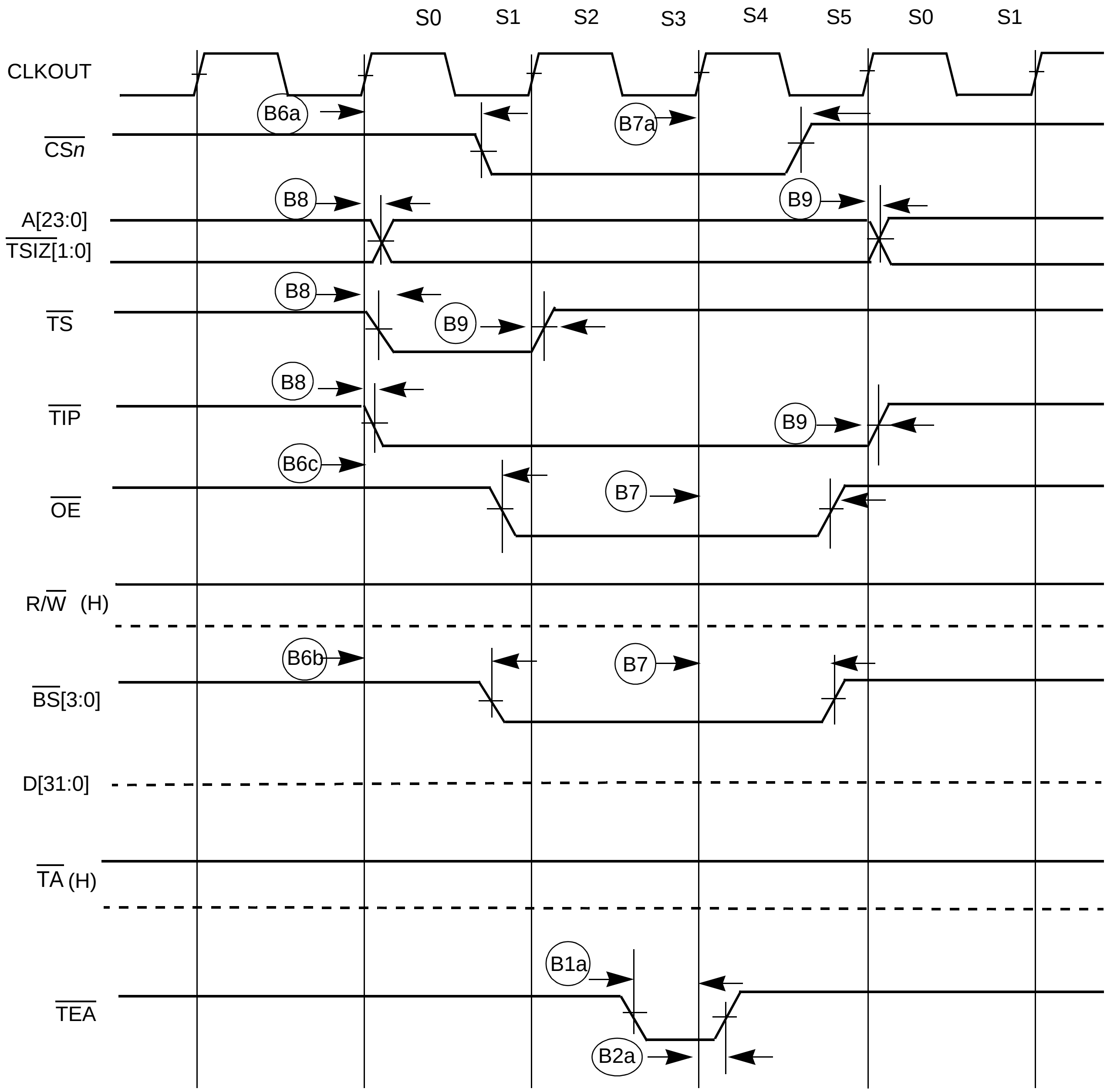
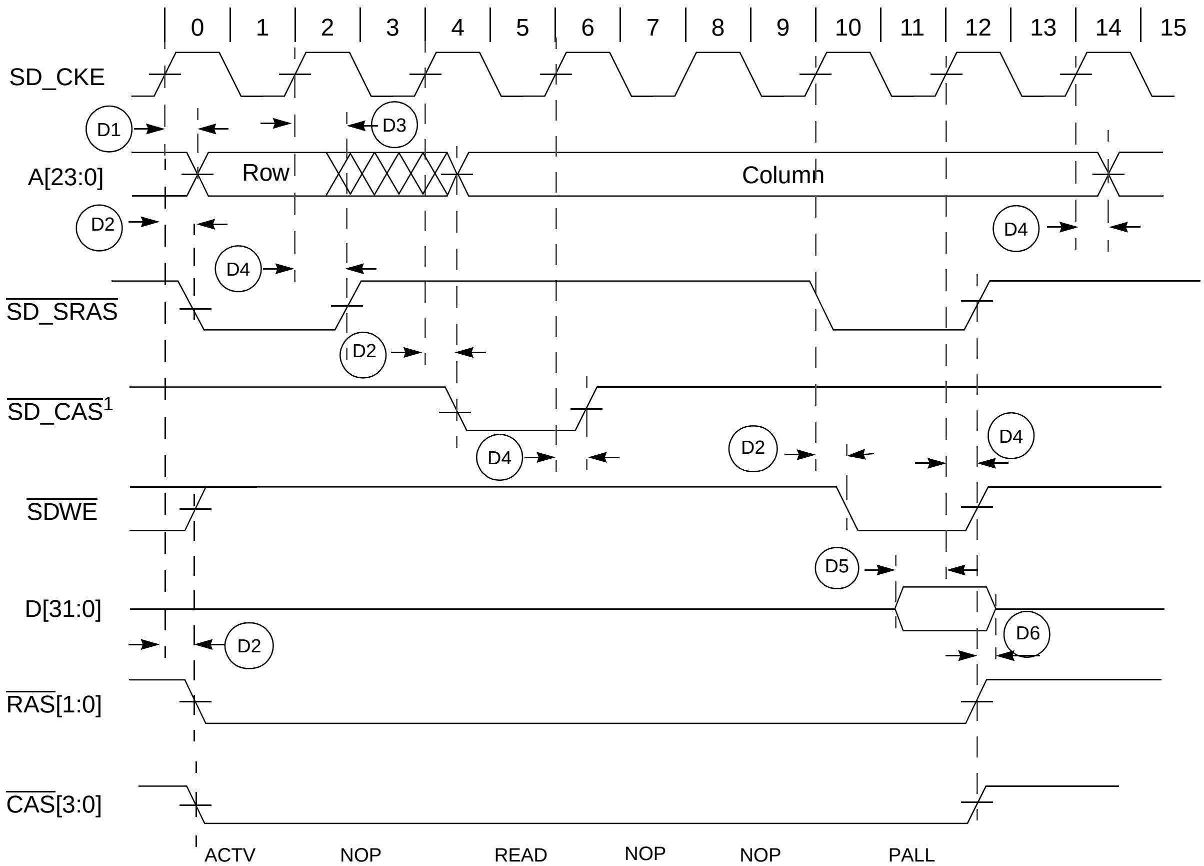


Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$

Figure 11 shows an SDRAM read cycle.



[1] DACR[CASL] = 2

Figure 11. SDRAM Read Cycle

Table 13. SDRAM Timing

NUM	Characteristic	Symbol	Min	Max	Unit
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}	—	9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.5	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.5	—	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	4	—	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.5	—	ns
D7[1]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	—	9	ns
D8[1]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.5	—	ns

[1] D7 and D8 are for write cycles only.

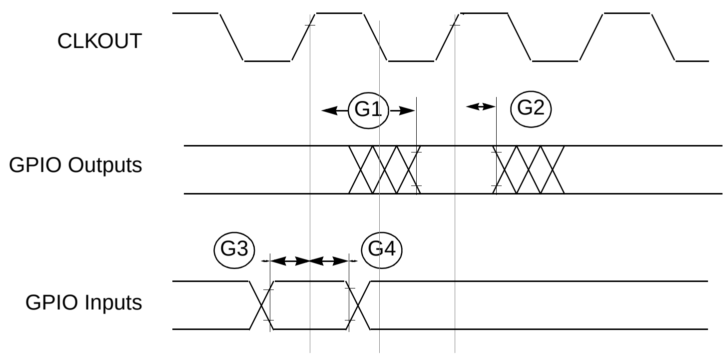


Figure 13. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

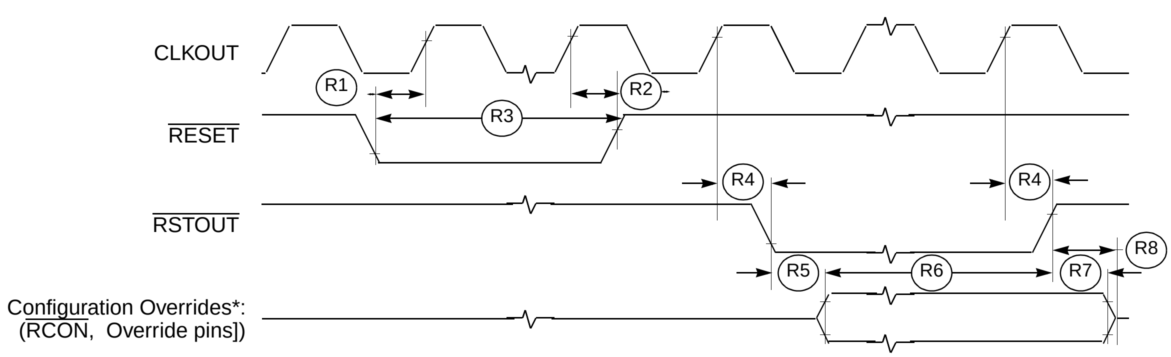


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

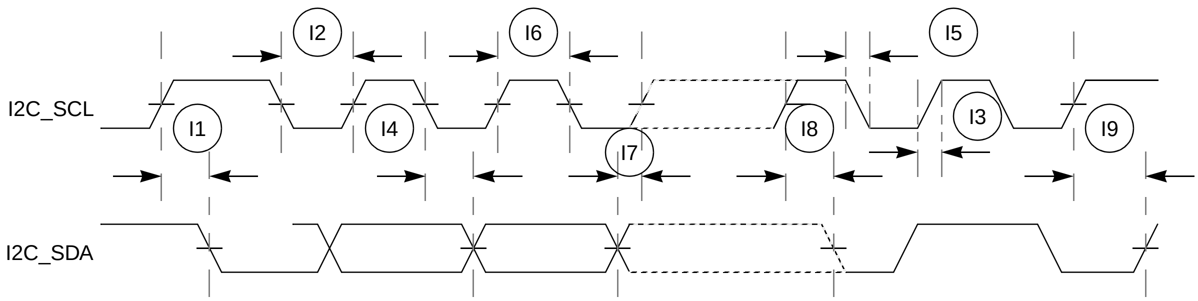


Figure 15. I²C Input/Output Timings

7.10 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

7.10.1 MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)

The receiver functions correctly up to a ERXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ERXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	ERXD[3:0], ERXDV, ERXER to ERXCLK setup	5	—	ns
M2	ERXCLK to ERXD[3:0], ERXDV, ERXER hold	5	—	ns
M3	ERXCLK pulse width high	35%	65%	ERXCLK period
M4	ERXCLK pulse width low	35%	65%	ERXCLK period

Figure 16 shows MII receive signal timings listed in Table 18.

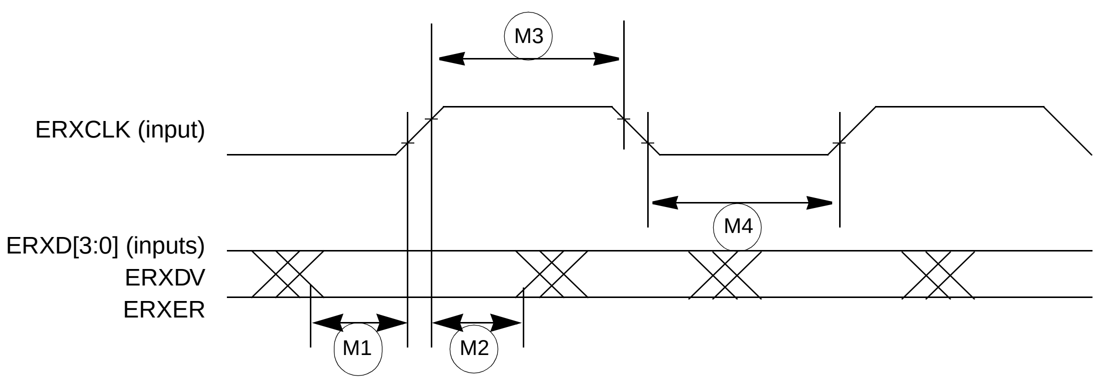


Figure 16. MII Receive Signal Timing Diagram

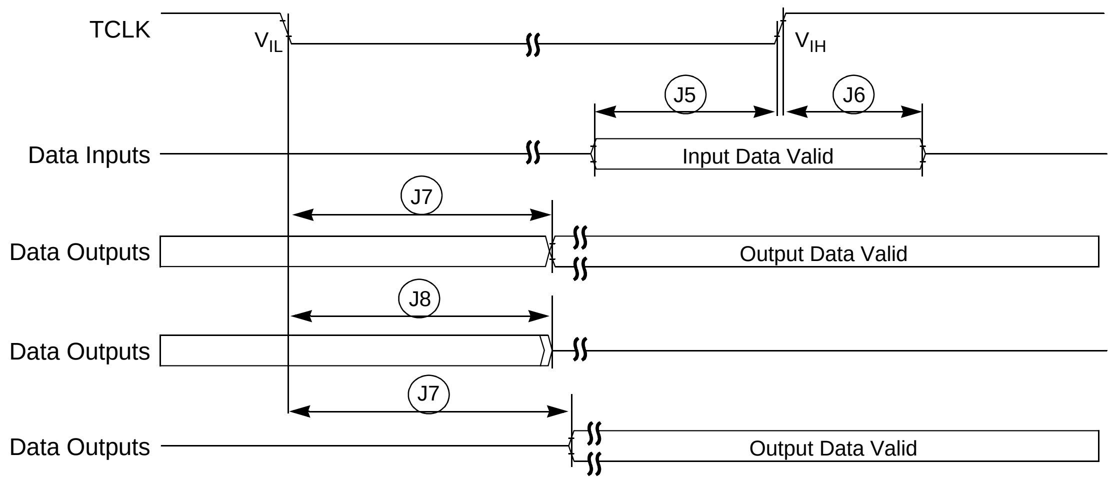


Figure 22. Boundary Scan (JTAG) Timing

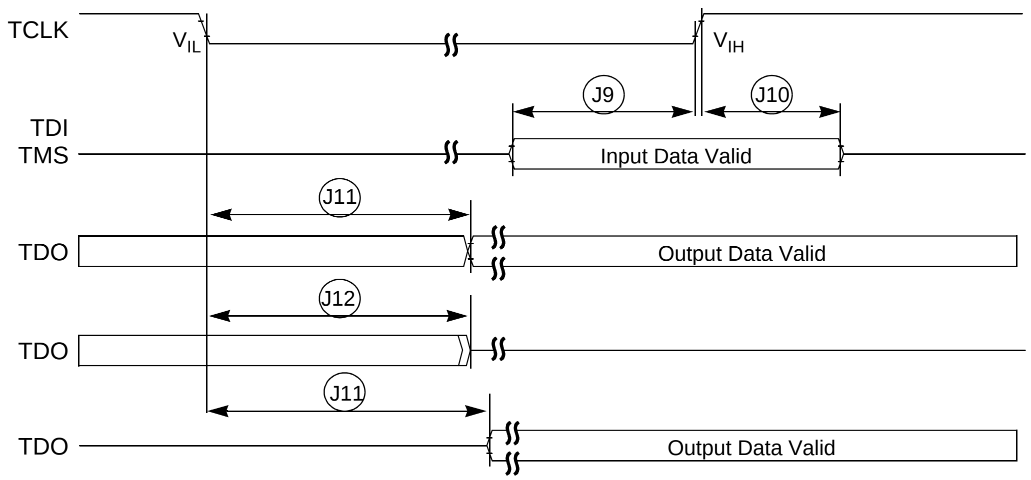


Figure 23. Test Access Port Timing

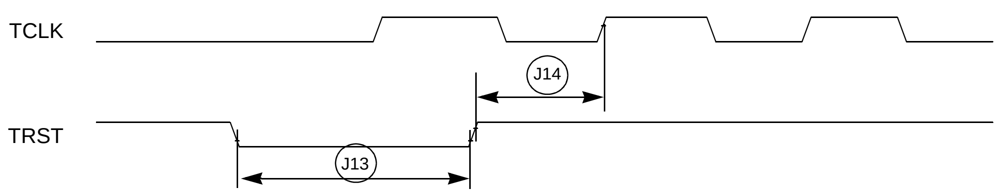


Figure 24. $\overline{\text{TRST}}$ Timing

7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 26.

Table 25. Debug AC Timing Specification

Num	Characteristic	150 MHz		Units
		Min	Max	
DE0	PSTCLK cycle time	—	0.5	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
DE7	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0	10	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 25 shows real-time trace timing for the values in Table 25.

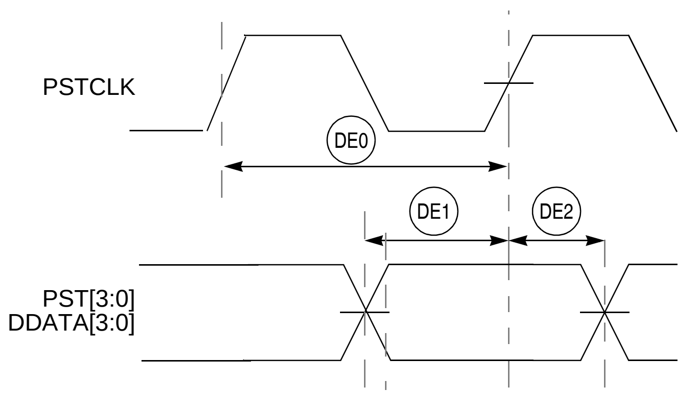


Figure 25. Real-Time Trace AC Timing

Figure 26 shows BDM serial port AC timing for the values in Table 25.

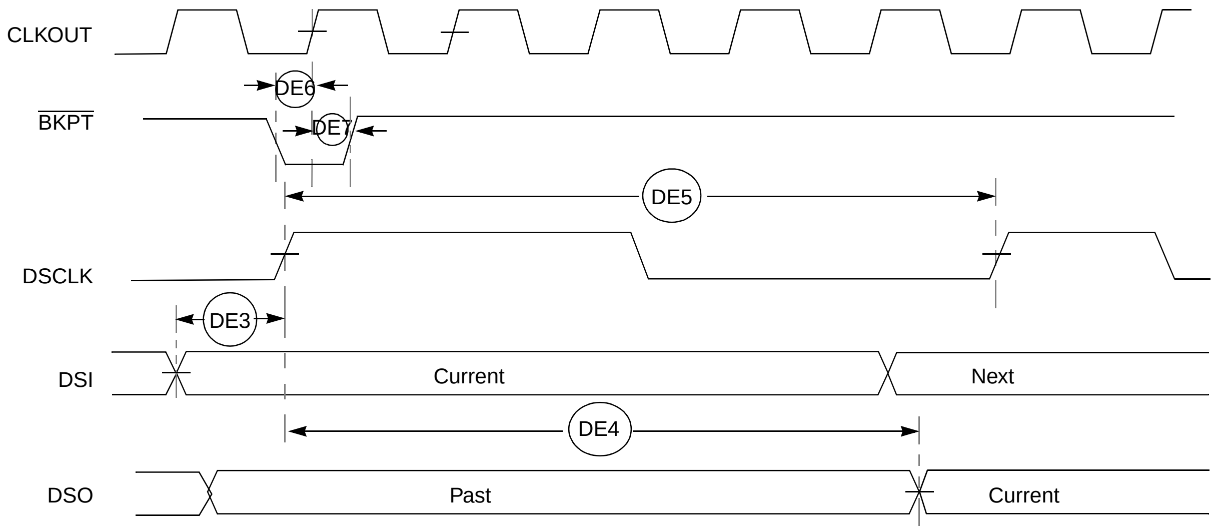


Figure 26. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF5271 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5271EC Revision History

Rev. No.	Substantive Change(s)
0	Initial release
1	• Fixed several clock values. • Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Removed detailed signal description section. This information can be found in the MCF5271RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5271RM Chapter 1. • Changed instances of Motorola to Freescale • Added values for 'Maximum operating junction temperature' in Table 8. • Added typical values for 'Core operating supply current (master mode)' in Table 9. • Added typical values for 'Pad operating supply current (master mode)' in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.

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Document Number: MCF5271EC
Rev. 4
08/2009