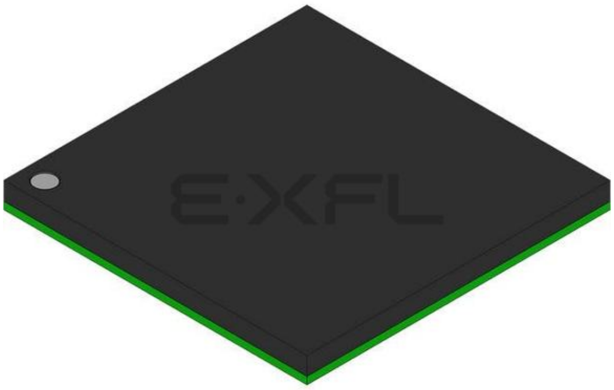


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5270cvm150j

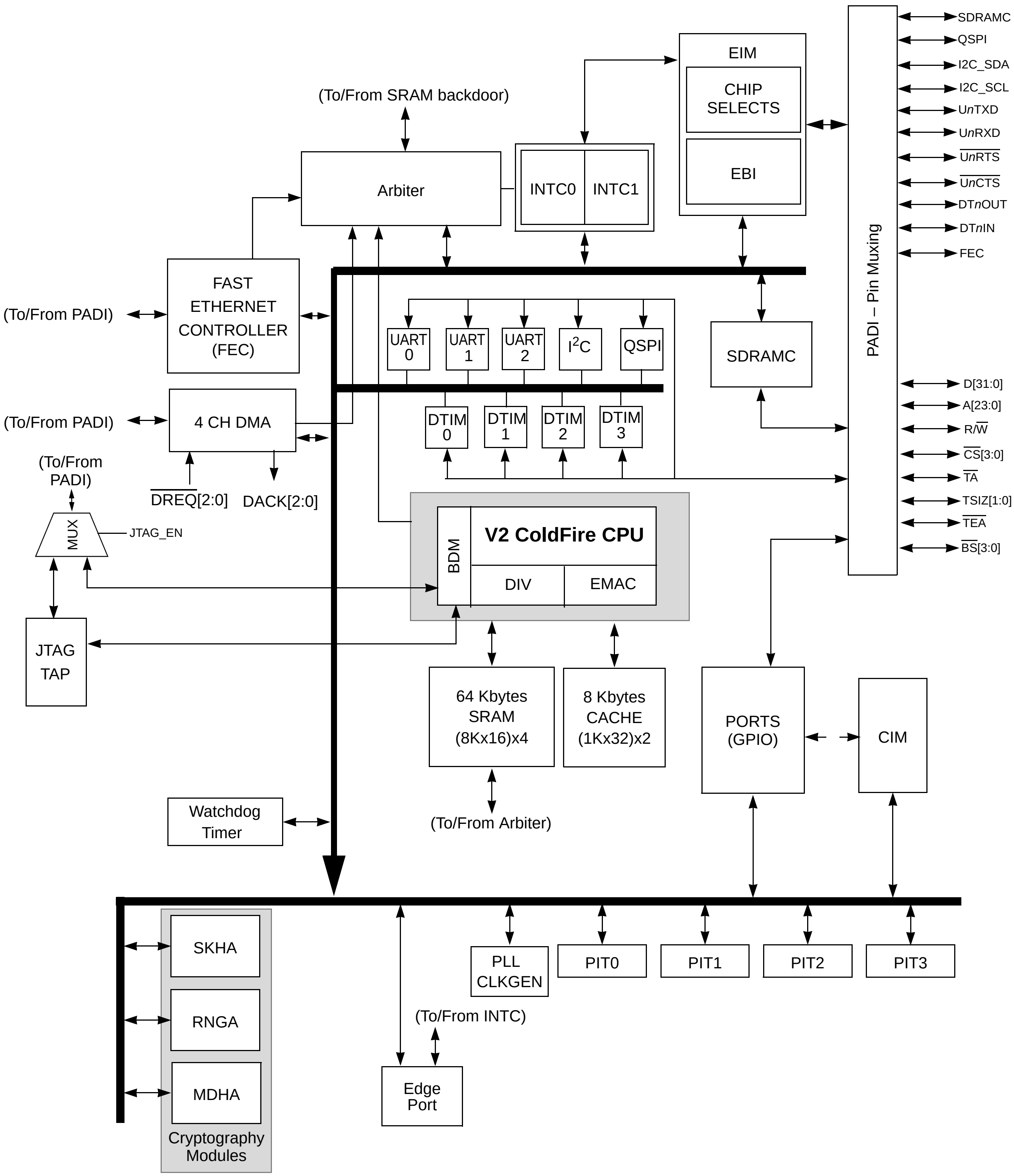


Figure 1. MCF5271 Block Diagram

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
UARTs						
U2TXD	PUARTH1	—	—	O	—	A8
U2RXD	PUARTH0	—	—	I	—	A7
$\overline{\text{U1CTS}}$	PUARTL7	$\overline{\text{U2CTS}}$	—	I	136	B8
$\overline{\text{U1RTS}}$	PUARTL6	$\overline{\text{U2RTS}}$	—	O	135	C8
U1TXD	PUARTL5	—	—	O	133	D9
U1RXD	PUARTL4	—	—	I	134	D8
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	12	F3
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	15	G3
U0TXD	PUARTL1	—	—	O	14	F1
U0RXD	PUARTL0	—	—	I	13	F2
DMA Timers						
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	66	M9
DT2OUT	PTIMER4	DACK2	—	O	—	L9
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	61	L6
DT1OUT	PTIMER2	DACK1	—	O	—	M6
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	10	E4
DT0OUT	PTIMER0	DACK0	—	O	11	F4
BDM/JTAG[2]						
DSCLK	—	TRST	—	O	70	N9
PSTCLK	—	TCLK	—	O	68	P9
$\overline{\text{BKPT}}$	—	TMS	—	O	71	P10
DSI	—	TDI	—	I	73	M10
DSO	—	TDO	—	O	72	N10
JTAG_EN	—	—	—	I	78	K9
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Test						
TEST	—	—	—	I	19	F5
PLL_TEST	—	—	—	I	—	
Power Supplies						
VDDPLL	—	—	—	I	87	M13
VSSPLL	—	—	—	I	84	L14
OVDD	—	—	—	I	1, 18, 32, 41, 55, 69, 81, 94, 105, 114, 128, 138, 145	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8
VSS	—	—	—	I	17, 31, 40, 54, 67, 80, 88, 93, 104, 113, 127, 137, 144, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14
VDD	—	—	—	I	16, 53, 103	D6, F11, G4, L4

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

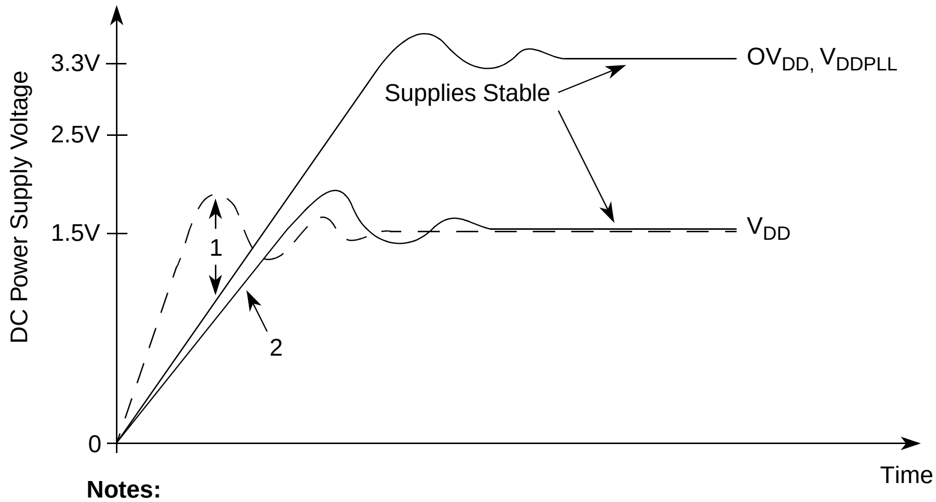
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5271.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33 µF, 0.1 µF, and 0.01 µF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}/V_{DDPLL} must power down. V_{DD} should not lag OV_{DD} or V_{DDPLL} going low by more than 0.4 V during power down or there

Table 3. Synchronous DRAM Signal Connections

Signal	Description
SD_SRAS	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. SD_SRAS should be connected to the corresponding SDRAM SD_SRAS. Do not confuse SD_SRAS with the DRAM controller's SD_CS[1:0], which should not be interfaced to the SDRAM SD_SRAS signals.
SD_SCAS	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. SD_SCAS should be connected to the corresponding signal labeled SD_SCAS on the SDRAM.
DRAMW	DRAM read/write. Asserted for write operations and negated for read operations.
SD_CS[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One SD_CS signal selects one SDRAM block and connects to the corresponding CS signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
BS[3:0]	Column address strobe. For synchronous operation, BS[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]

6.1 Pinout—196 MAPBGA

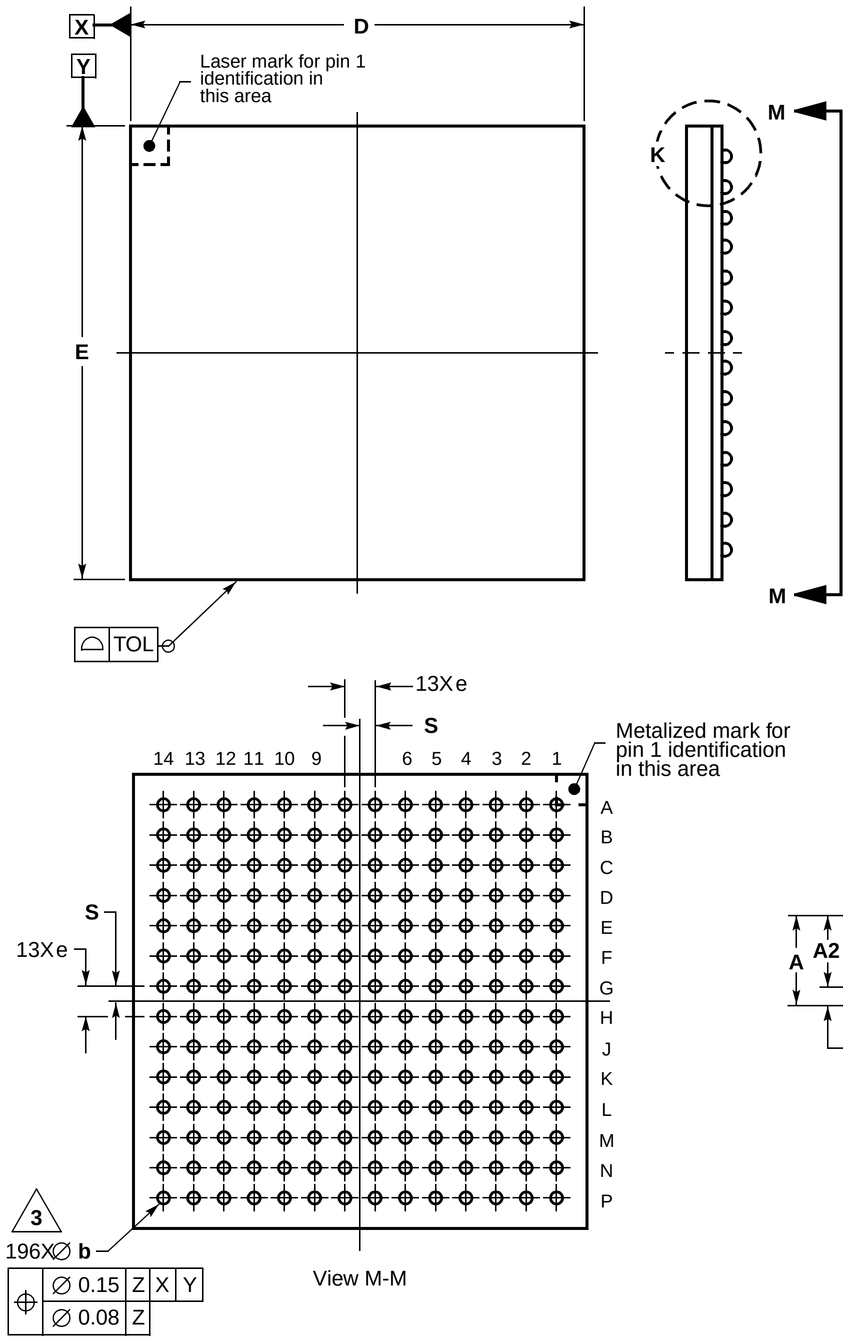
The following figure shows a pinout of the MCF5270/71CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	ETXCLK	ETXD3	ETXD2	QSPI_ DOUT	QSPI_CS0	U2RXD	U2TXD	CS3	CS6	CS4	A20	A17	VSS	A
B	ERXD0	ERXER	ETXER	ETXD0	QSPI_DIN	BS3	QSPI_CS1	U1CTS	CS7	CS1	A23	A19	A16	A15	B
C	ERXD2	ERXD1	ETXEN	ETXD1	QSCK	BS2	BS0	RTS1	CS2	CS5	A22	A18	A14	A13	C
D	ERXCLK	ERXDV	ERXD3	EMDC	EMDIO	Core VDD_4	BS1	U1RXD1	U1TXD	CS0	A21	A12	A11	A10	D
E	ECRS	ECOL	NC	TIN0	VDD	VSS	VDD	SD_CKE	VSS	VDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	U0CTS	DTOUT0	TEST	VSS	VDD	VSS	VDD	VSS	Core VDD_3	A5	A4	A3	F
G	D31	D30	U0RTS	Core VDD_1	CLK MOD1	VDD	VSS	VDD	VSS	NC	A2	A1	A0	DTOUT3	G
H	D29	D28	D27	D26	CLK MOD0	VSS	VDD	VDD	VDD	NC	TA	TIP	TS	DTIN3	H
J	D25	D24	D23	D22	VSS	VDD	VSS	VDD	VSS	VDD	I2C_SCL	I2C_SDA	R/W	TEA	J
K	D21	D20	D19	D18	VDD	VDD	VSS	VDD	JTAG_EN	RCON	SD_ RAS	SD_ CAS	SD_ WE	CLKOUT	K
L	D17	D16	D10	Core VDD_2	D3	DTIN1	IRQ5	IRQ1	DTOUT2	PST0	DDATA0	SD_ CS1	SD_ CS0	VSSPLL	L
M	D15	D13	D9	D6	D2	DTOUT1	IRQ6	IRQ2	DTIN2	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	OE	IRQ7	IRQ3	TRST/ DSCLK	TDO/DSO	PST2	DDATA2	RESET	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	IRQ4	TCLK/ PSTCLK	TMS/ BKPT	PST1	DDATA1	RSTOUT	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3. MCF5270/71CVMxxx Pinout (196 MAPBGA)

6.2 Package Dimensions—196 MAPBGA

Figure 4 shows MCF5270/71CVMxxx package dimensions.



NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

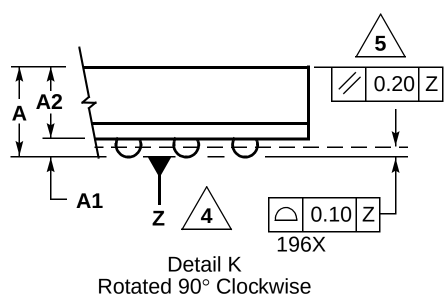


Figure 4. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5270AB100	MCF5270 RISC Microprocessor	160 QFP	100MHz	Yes	0° to +70° C
MCF5270CAB100	MCF5270 RISC Microprocessor	160 QFP	100MHz	Yes	-40° to +85° C
MCF5270VM100	MCF5270 RISC Microprocessor	196 MAPBGA	100MHz	Yes	0° to +70° C
MCF5270CVM150	MCF5270 RISC Microprocessor	196 MAPBGA	150MHz	Yes	-40° to +85° C
MCF5271CAB100	MCF5271 RISC Microprocessor	160 QFP	100MHz	Yes	-40° to +85° C
MCF5271CVM100	MCF5271 RISC Microprocessor	196 MAPBGA	100MHz	Yes	-40° to +85° C
MCF5271CVM150	MCF5271 RISC Microprocessor	196 MAPBGA	150MHz	Yes	-40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5271 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5271.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A $(T_L - T_H)$	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

Table 9. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Load Capacitance[4] Low drive strength High drive strength	C_L		— —	25 50	pF pF
Core Operating Supply Current [5] Master Mode	I_{DD}	—	135	150	mA
Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	— —	100 TBD	— —	mA µA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total processor Limit, Includes sum of all stressed pins	I_{IC}	–1.0 –10		1.0 10	mA mA

1 Refer to Table 10 for additional PLL specifications.
2 Refer to the MCF5271 signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.
4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.
5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
6 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.
7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

7.4 Oscillator and PLLMRFM Electrical Characteristics

Table 10. HiP7 PLLMRFM Electrical Specifications[1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference 1:1 mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$)	$f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	8 8 24	25 25 75	MHz
2	Core frequency CLKOUT Frequency [2] External reference On-Chip PLL Frequency	f_{sys} $f_{sys/2}$	0 $f_{ref} \div 32$	150 75 75	MHz MHz MHz
3	Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
4	Self Clocked Mode Frequency [4, 5]	f_{SCM}	10.25	15.25	MHz
5	Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..
2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

Timings listed in Table 11 are shown in Figure 7.

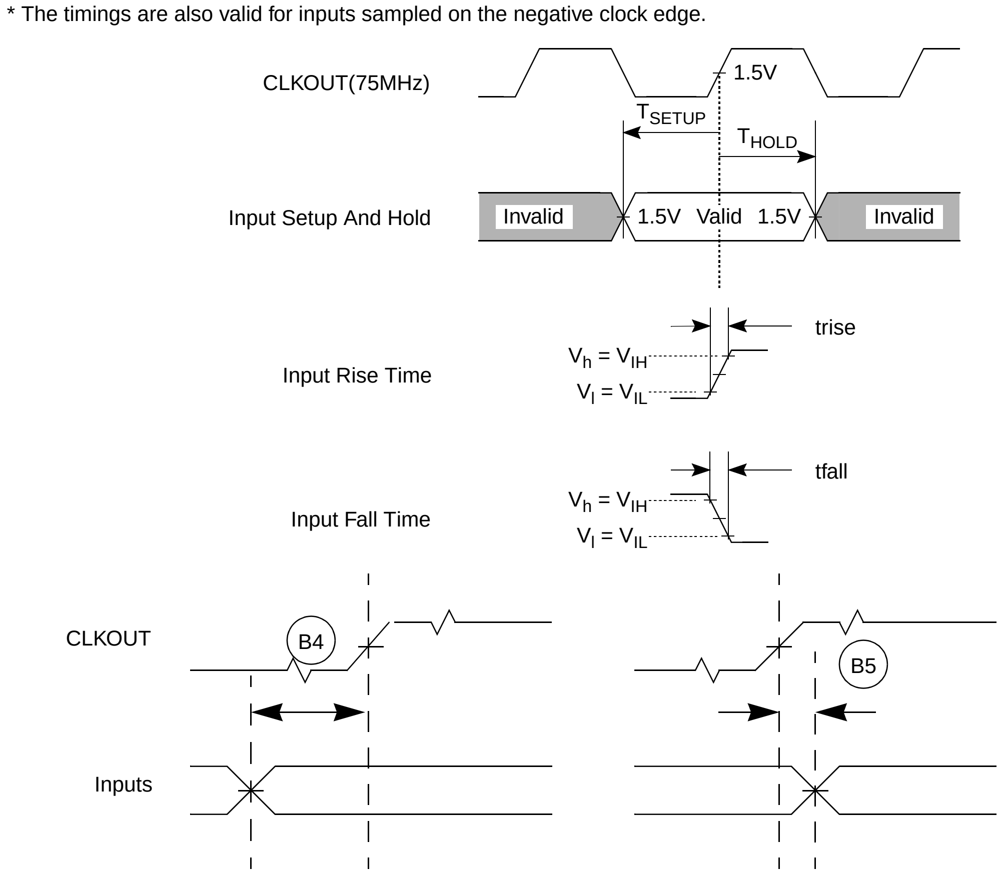


Figure 7. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

Read/write bus timings listed in Table 12 are shown in Figure 8, Figure 9, and Figure 10.

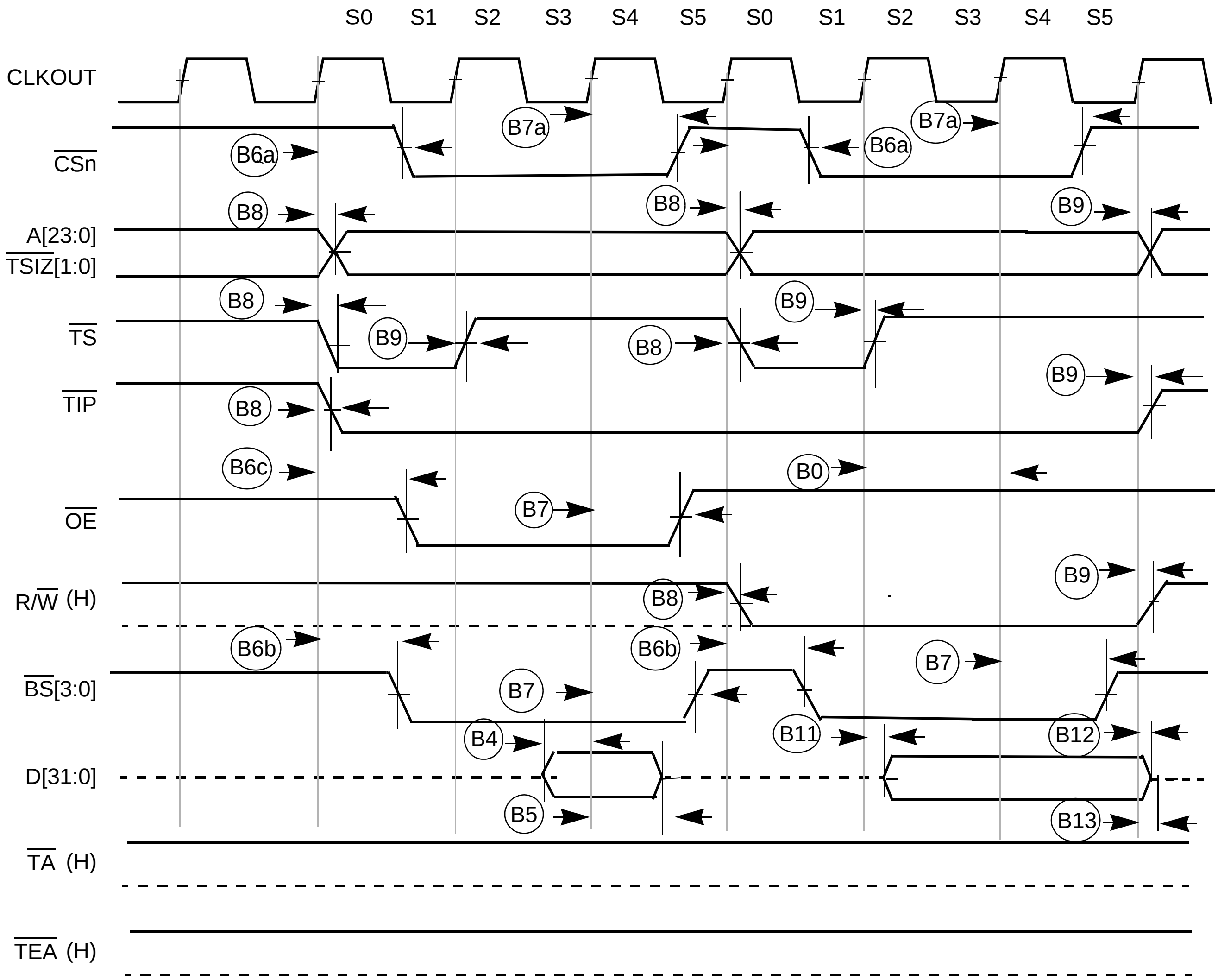


Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 10 shows an SRAM bus cycle terminated by $\overline{TEA}$ showing timings listed in Table 12.

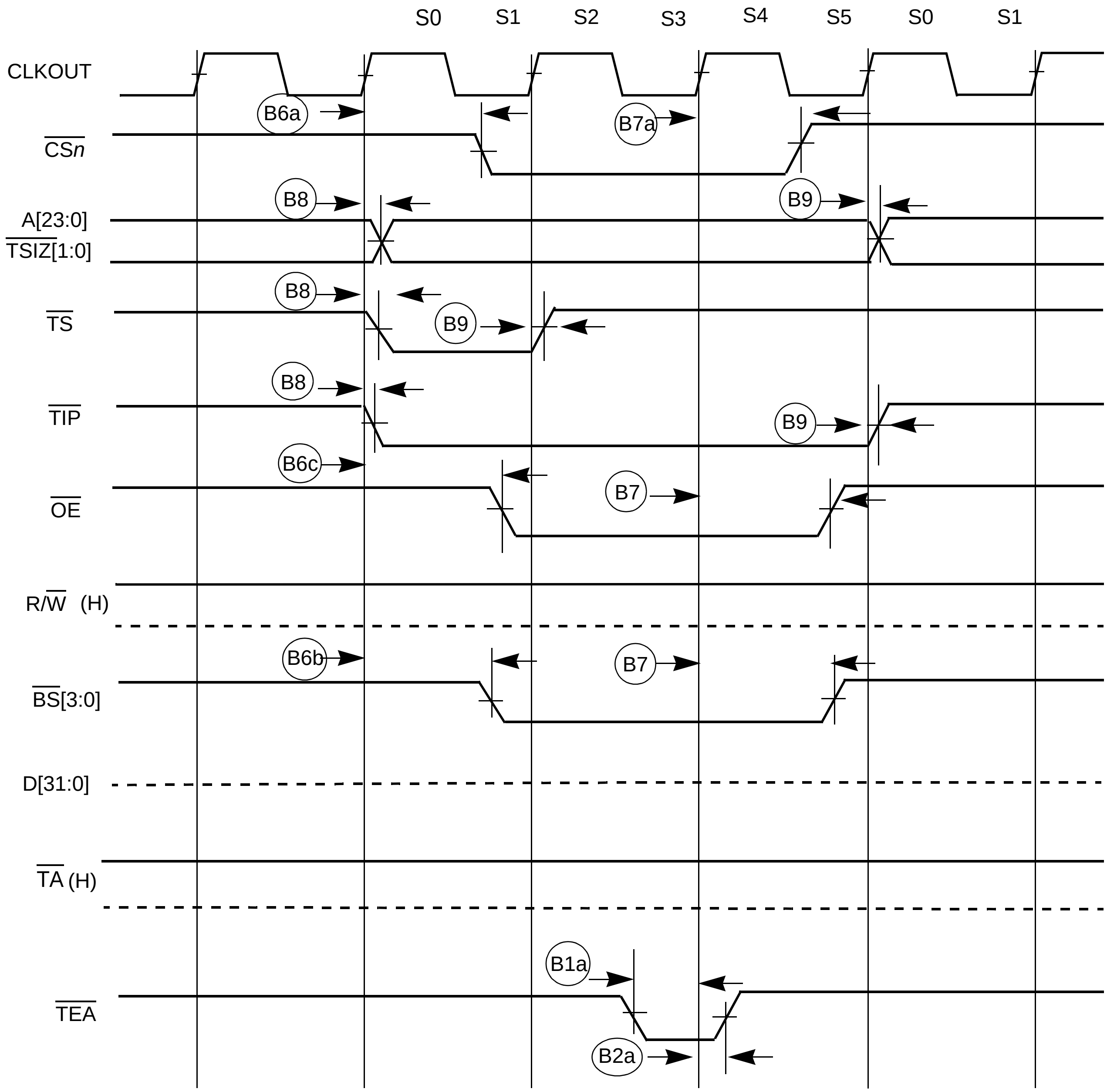


Figure 10. SRAM Read Bus Cycle Terminated by $\overline{TEA}$

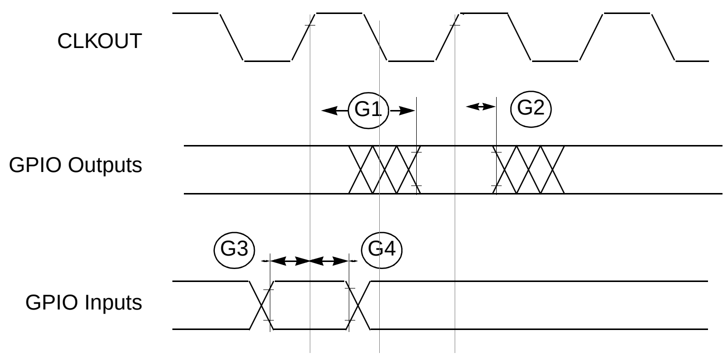


Figure 13. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

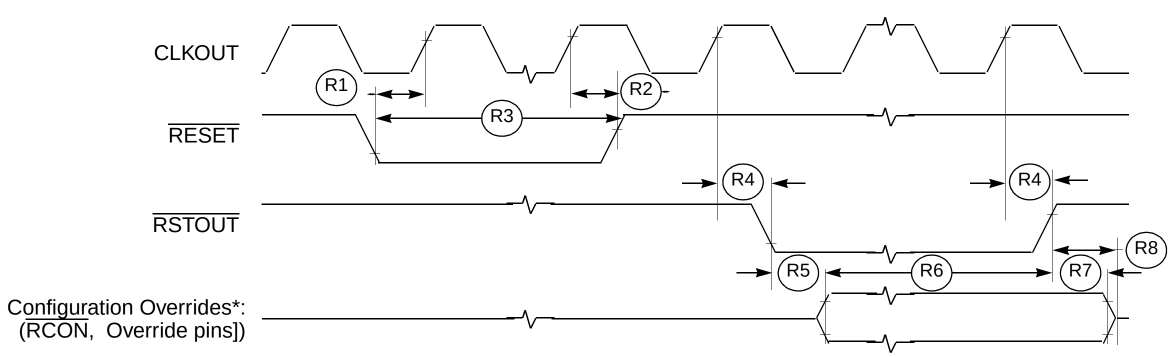


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

7.9 I^2C Input/Output Timing Specifications

Table 16 lists specifications for the I^2C input timing parameters shown in Figure 15.

Table 16. I^2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17 lists specifications for the I^2C output timing parameters shown in Figure 15.

Table 17. I^2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1 [1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

[1] Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

[2] Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

[3] Specified at a nominal 50-pF load.

Figure 15 shows timing for the values in Table 16 and Table 17.

7.10.2 MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a ETXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ETXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	ETXCLK to ETXD[3:0], ETXEN, ETXER invalid	5	—	ns
M6	ETXCLK to ETXD[3:0], ETXEN, ETXER valid	—	25	ns
M7	ETXCLK pulse width high	35%	65%	ETXCLK period
M8	ETXCLK pulse width low	35%	65%	ETXCLK period

Figure 17 shows MII transmit signal timings listed in Table 19.

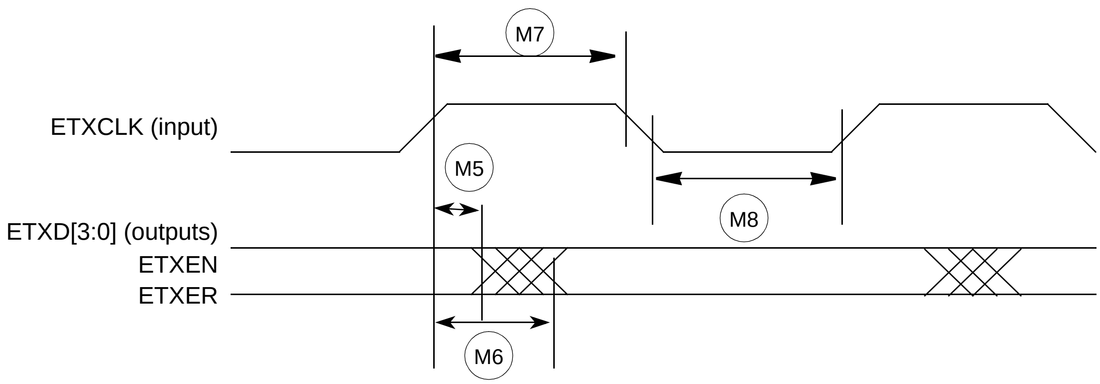


Figure 17. MII Transmit Signal Timing Diagram

7.10.3 MII Async Inputs Signal Timing (ECRS and ECOL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	ECRS, ECOL minimum pulse width	1.5	—	ETXCLK period

Figure 18 shows MII asynchronous input timings listed in Table 20.

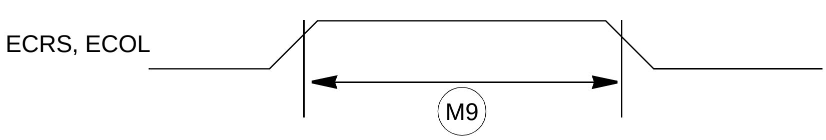


Figure 18. MII Async Inputs Timing Diagram

7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[1:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 20.

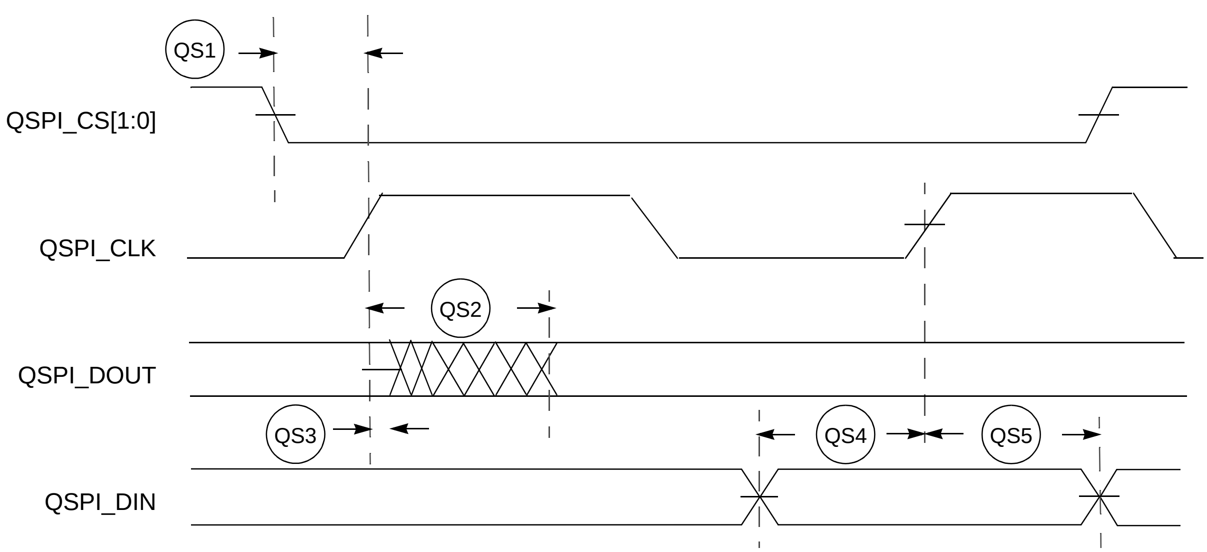


Figure 20. QSPI Timing

7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

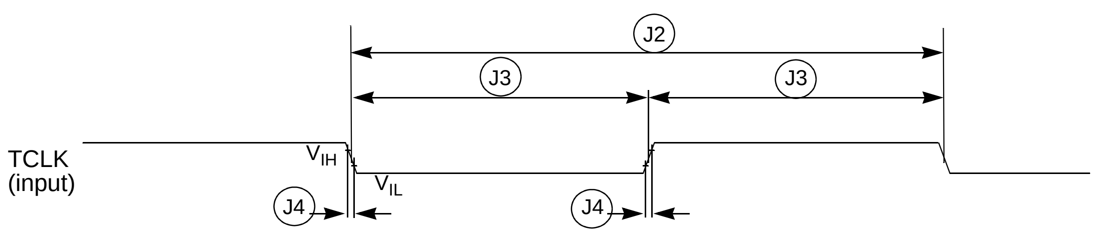


Figure 21. Test Clock Input Timing

7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 26.

Table 25. Debug AC Timing Specification

Num	Characteristic	150 MHz		Units
		Min	Max	
DE0	PSTCLK cycle time	—	0.5	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
DE7	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0	10	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 25 shows real-time trace timing for the values in Table 25.

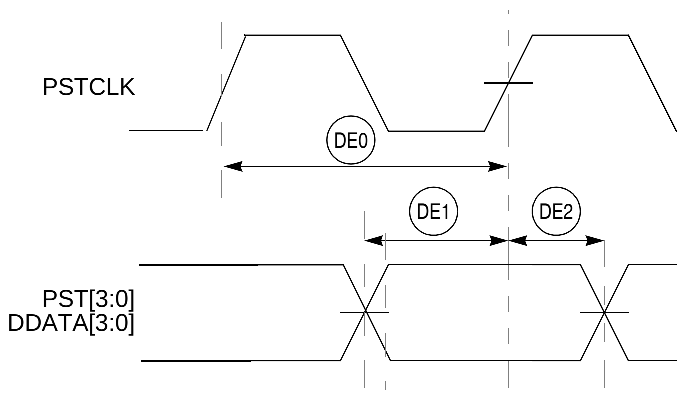


Figure 25. Real-Time Trace AC Timing

Figure 26 shows BDM serial port AC timing for the values in Table 25.

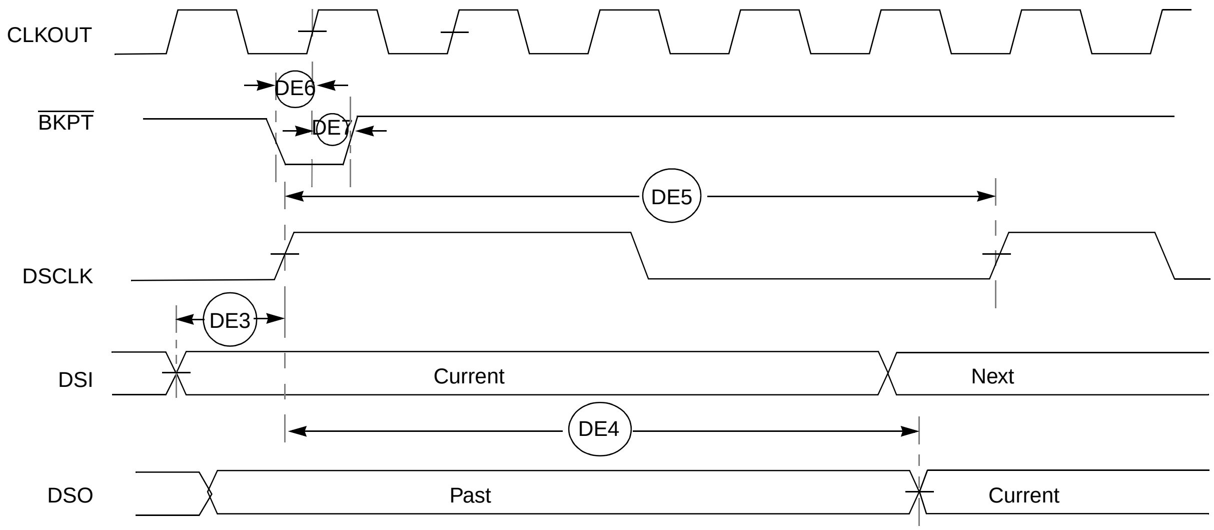


Figure 26. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF5271 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5271EC Revision History

Rev. No.	Substantive Change(s)
0	Initial release
1	• Fixed several clock values. • Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Removed detailed signal description section. This information can be found in the MCF5271RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5271RM Chapter 1. • Changed instances of Motorola to Freescale • Added values for 'Maximum operating junction temperature' in Table 8. • Added typical values for 'Core operating supply current (master mode)' in Table 9. • Added typical values for 'Pad operating supply current (master mode)' in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.