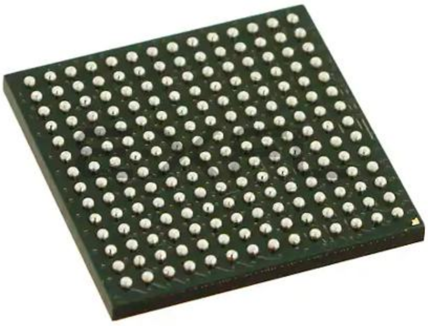

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5270cvm150r2

1 MCF5271 Family Configurations

Table 1. MCF5271 Family Configurations

Module	MCF5270	MCF5271
ColdFire V2 Core with EMAC and Hardware Divide	x	x
System Clock	150 MHz	
Performance (Dhrystone/2.1 MIPS)	144	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	64 Kbytes	
Interrupt Controllers (INTC)	2	2
Edge Port Module (EPORT)	x	x
External Interface Module (EIM)	x	x
4-channel Direct-Memory Access (DMA)	x	x
SDRAM Controller	x	x
Fast Ethernet Controller (FEC)	x	x
Hardware Encryption	—	x
Watchdog Timer (WDT)	x	x
Four Periodic Interrupt Timers (PIT)	x	x
32-bit DMA Timers	4	4
QSPI	x	x
UART(s)	3	3
I^2C	x	x
General Purpose I/O Module (GPIO)	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x
Package	160 QFP, 196 MAPBGA	160 QFP, 196 MAPBGA

2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array plastic ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

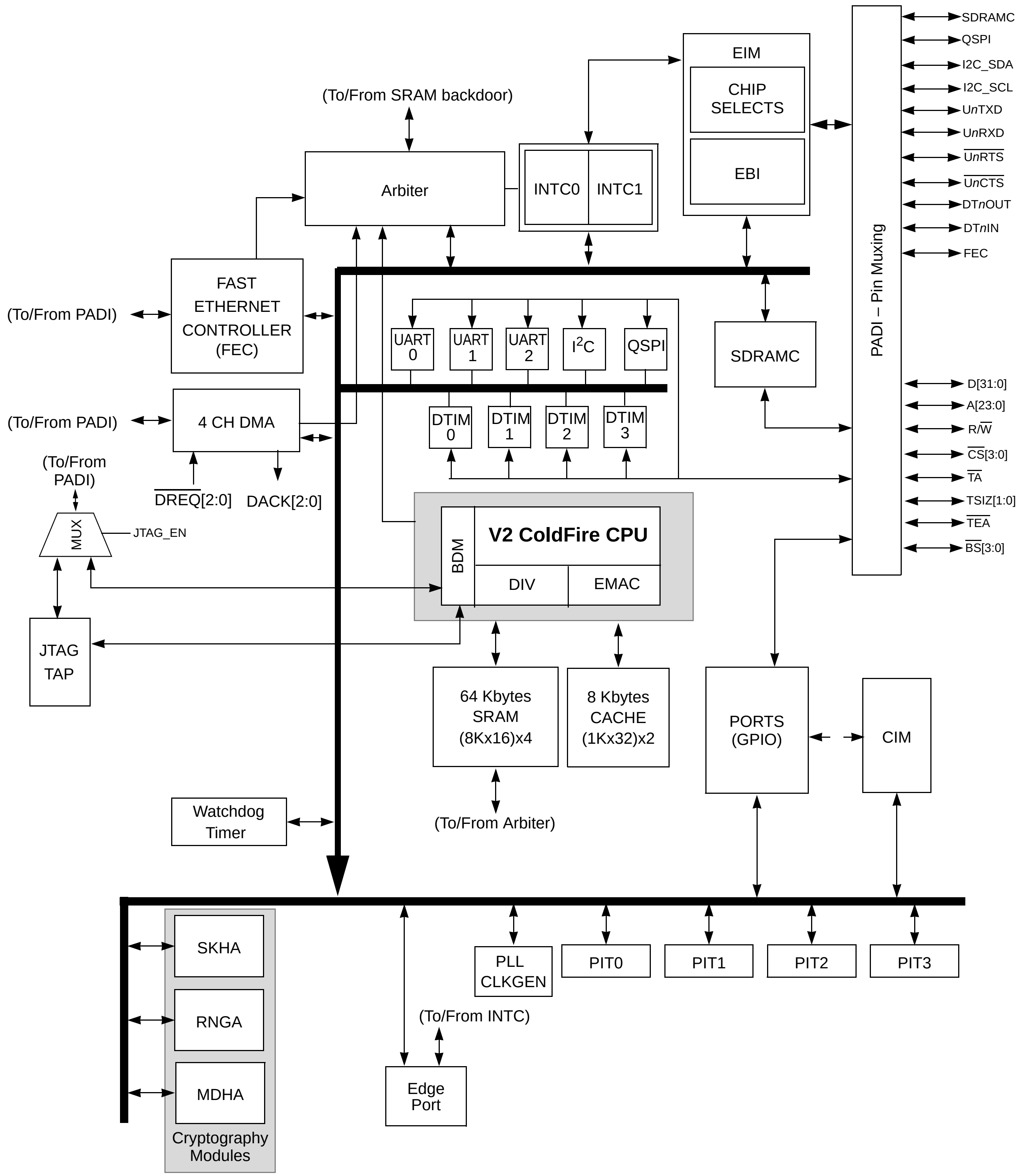


Figure 1. MCF5271 Block Diagram

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Test						
TEST	—	—	—	I	19	F5
PLL_TEST	—	—	—	I	—	
Power Supplies						
VDDPLL	—	—	—	I	87	M13
VSSPLL	—	—	—	I	84	L14
OVDD	—	—	—	I	1, 18, 32, 41, 55, 69, 81, 94, 105, 114, 128, 138, 145	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8
VSS	—	—	—	I	17, 31, 40, 54, 67, 80, 88, 93, 104, 113, 127, 137, 144, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14
VDD	—	—	—	I	16, 53, 103	D6, F11, G4, L4

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

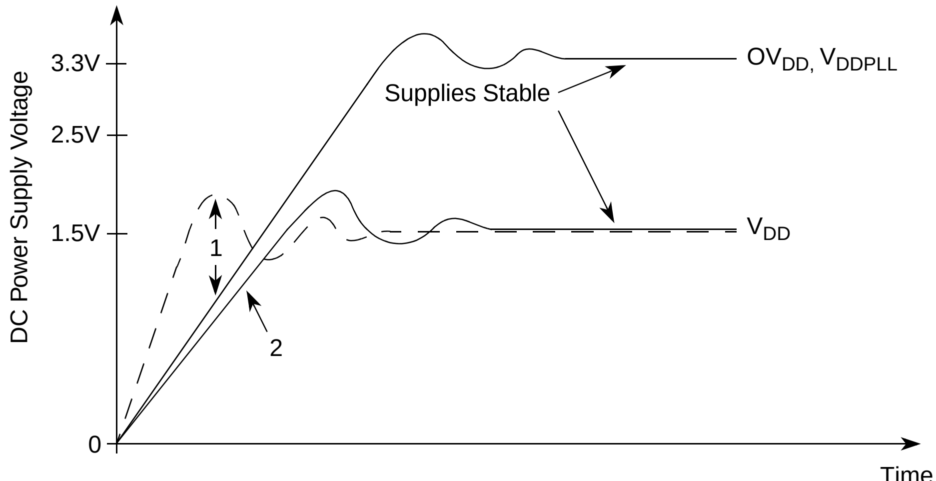
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5271.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33 µF, 0.1 µF, and 0.01 µF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}/V_{DDPLL} must power down. V_{DD} should not lag OV_{DD} or V_{DDPLL} going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/V_{DDPLL} supplies.

5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, "Electrical Characteristics."

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
SD_SRAS	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. SD_SRAS should be connected to the corresponding SDRAM SD_SRAS. Do not confuse SD_SRAS with the DRAM controller's SD_CS[1:0], which should not be interfaced to the SDRAM SD_SRAS signals.
SD_SCAS	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. SD_SCAS should be connected to the corresponding signal labeled SD_SCAS on the SDRAM.
DRAMW	DRAM read/write. Asserted for write operations and negated for read operations.
SD_CS[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One SD_CS signal selects one SDRAM block and connects to the corresponding CS signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
BS[3:0]	Column address strobe. For synchronous operation, BS[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

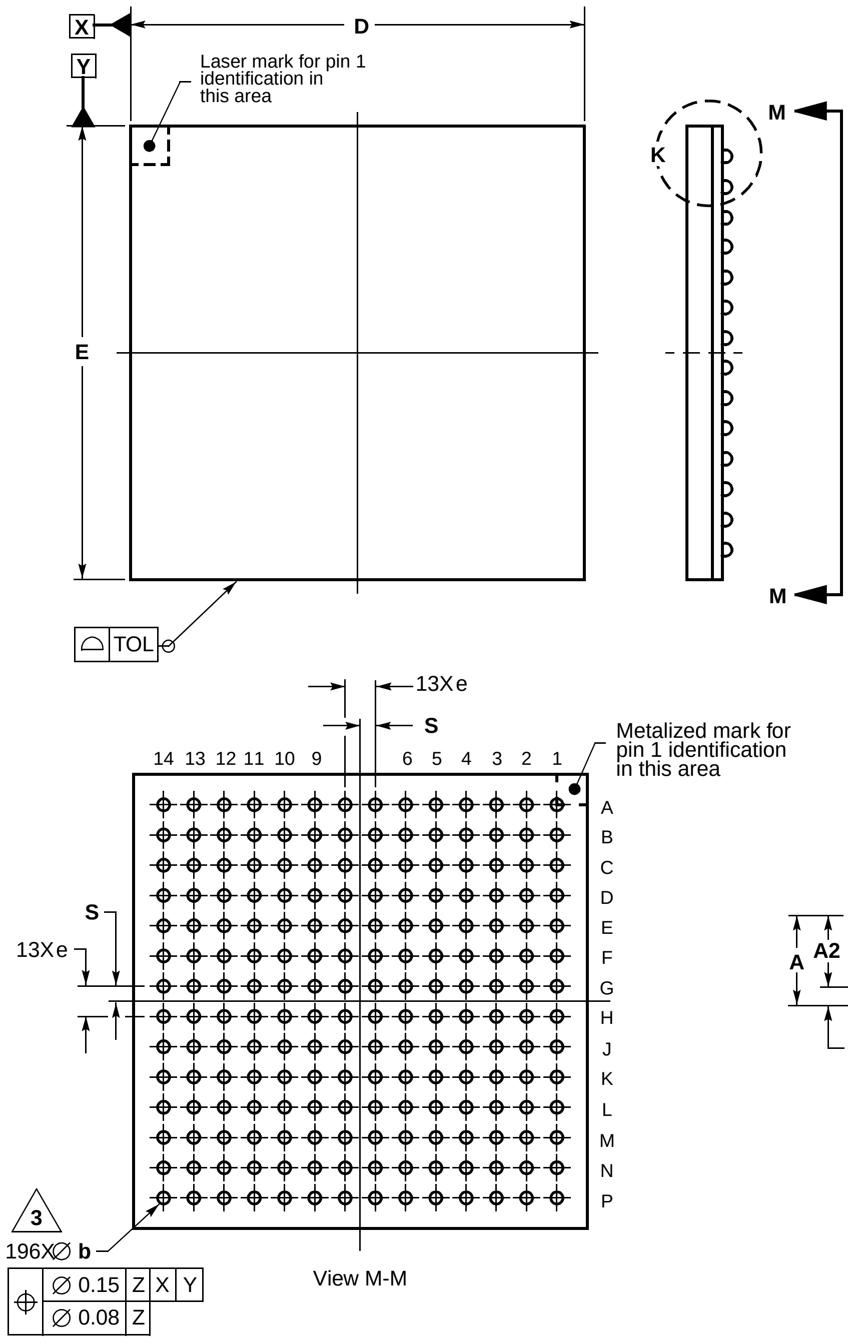
The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]

6.2 Package Dimensions—196 MAPBGA

Figure 4 shows MCF5270/71CVMxxx package dimensions.



NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

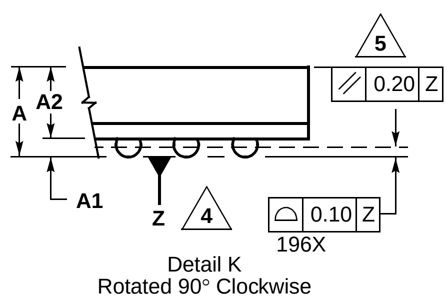
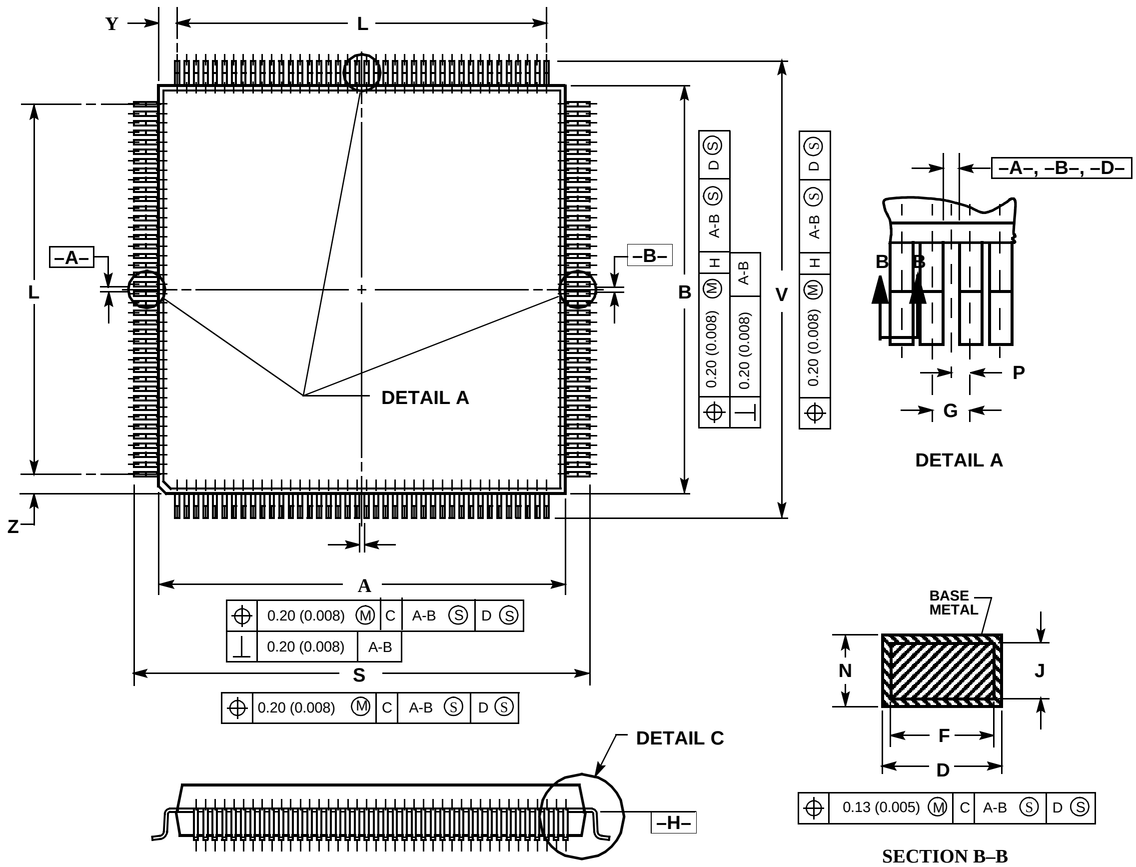
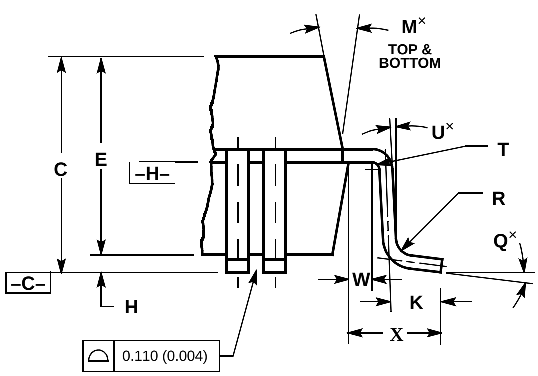


Figure 4. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

6.4 Package Dimensions—160 QFP

Figure 6 shows MCF5270/71CAB80 package dimensions.





DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 6. 160 QFP Package Dimensions

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.

5 Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2 Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	104	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

Table 10. HiP7 PLLMRFM Electrical Specifications[1] (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
6	XTAL Load Capacitance[5]		5	30	pF
7	PLL Lock Time [5, 7,13]	t_{lpll}	—	750	µs
8	Power-up To Lock Time [5, 6,8] With Crystal Reference (includes 5 time) Without Crystal Reference[9]	t_{lplk}	 — —	 11 750	 ms µs
9	1:1 Mode Clock Skew (between CLKOUT and EXTAL) [10]	t_{skew}	–1	1	ns
10	Duty Cycle of reference [5]	t_{dc}	40	60	%
11	Frequency un-LOCK Range	f_{UL}	–3.8	4.1	% $f_{sys/2}$
12	Frequency LOCK Range	f_{LCK}	–1.7	2.0	% $f_{sys/2}$
13	CLKOUT Period Jitter, [5, 6, 8,11, 12] Measured at $f_{sys/2}$ Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5.0 .01	% $f_{sys/2}$
14	Frequency Modulation Range Limit[13,14] ($f_{sys/2}$ Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/2}$
15	ICO Frequency. $f_{ico} = f_{ref} \times 2 \times (MFD+2)$ [15]	f_{ico}	48	150	MHz

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
9 $t_{lpll} = (64 * 4 * 5 + 5 \tau) T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6}$ 2(MFD + 2).
10 PLL is operating in 1:1 PLL mode.
11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.
12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.
13 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

Timings listed in Table 11 are shown in Figure 7.

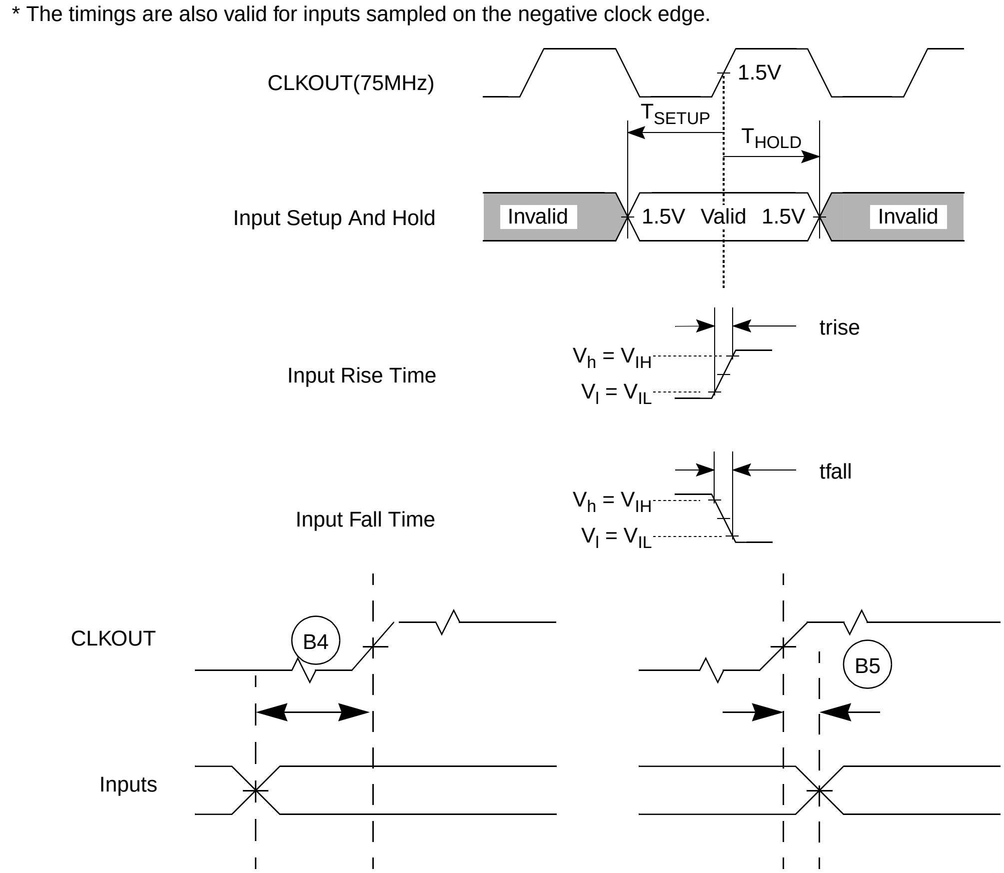


Figure 7. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

[1] $\overline{CS}$ transitions after the falling edge of CLKOUT.
[2] $\overline{BS}$ transitions after the falling edge of CLKOUT.
[3] $\overline{OE}$ transitions after the falling edge of CLKOUT.

Read/write bus timings listed in Table 12 are shown in Figure 8, Figure 9, and Figure 10.

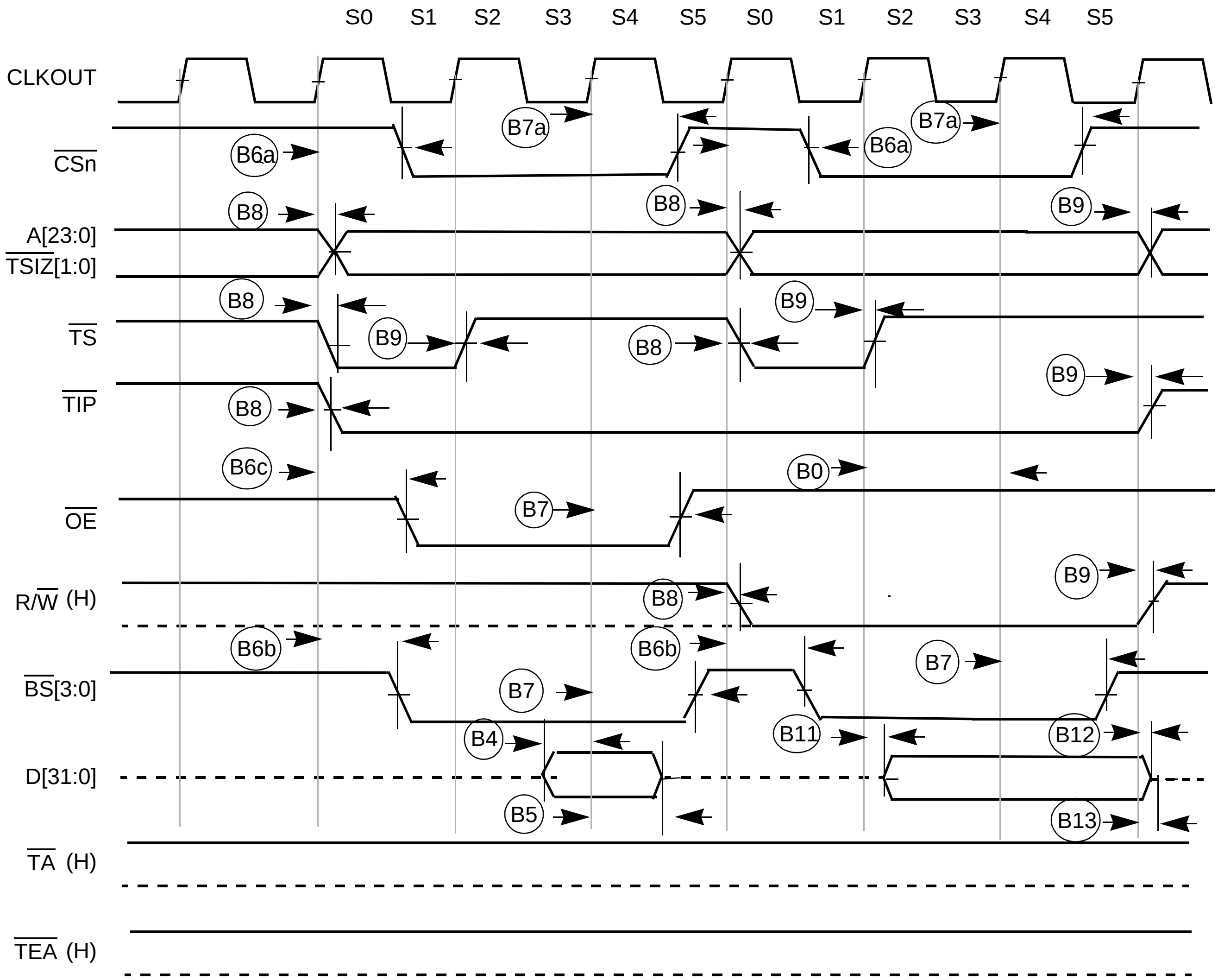
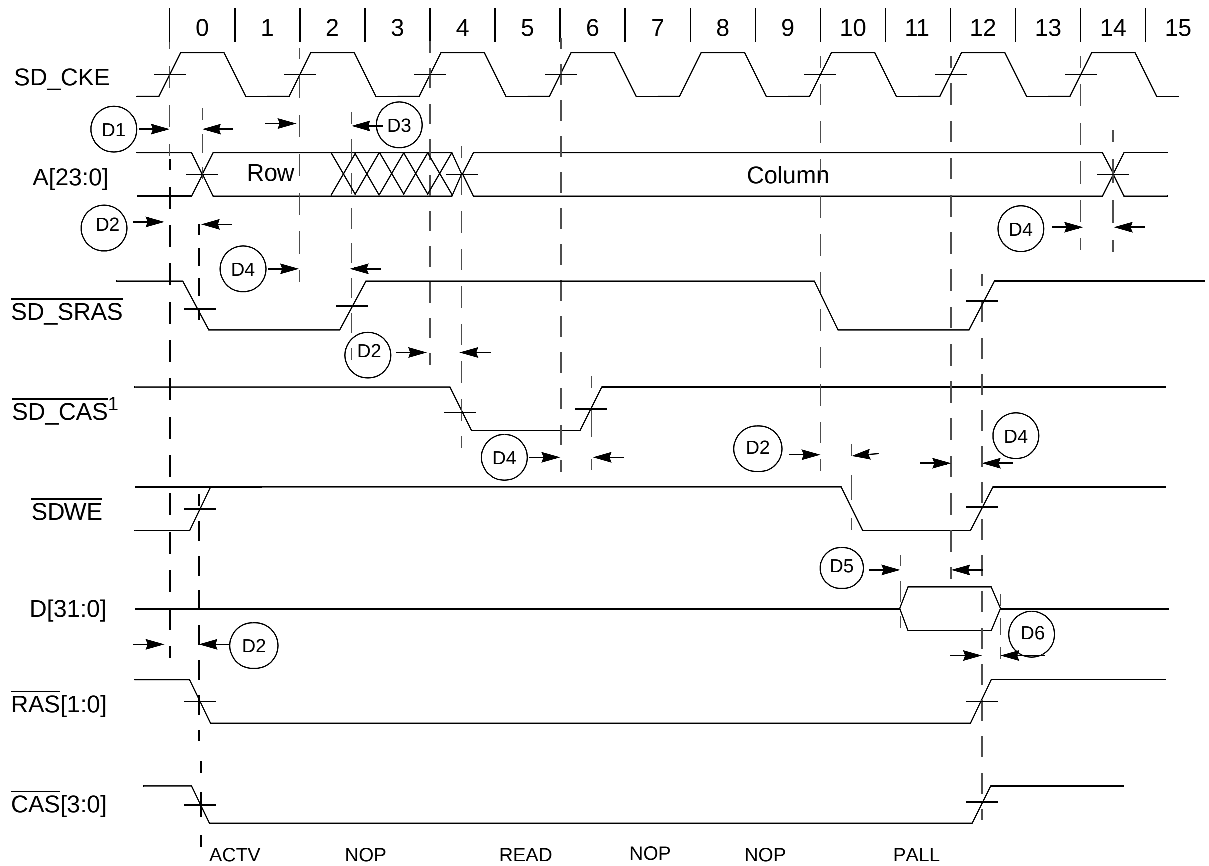


Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 11 shows an SDRAM read cycle.



[1] DACR[CASL] = 2

Figure 11. SDRAM Read Cycle

Table 13. SDRAM Timing

NUM	Characteristic	Symbol	Min	Max	Unit
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}	—	9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.5	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.5	—	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	4	—	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.5	—	ns
D7[1]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	—	9	ns
D8[1]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.5	—	ns

[1] D7 and D8 are for write cycles only.

Figure 12 shows an SDRAM write cycle.

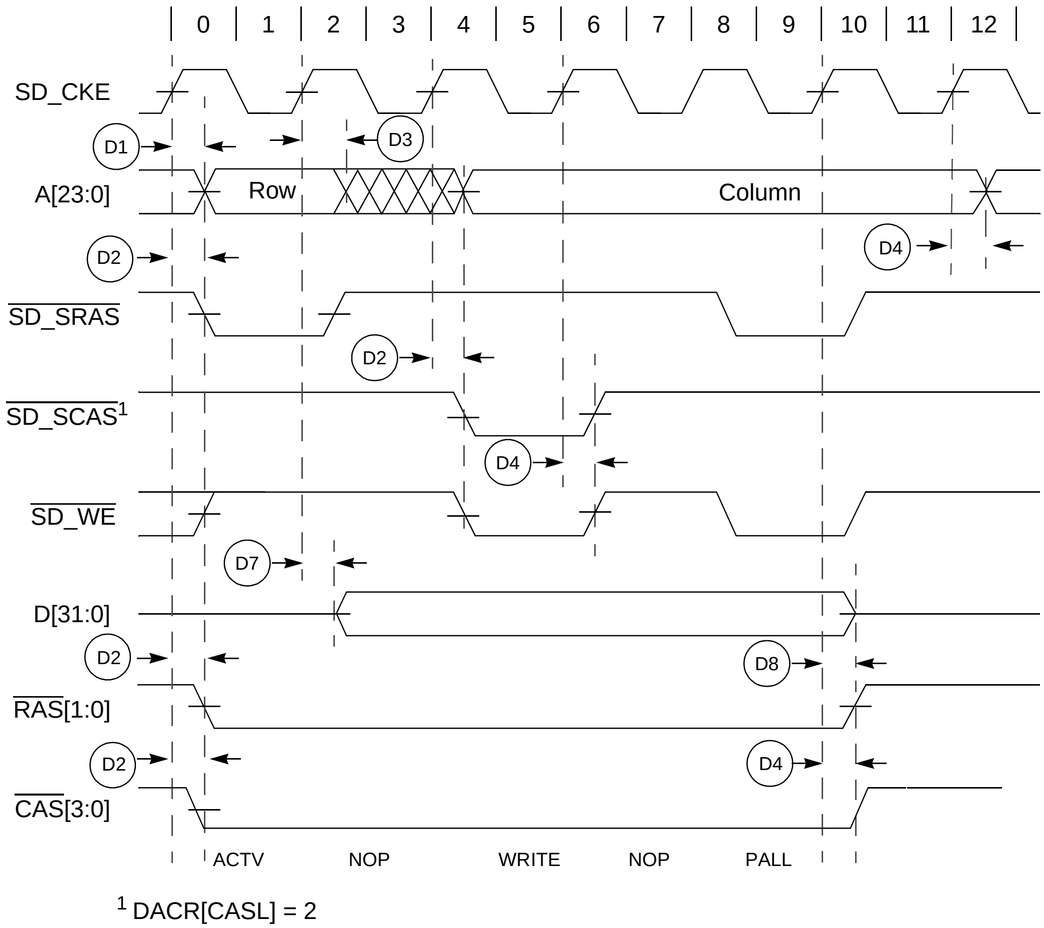


Figure 12. SDRAM Write Cycle

7.7 General Purpose I/O Timing

Table 14. GPIO Timing[1]

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

[1] GPIO pins include: INT, UART, Timer, DREQ*n* and DACK*n* pins.

7.10.4 MII Serial Management Channel Timing (EMDIO and EMDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	EMDC falling edge to EMDIO output invalid (minimum propagation delay)	0	—	ns
M11	EMDC falling edge to EMDIO output valid (max prop delay)	—	25	ns
M12	EMDIO (input) to EMDC rising edge setup	10	—	ns
M13	EMDIO (input) to EMDC rising edge hold	0	—	ns
M14	EMDC pulse width high	40%	60%	MDC period
M15	EMDC pulse width low	40%	60%	MDC period

Figure 19 shows MII serial management channel timings listed in Table 21.

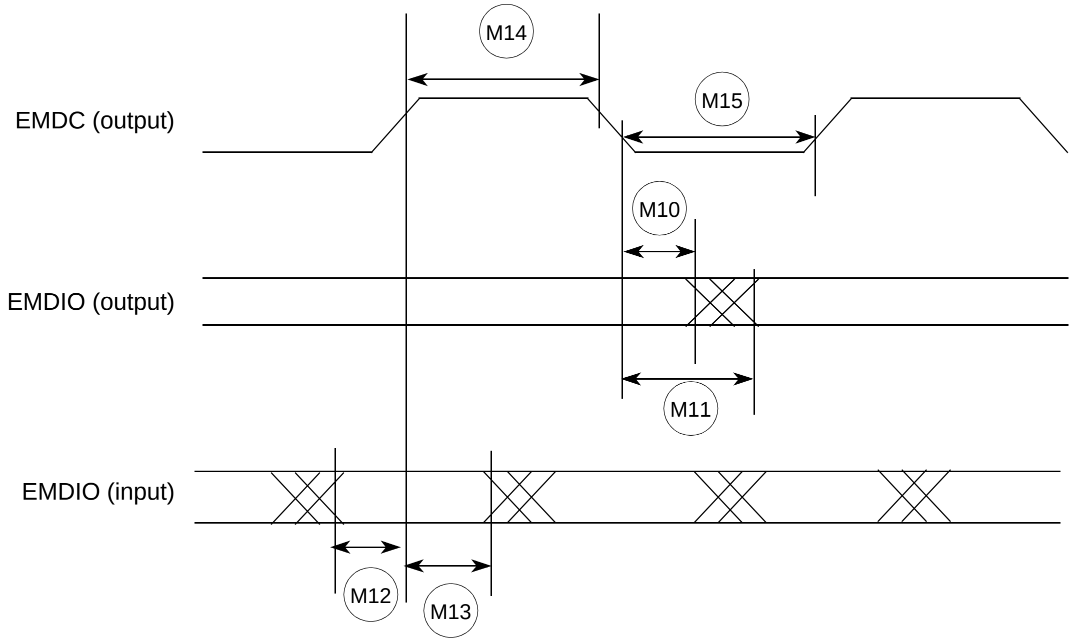


Figure 19. MII Serial Management Channel Timing Diagram

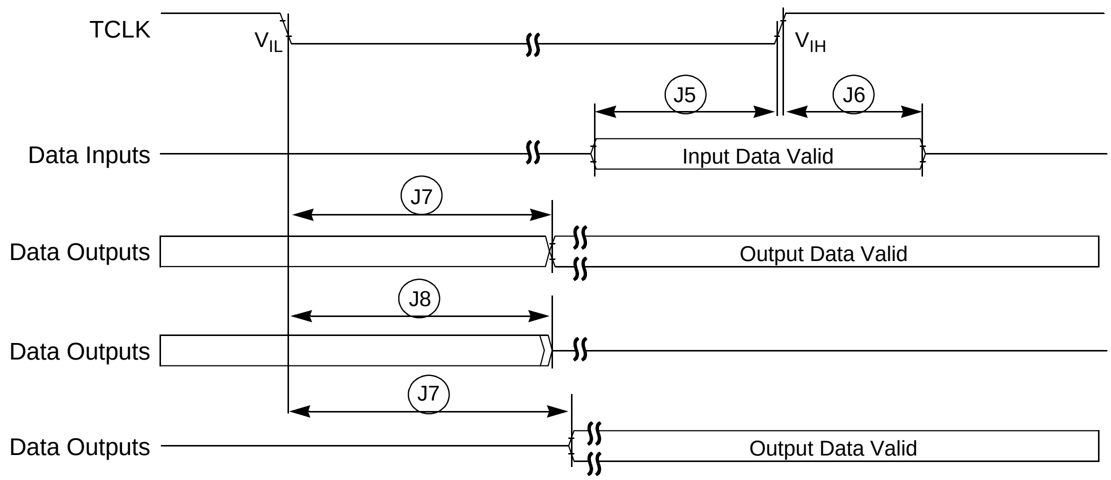


Figure 22. Boundary Scan (JTAG) Timing

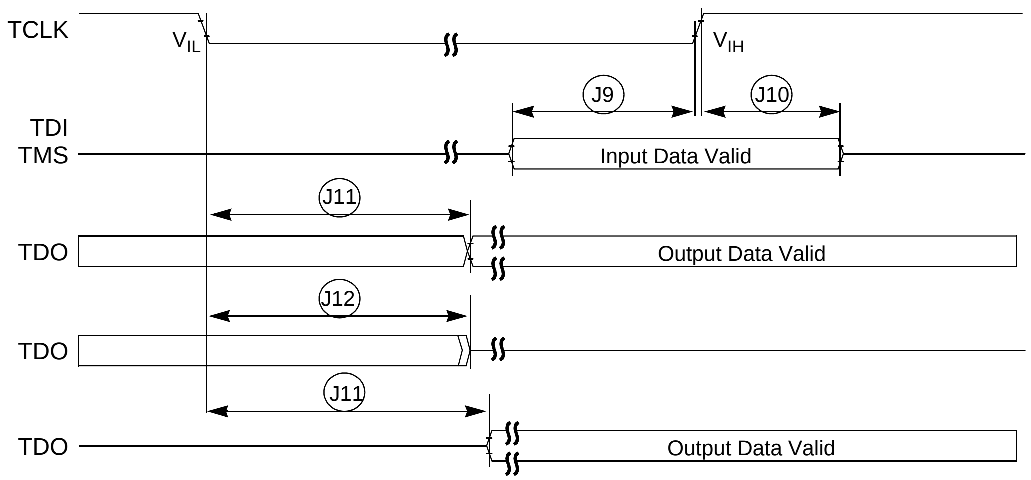


Figure 23. Test Access Port Timing

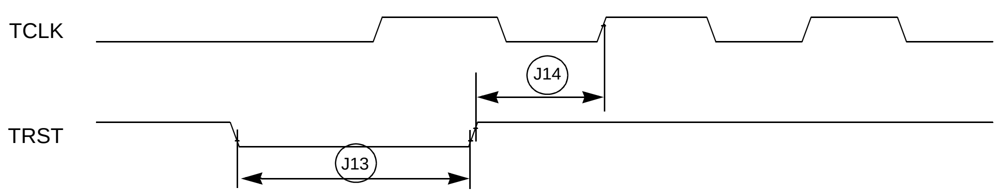


Figure 24. $\overline{\text{TRST}}$ Timing

7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 26.

Table 25. Debug AC Timing Specification

Num	Characteristic	150 MHz		Units
		Min	Max	
DE0	PSTCLK cycle time	—	0.5	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
DE7	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0	10	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 25 shows real-time trace timing for the values in Table 25.

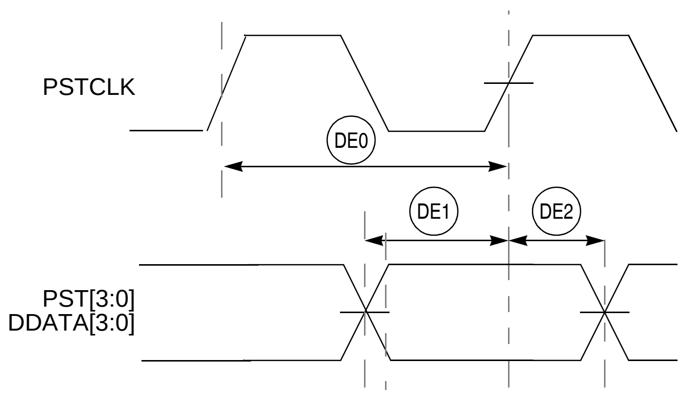


Figure 25. Real-Time Trace AC Timing

Figure 26 shows BDM serial port AC timing for the values in Table 25.

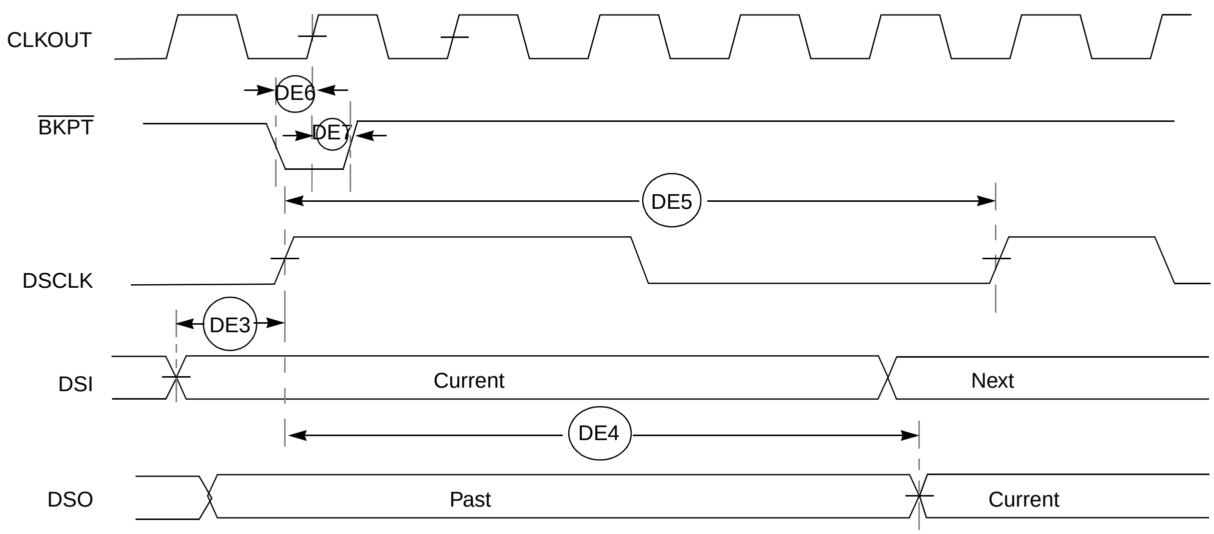


Figure 26. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF5271 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5271EC Revision History

Rev. No.	Substantive Change(s)
0	Initial release
1	• Fixed several clock values. • Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Removed detailed signal description section. This information can be found in the MCF5271RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5271RM Chapter 1. • Changed instances of Motorola to Freescale • Added values for ‘Maximum operating junction temperature’ in Table 8. • Added typical values for ‘Core operating supply current (master mode)’ in Table 9. • Added typical values for ‘Pad operating supply current (master mode)’ in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.